

PROGRAMME LOGIC CALL AND ARRAY

ABSTRACT

An improved programmable logic cell (1) for use in a programmable logic array comprising cells which are arranged in two-dimensional matrix of rows and columns and are interconnected by a two-dimensional array of direct connections between a cell (1) and its four nearest neighbors, one to its left (or to the West) (3a, 3b, 7a, 7b) and one to its right (or to the East) (5a, 5b, 9a, 9b), one above it (or to the North) (2a, 2b, 6a, 6b) and one below it (or to the South) (4a, 4b, 8a, 8b). Each cell receives input(s) from each of its nearest neighbors and additional input(s) from a bus, pin, or neighbor and may be programmed to generate a variety of logical functions at its outputs which connect to the cell's four nearest neighbors. The core of the improved logic cell (fig. 2) comprises two upstream gates (21,23) the outputs of which feed two downstream gates (28,41), one of which is an exclusive-OR gate (28) which feeds a downstream register (33). Additional programmable connections and other logic augment the cell core to produce cell embodiments which can be configured to efficiently implement various logical functions. Among the functions which may be implemented by the improved cell are a number of two-level combinational functions (such as multiplexing) and sequential functions (such as counting and shifting). A variety of cell embodiments based on the improved cell core are illustrated.

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FIGURE 1

