

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a cell array region connected to a peripheral circuit region,
the cell array region including a plurality of electrode structures and a plurality of vertical structures on a body conductive layer, the plurality of electrode structure each including a plurality of electrodes that are sequentially stacked on the body conductive layer, the plurality of vertical structures penetrating the plurality of electrode structures and being connected to the body conductive layer,
the peripheral circuit region including a peripheral transistor on a residual substrate,
and
a top surface of the residual substrate being higher than a top surface of the body conductive layer,
the body conductive layer including a polycrystalline semiconductor layer.
2. The device of claim 1, wherein the body conductive layer extends below the residual substrate.
3. The device of claim 1, wherein a thickness of the body conductive layer is less than a thickness of the residual substrate.
4. The device of claim 1, wherein the residual substrate includes a single-crystalline layer.
5. The device of claim 1, wherein
each of the plurality of vertical structures includes a channel semiconductor layer and a data storage layer, and

the body conductive layer is connected to the channel semiconductor layer.

6. The device of claim 5, wherein a bottom surface of the channel semiconductor layer is at the same level as a bottom surface of the data storage layer.

7. The device of claim 1, further comprising:
an etch stop layer between the plurality of electrode structures and the body conductive layer,
wherein the plurality of vertical structures penetrate the etch stop layer.

8. The device of claim 1, further comprising:
a common source conductive line that extends between the plurality of electrode structures, wherein the common source conductive line is connected to the body conductive layer.

9. The device of claim 1, wherein
the body conductive layer includes a metal layer, and
the metal layer is spaced apart from the plurality of vertical structures across the polycrystalline semiconductor layer.

10. The device of claim 1, further comprising:
a plurality of insulation patterns lying in and penetrating through the body conductive layer.

11. The device of claim 1, further comprising:
an insulation pattern below the residual substrate such that the residual substrate is on the insulation pattern,

wherein the body conductive layer is locally provided in the cell array region.

12. The device of claim 1, wherein, on the cell array region, the residual substrate extends between the body conductive layer and the plurality of electrode structures.

13. The device of claim 12, wherein the residual substrate is thicker on the peripheral circuit region than on the cell array region.

14. The device of claim 1, wherein
the body conductive layer extends below the residual substrate, and the body conductive layer has a greater impurity concentration on the cell array region than on the peripheral circuit region.

15. The device of claim 1, wherein
the body conductive layer includes a first semiconductor layer and a second semiconductor layer,
the first semiconductor layer is adjacent to the plurality of vertical structures,
the second semiconductor layer is spaced apart from the plurality of vertical structures across the first semiconductor layer,
the first semiconductor layer has an impurity concentration greater than that of the second semiconductor layer.

16. The device of claim 1, wherein
the residual substrate extends onto the cell array region, the residual substrate contacts the body conductive layer on the cell array region, and
the residual substrate in contact with the body conductive layer on the cell array region includes an impurity region whose doping concentration is greater than that of the body

conductive layer.

17. The device of claim 1, further comprising:
an insulation pattern between the residual substrate and the body conductive layer,
wherein
the body conductive layer extends below the residual substrate.

18. The device of claim 17, wherein the body conductive layer has a stepwise structure between the cell array region and the peripheral circuit region.

19. A semiconductor memory device, comprising:
a cell array region connected to a peripheral circuit region,
the cell array region including a plurality of electrode structures including a plurality of electrodes sequentially stacked on a body conductive layer;
a plurality of vertical structures that penetrate the electrode structures and are connected to the body conductive layer; and
a common conductive line that extends between the electrode structures and is connected to the body conductive layer,
wherein the body conductive layer comprises a polycrystalline semiconductor material, and
wherein the cell array region and the peripheral circuit region are spaced apart from each other in a direction parallel with a top surface of the body conductive layer.

20. The device of claim 19, further comprising:
a residual substrate; and
a plurality of peripheral transistors on the residual substrate and spaced apart from the vertical structures.

21. The device of claim 19, wherein the cell array region and the peripheral circuit region are disposed along a top surface of the body conductive layer.