

Description

The present invention relates to a data write circuit connected to a nonvolatile memory cell transistor array which can prevent the possibility of data being erroneously written into a memory cell.

Data write circuit 20 as shown in Fig. 1 is conventionally used for a nonvolatile memory, such as an EPROM. That is, a plurality of floating gate type memory cell transistors MC have their drains connected to bit lines BL for memory cell array MA. Data write circuit 20 and data readout circuit 20 are connected to bit lines BL through bit line select transistor T_{BL} . Data write circuit 20 has one MOS transistor 22, such as an N-channel transistor, connected across a write voltage terminal V_{pp} and bit line BL via a bit line select transistor T_{BL} having a write signal line WE connected to the gate of transistor 22.

The operation of the nonvolatile memory cell transistor array is as follows.

Let it be assumed that a write operation is performed at a time of data "0". When a high voltage V_{pp} is applied to write signal line WE at a write time, write transistor 22 is turned ON. With transistor 22 in an "ON" state, a voltage on the bit line BL for a specific row connected to the bit line select transistor selected by the output of the column decoder becomes level V_{pp} . At this time, a voltage V_{pp} is applied to the word line WL on a specific column selected by the output of the row decoder, and hence the voltage V_{pp} is applied to the same column which is connected to the word line WL on the control gates of memory cell transistors MC. As a result, a voltage V_{pp} is applied across the drain D and control gate CG of a selected specific memory cell transistor MC as shown in Fig. 2, thereby causing a large current flow across the drain and the source S (grounded) of the same transistor. Hot electrons are drawn across the channel section and into a floating gate FG by voltage V_{pp} applied to the control gate CG. As a result, data "1" is written into the selected memory cell.

When the "1" data is written into the select memory cell, voltage V_{pp} is not applied to the write signal line WE, and write transistor 22 is turned OFF.

With write transistor 22 placed in a non-active (OFF) state, noise is adversely produced due to some effect on that V_{pp} voltage system and, if at this time the noise level exceeds level V_{pp} , a "punch-through" occurs in transistor 22 due to the application of a high voltage in excess of a withstand voltage to that transistor. As a result, a high voltage will be erroneously applied to each bit line which is connected as a load of write transistor 22. Let it be assumed that a voltage V_{pp} is applied to a

selected column in memory array MA of a memory cell array matrix. Even if, in this case, the memory cell transistors whose gates are connected to the "not selected" column may produce hot electrons into their floating gates when a high voltage on the bit line is applied to the drains of the memory cell transistors. Such an event, when occurring nearly once, produces no risk of data inversion. However, if such an event occurs several times repetitively, then data inversion may occur in the form of a "write" error.

In the case where, in the aforementioned EPROM, the memory cell transistor is used, for example, as some type of a flag, a "write error" resulting from the noise of the V_{pp} voltage prominently occurs due in part to a small transistor load, in particular of write transistor 22.

It is accordingly the object of the present invention to provide a nonvolatile memory which, even when noises occur in a write voltage system, can prevent a high voltage from being inadvertently supplied to the drain of a memory cell transistor via a data write circuit and hence can prevent a write error from occurring relative to the memory cell transistor.

To solve this object the present invention provides a nonvolatile memory as specified in claim 1.

A nonvolatile semiconductor memory of the present invention comprises bit lines connected to the drains of memory cell transistors, a data write circuit connected between the bit line and a write circuit and having at least two write MOS transistors connected in a serial manner, and a write-enable signal line commonly connected to the gates of the at least two write MOS transistors.

If noises are produced in the write voltage system, a punch-through effect is less likely to occur in the respective associated transistors, while the two transistors are connected in a serial manner. Even when the punch-through occurs in the respective associated transistors, a voltage to be applied to the bit line is lowered, thereby lowering the probability that a "write error" will occur in the memory cell transistors.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 shows a circuit arrangement in which a conventional data write circuit is connected to a non-volatile semiconductor memory cell transistor array;

Fig. 2 shows a model of the memory transistor as shown in Fig. 1; and

Fig. 3 shows a circuit arrangement in which a data write circuit of the present invention is connected to nonvolatile memory cell transistor array.

One embodiment of the present invention will be explained below with reference to the accompanying drawings.

Fig. 3 is a circuit arrangement in which a data write circuit of the present invention is connected to a nonvolatile memory cell transistor array. MA shows a memory cell transistor array having floating gate type memory cell transistors arranged in a matrix fashion. WL's show word lines for the memory cell transistor array, which are each connected to the respective gates of the memory cell transistors in the same column. TB's show bit line select transistors (MOS transistors) each connected in series with the respective bit lines. 10 and 21 are a data write circuit and a data readout circuit, respectively, which are each connected to the corresponding bit line via a corresponding bit line select transistor. WE shows a write-enable signal line.

In the present embodiment, data write circuit 10 includes at least two write transistors 11 and 12, for example, N-channel MOS transistors, connected in a serial manner with the gates of the write transistors connected in common with write-enable signal line WE. MOS transistor 13, for example, an N-channel MOS transistor, which is used for short-circuit switching is connected between a junction of the write transistors mentioned and a ground terminal. A signal on the write-enable line WE is supplied an an inverted signal to the gate of transistor 13 via an inverted circuit 14.

In the aforementioned circuit, with write data as "0", a write voltage V_{pp} is applied to write-enable signal WE, and write transistors 11 and 12 are turned ON. At this time, transistor 13 for short-circuit switching is turned OFF by the output ("0" level) of inverter circuit 14 and hence the voltage V_{pp} is supplied to the bit line side via write transistors 11 and 12. At this time, the voltage V_{pp} is applied to a specific bit line via select transistor T_{BL} selected by the output of the column decoder and to the word line for the specific column by an output of the row decoder. As a result, a specific memory cell transistor is selected and a voltage V_{pp} is applied to the drain and gate of the selected memory cell transistor to allow "0" data to be written therein.

With the write data as "1", a level of a signal on the write-enable signal line WE becomes "0" and write transistors 11 and 12 are turned OFF. At this time, transistor 13 for short-circuit switching is turned ON by the output of inverter circuit 14.

Let it be assumed that, when data write circuit 10 is in a non-active state, a noise voltage is generated on the V_{pp} voltage system for some effect or other and that, at this time, write transistor 11 on the V_{pp} voltage terminal side undergoes a "punch-through" upon receipt of a high voltage. Since, in this case, transistor 13 is turned ON, a

charge on the junction of transistors 11 and 12 is discharged to a ground terminal. Therefore, the other transistor 12 on the bit line side experiences no punch-through, thus preventing a high voltage from being unnecessarily supplied to the bit line side. As a result, it becomes possible to prevent a "write error" from occurring relative to the memory cell.

Although, in the aforementioned embodiment, transistor 13 for short-circuit switching is connected between the junction of write transistor group and a ground terminal to allow the "punch-through", if being produced, to be passed through a ground terminal short-circuit path, at least two write transistors may be connected in a serial manner, in place of using transistor 13, so that a bit line voltage at the time of a "punch-through" may be lowered, that is, the "write error" of the memory cell transistor may be prevented.

Claims

1. A nonvolatile memory comprising a plurality of memory cell transistors (MC) of a bit lines (BL) by word lines (WL) matrix array in which a write signal is supplied via a corresponding bit line (BL) to a memory cell transistor which is selected from among said plurality of memory cell transistors, said nonvolatile memory characterized by:
 - a data write circuit (10) having at least two write MOS transistors (11, 12) connected in series between said bit lines (BL) and a write-enable voltage terminal (V_{pp}), and
 - a write-enable signal line (WE) commonly connected to gates of said write MOS transistors (11, 12).
2. The nonvolatile memory according to claim 1, characterized in that said write circuit (10) has a MOS transistor (13) which is connected between a junction of said two series-connected MOS transistors (11, 12) and a ground terminal, for supplying a current to the ground terminal, and said MOS transistor is switchingly and complementarily controlled in accordance with a potential on said write-enable signal line (WE).
3. The nonvolatile memory according to claim 2, characterized in that a signal on said write-enable signal line is supplied as an inverted replica via an inverter (14) to a gate of said MOS transistor (13) connected to said ground terminal.

One embodiment of the present invention will be explained below with reference to the accompanying drawings.

Fig. 3 is a circuit arrangement in which a data write circuit of the present invention is connected to a nonvolatile memory cell transistor array. MA shows a memory cell transistor array having floating gate type memory cell transistors arranged in a matrix fashion. WL's show word lines for the memory cell transistor array, which are each connected to the respective gates of the memory cell transistors in the same column. TB's show bit line select transistors (MOS transistors) each connected in series with the respective bit lines. 10 and 21 are a data write circuit and a data readout circuit, respectively, which are each connected to the corresponding bit line via a corresponding bit line select transistor. WE shows a write-enable signal line.

In the present embodiment, data write circuit 10 includes at least two write transistors 11 and 12, for example, N-channel MOS transistors, connected in a serial manner with the gates of the write transistors connected in common with write-enable signal line WE. MOS transistor 13, for example, an N-channel MOS transistor, which is used for short-circuit switching is connected between a junction of the write transistors mentioned and a ground terminal. A signal on the write-enable line WE is supplied an an inverted signal to the gate of transistor 13 via an inverted circuit 14.

In the aforementioned circuit, with write data as "0", a write voltage V_{pp} is applied to write-enable signal WE, and write transistors 11 and 12 are turned ON. At this time, transistor 13 for short-circuit switching is turned OFF by the output ("0" level) of inverter circuit 14 and hence the voltage V_{pp} is supplied to the bit line side via write transistors 11 and 12. At this time, the voltage V_{pp} is applied to a specific bit line via select transistor T_{BL} selected by the output of the column decoder and to the word line for the specific column by an output of the row decoder. As a result, a specific memory cell transistor is selected and a voltage V_{pp} is applied to the drain and gate of the selected memory cell transistor to allow "0" data to be written therein.

With the write data as "1", a level of a signal on the write-enable signal line WE becomes "0" and write transistors 11 and 12 are turned OFF. At this time, transistor 13 for short-circuit switching is turned ON by the output of inverter circuit 14.

Let it be assumed that, when data write circuit 10 is in a non-active state, a noise voltage is generated on the V_{pp} voltage system for some effect or other and that, at this time, write transistor 11 on the V_{pp} voltage terminal side undergoes a "punch-through" upon receipt of a high voltage. Since, in this case, transistor 13 is turned ON, a

charge on the junction of transistors 11 and 12 is discharged to a ground terminal. Therefore, the other transistor 12 on the bit line side experiences no punch-through, thus preventing a high voltage from being unnecessarily supplied to the bit line side. As a result, it becomes possible to prevent a "write error" from occurring relative to the memory cell.

Although, in the aforementioned embodiment, transistor 13 for short-circuit switching is connected between the junction of write transistor group and a ground terminal to allow the "punch-through", if being produced, to be passed through a ground terminal short-circuit path, at least two write transistors may be connected in a serial manner, in place of using transistor 13, so that a bit line voltage at the time of a "punch-through" may be lowered, that is, the "write error" of the memory cell transistor may be prevented.

Claims

1. A nonvolatile memory comprising a plurality of memory cell transistors (MC) of a bit lines (BL) by word lines (WL) matrix array in which a write signal is supplied via a corresponding bit line (BL) to a memory cell transistor which is selected from among said plurality of memory cell transistors, said nonvolatile memory characterized by:
 - a data write circuit (10) having at least two write MOS transistors (11, 12) connected in series between said bit lines (BL) and a write-enable voltage terminal (V_{pp}), and
 - a write-enable signal line (WE) commonly connected to gates of said write MOS transistors (11, 12).
2. The nonvolatile memory according to claim 1, characterized in that said write circuit (10) has a MOS transistor (13) which is connected between a junction of said two series-connected MOS transistors (11, 12) and a ground terminal, for supplying a current to the ground terminal, and said MOS transistor is switchingly and complementarily controlled in accordance with a potential on said write-enable signal line (WE).
3. The nonvolatile memory according to claim 2, characterized in that a signal on said write-enable signal line is supplied as an inverted replica via an inverter (14) to a gate of said MOS transistor (13) connected to said ground terminal.



Patentansprüche

1. Nichtflüchtiger Speicher mit einer Vielzahl von Speicherzellentransistoren (MC) eines Bitleitungen (BL)-mal-Wortleitungen (WL)-Matrixarrays, in welchem ein Schreibsignal über eine entsprechende Bitleitung (BL) zu einem Speicherzellentransistor zugeführt wird, welcher aus einer Vielzahl von Speicherzellentransistoren ausgewählt wird, wobei der nichtflüchtige Speicher gekennzeichnet ist durch:

eine Datenschreibschaltung (10) mit mindestens zwei Schreib-MOS-Transistoren (11, 12), die in Serie zwischen den Bitleitungen (BL) und einem Schreibfreigabe-Spannungsanschluß (V_{pp}) verbunden sind, und

eine Schreibfreigabe-Signalleitung (WE) die gemeinschaftlich mit den Gates der Schreib-MOS-Transistoren (11, 12) verbunden ist.

2. Nichtflüchtiger Speicher nach Anspruch 1, dadurch gekennzeichnet, daß die Schreibschaltung (10) einen MOS-Transistor (13) besitzt, der zwischen einem Knoten der zwei serienverbundenen MOS-Transistoren (11, 12) und einem Masseanschluß zum Zuspiesen eines Stroms zum Masseanschluß verbunden ist, und daß der MOS-Transistor auf schaltende und komplementäre Weise entsprechend einem Potential auf der Schreibfreigabe-Signalleitung (WE) gesteuert wird.

3. Nichtflüchtiger Speicher nach Anspruch 2, dadurch gekennzeichnet, daß ein Signal auf der Schreibfreigabe-Signalleitung als eine invertierte Nachbildung über einen Invertierer (14) einem Gate des MOS-Transistors (13) zugeführt wird, der mit dem Masseanschluß verbunden ist.

(WE) connecté en commun aux grilles desdits transistors MOS d'écriture (11,12).

2. Mémoire rémanente selon la revendication 1, caractérisée en ce que ledit circuit d'écriture (10) comporte un transistor MOS (13) qui est connecté entre une jonction desdits deux transistors MOS (11,12) connectés en série et une borne de masse, pour fournir un courant à la borne de masse, et ledit transistor MOS est commandé par commutation et d'une façon complémentaire selon le potentiel présent sur ledit fil de signaux de validation d'écriture (WE).

3. Mémoire rémanente selon la revendication 2, caractérisée en ce qu'un signal présent sur ledit fil de signaux de validation d'écriture est fourni comme réplique inversée par un inverseur (14) à une grille dudit transistor MOS (13) connecté à ladite borne de masse.

Revendications

1. Mémoire rémanente comprenant une pluralité de transistors de cellules de mémoire (MC) d'un réseau matriciel de fils de bit (BL) et de fils de mot (WL) dans lequel un signal d'écriture est fourni par un fil de bit (BL) correspondant à un transistor de cellule de mémoire qui est sélectionné parmi ladite pluralité des transistors de cellules de mémoire, ladite mémoire rémanente étant caractérisée par:

un circuit d'écriture de données (10) comportant au moins deux transistors MOS d'écriture (11,12) connectés en série entre lesdits fils de bit (BL) et une borne de tension de validation d'écriture (V_{pp}), et

un fil de signaux de validation d'écriture

