A problem arises from the fact that such a circuit is not symmetrical. Indeed both branches may have different designs concerning dimensions of the respective transistors (T1 being compared to T4, and T2 being compared to T3). Moreover, the first and second nodes N1, N2 are operated in a different manner and with different loads (with nodes N1 and N2 being either both inputs or both outputs). Moreover, the operating points of all transistors may usually differ from each other during the sensing process (once again T1 is compared to T4, and T2 to T3). Thus for ensuring proper operation of the circuit, widths and lengths of the transistors must be thoroughly designed (and T1 and T4, respectively T2 and T3, may intentionally differ). Reference, bias and supply voltage must also be well defined and well controlled.

In practice however, all these parameters and the transistor properties (current drive capability, threshold voltage, transconductance, drain conductance, etc.) are prone to variations (PVT: process, voltage, temperature). As the single-ended sense amplifier is a non-symmetrical circuit, PVT induced variations do not compensate for each other in the two branches and malfunction of the circuit may result.

SUMMARY OF THE INVENTION

The invention aims to provide a single-ended sense amplifier which is not prone to PVT variations.

In this respect, the invention relates, according to its first aspect, to a semiconductor memory device comprising:

- a single-ended sense amplifier circuit for reading data sensed from selected memory cells in a memory array, the sense amplifier having a first node used to feed in a reference signal, a second node coupled to a bit line, and sense transistors responsible for amplifying the content of a selected memory cell during a sense operation,
- a reference circuit having replica transistors of the sense transistors and further comprising a regulation network designed ~~to operate~~so that each replica transistor operates in a stable operating point, and wherein the regulation network generates a control voltage which is applied to the sense amplifier circuit.

Other preferred, although non limitative, ~~aspects~~ embodiments of this memory device are as follows:

- the regulation network of the reference circuit is designed to set the operating point of each replica transistor equal to the operating point of the respective sense transistor at the onset of a sense operation of a selected memory cell performed by the sense amplifier circuit, said operating point at the onset of a sense operation being defined under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage

~~The~~ Embodiments of the invention further relate~~s~~ to a semiconductor memory incorporating a semiconductor memory device according to its first aspect, as well as to a process of operating a semiconductor memory device according to its first aspect comprising the steps of:

- operating each replica transistor in a stable operating point,
- generating a control voltage in the reference circuit and applying said control voltage to the sense amplifier circuit.
-

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, objects and advantages of the present invention will become better apparent upon reading the following detailed description of preferred embodiments thereof, given as a non-limiting example, and made with reference to the appended drawings wherein:

- Figure 1 already discussed above shows a single-ended sense amplifier as introduced in publication EP 2 365 487 A2;
- Figure 2 shows a first embodiment of a semiconductor memory device according to the invention comprising a single-ended sense amplifier together with a reference circuit for compensating the effect of PVT variations;
- Figure 3 shows a second embodiment of a semiconductor memory device according to the invention comprising a single-ended sense amplifier together with a reference circuit for compensating the effect of PVT variations;
- Figures 4 and 5 show possible layouts of a semiconductor memory device according to the invention comprising a single-ended sense amplifier together with a reference circuit for compensating the effect of PVT variations;
- Figures 6a and 6b show cascaded current mirrors that can be used in the semiconductor memory device of the invention;
- Figures 7a, 7b and 7c show simple operational amplifiers, or basic differential stages which can be used as very simple operational amplifiers, that can be used in the semiconductor memory device of the invention;
- Figure 8 shows another possible embodiment of a semiconductor memory device according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to a semiconductor memory device comprising a reference circuit and a plurality of single-ended sense amplifier circuits coupled to the reference circuit. Stated briefly, the reference circuit is designed and operated so as to generate a control signal fed to

CLAIMS

1. A semiconductor memory device comprising:

- a single-ended sense amplifier (SA) circuit for reading data sensed from selected memory cells in a memory array, the sense amplifier having a first node (N1) used to feed in a reference signal (REF), a second node (N2) coupled to a bit line (BL), and sense transistors (T2, T3) responsible for amplifying the content of a selected memory cell during a sense operation,

- a reference circuit (R) having replica transistors (T'2, T'3) of the sense transistors (T2, T3) and further comprising a regulation network (OP1, T'5; OP2) designed so that each replica transistor operates in a stable operating point, and wherein the regulation network generates a control voltage which is applied to the sense amplifier circuit.

2. The semiconductor memory device of claim 1, wherein the regulation network of the reference circuit is designed to set the operating point of each replica transistor equal to the operating point of the respective sense transistor at the onset of a sense operation of a selected memory cell performed by the sense amplifier circuit, said operating point at the onset of a sense operation being defined under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage which would be sensed on the bit line if a logical "1" were stored within the selected memory cell and the voltage which would be sensed on the bit line if a logical "0" were stored within the selected memory cell.

3. The semiconductor memory device of claim 1, wherein the control voltage generated by the regulation network is applied to one terminal (BG3') of a replica transistor (T'3) in the reference circuit and to the respective terminal (BG3) of the respective sense transistor (T3) in the sense amplifier circuit.

4. The semiconductor memory device of claim 1, wherein the sense amplifier circuit and the reference circuit each have first and second circuit branches, each of said branches having at least one first transistor of a first conductivity type and a second transistor of a second conductivity type (T2, T3; T'2, T'3) connected in series, wherein the second transistor (T2, T3) of each branch of the sense amplifier circuit is a sense transistor and wherein the second

transistor (T'2, T'3) of each branch of the reference circuit is a replica transistor of the second transistor of each branch of the sense amplifier.

5. The semiconductor memory device of claim 4, wherein the regulation network of the reference circuit comprises a first regulation loop (T'5, OP1) designed to maintain the drain voltage of the replica transistor (T'2) of the second branch in the reference circuit (R) at a voltage level corresponding to the voltage level on the data line (BL) at the onset of a sense operation under condition that the voltage sensed on the bit line at the onset of a sense operation corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.

6. The semiconductor memory device of claim 5, wherein the sense transistors and the replica transistors are double gate transistors having first and second control gates, and wherein the regulation network of the reference circuit comprises a second regulation loop (OP2) designed to drive the second control gate (BG3') of the replica transistor (T'3) of the first branch so that the current ratio between the replica transistor (T'3) of the first branch and the replica transistor (T'2) of the second branch is equal to the current ratio between the sense transistor (T3) of the first branch and the sense transistor (T3) of the second branch at the onset of a sense operation under condition that the voltage sensed on the bit line corresponds to the mean value between the voltage which would be sensed on the bit line from a logical "1" stored within the selected memory cell and the voltage which would be sensed on the bit line from a logical "0" stored within the selected memory cell.

7. The semiconductor memory device of claim 6, wherein the second regulation loop generates a control voltage which is applied to the second control gate (BG3') of the replica transistor (T'3) of the first branch of the reference circuit and to the second control gate (BG3) of the sense transistor (T3) of the second branch of the sense amplifier circuit.

8. The semiconductor memory device of any one of claims 4-7, wherein the at least one first transistors (T'1, T'4) of a first conductivity type in the branches of the reference circuit are arranged so as to form a current mirror.

9. The semiconductor memory device of any one of claims 4-8, wherein the replica transistors (T'2, T'3) have the same lengths as the corresponding sense transistors (T2, T3) and the same width ratio.

10. The semiconductor memory device of any one of claims 1-9 having a plurality of sense amplifier circuits arranged as stripes ~~(STSA)~~ of sense amplifier circuits.

11. A semiconductor memory comprising a semiconductor memory device according to any one of claims 1-10.

12. A process of operating a semiconductor memory device according to any one of claims 1-10, comprising the steps of:

- operating each replica transistor ~~(T'2, T'3)~~ in a stable operating point,
- generating a control voltage in the reference circuit and applying said control voltage to the sense amplifier circuit.