What is claimed is:

1. A memory device, comprising

a plurality of variable resistance memory cell pillars,

wherein adjacent memory cell pillars are separated by a partially filled gap that includes a buried void,

wherein the adjacent memory cell pillars include storage material elements that are at least partially interposed by the buried void, and

wherein the gap comprises an unfilled isolation gap above a seal region formed in the gap located above the buried void, and

wherein the gap comprises a first gap-seal dielectric extending in a first direction and a second gap-seal dielectric different from the first gap-seal dielectric extending in a second direction.

2. The memory device of claim **1**, wherein at least one of the storage material elements comprises a phase change material.

3. The memory device of claim **1**, wherein at least one of the first and second gap-seal dielectrics cover at least portions of opposing sidewalls of the adjacent memory cell pillars below the seal region.

4. The memory device of claim **3**, wherein a thickness of the at least one of the first and second gap-seal dielectrics covering the opposing sidewalls below the seal region continuously decreases away from the seal region.

5. The memory device of claim **3**, wherein the at least one of the first and second gap-seal dielectrics do not cover at least portions of the opposing sidewalls of the adjacent memory cell pillars below the seal region.

6. The memory device of claim **1**, wherein at least one of the first and second gap-seal dielectrics comprises silicon nitride.

7. A memory device, comprising

a plurality of variable resistance memory cell pillars,

wherein adjacent memory cell pillars are separated by a partially filled gap that includes a buried void,

wherein the adjacent memory cell pillars include storage material elements that are at least partially interposed by the buried void, the buried void spanning a height of the adjacent memory cell pillars in a first direction and at least partially spanning the height of the adjacent memory cell pillars in a second direction,

wherein a seal region is formed in the gap above the buried void and filled with a gap-seal dielectric,

wherein the gap further includes an unfilled isolation gap above the seal region,

wherein the gap comprises a first gap-seal dielectric extending in a first direction and a second gap-seal dielectric different from the first gap-seal dielectric extending in a second direction.

8. The memory device of claim 1, wherein opposing sidewalls of the adjacent memory cell pillars are lined with liner dielectric materials in contact with the opposing sidewalls.

9. The memory device of claim 1, wherein each of the plurality of variable resistance memory cell pillars is surrounded by the buried void.

10. A memory device, comprising:

a plurality of memory cell stacks,

wherein each memory cell stack comprises a storage element comprising a phase change material,

wherein adjacent memory cell stacks are separated by a gap which includes an enclosed void,

wherein a seal region is formed in the gap above the enclosed void and filled with a gap-seal dielectric,

wherein the gap further includes an unfilled isolation gap above the seal region, and

wherein each of the memory cell stacks is surrounded by the enclosed void and a height of the enclosed void extending in a first lateral direction is different from the height of the enclosed void extending in a second lateral direction.

11. The memory device of claim **10**, wherein each memory cell stack comprises upper and lower active elements, wherein one of the upper and lower active elements comprises the storage element and the other of the upper and lower active elements comprises a selector element.

12. The memory device of claim **11**, wherein the upper active element comprises the storage element, and the upper active elements of the adjacent memory cell stacks are at least partially interposed by the enclosed void.

13. The memory device of claim **12**, wherein the lower active elements of the adjacent memory cell stacks are at least partially interposed by the enclosed void.

14. The memory device of claim **11**, wherein each memory cell stack further comprises an upper electrode formed on the upper active element, wherein the enclosed void does not extend above a top surface of the upper electrode.

15. The memory device of claim **11**, wherein each memory cell stack is formed between an upper conductive line and a crossing lower conductive line, and wherein each memory cell stack further comprises an upper electrode formed on the upper active element, wherein the enclosed void does not extend above a top surface of the upper conductive line.

16. A memory device, comprising:

an array of memory pillars arranged in a plurality of rows of pillars aligned in a first lateral direction and a plurality of columns of pillars aligned in a second lateral direction crossing the first lateral direction,

wherein each memory pillar comprises a storage element comprising a phase change material,

wherein at least two adjacent memory pillars are separated by a gap comprising a gap-seal dielectric extending in the first lateral direction and a different gap-seal dielectric extending in the second lateral direction,

wherein adjacent rows of pillars and adjacent columns of pillars are separated by continuous buried voids extending in the respective first and second lateral directions of the rows of pillars and columns of pillars,

where the gap comprises an unfilled isolation gap above a seal region formed in the gap located above the buried voids.

17. The memory device of claim **16**, wherein the continuous buried voids extending in the first lateral direction and the continuous buried voids extending in the second lateral direction intersect each other such that each memory pillar is surrounded by a continuous buried void.

18. The memory device of claim **17**, wherein the continuous buried void surrounds the storage element.

19. A method of forming a memory device, comprising:

forming a plurality of variable resistance memory cell pillars, wherein each memory cell pillar includes a storage element;

forming a buried void that surrounds storage material elements of at least two adjacent memory cell pillars by partially filling a gap between the at least two adjacent memory cell pillars with a gap-seal dielectric,

wherein the buried void spans a height of the at least two adjacent memory cell pillars in a first direction and partially spans the height of the at least two adjacent memory cell pillars in a second direction, and

wherein the gap comprises an unfilled isolation gap above a seal region formed in the gap located above the buried void.

20. The method of claim **19**, wherein forming the memory cell pillars includes:

forming a plurality of memory cell line stacks extending in the first direction, wherein each memory cell line stack includes a storage material line; and

separating the memory cell line stacks in the first direction to form the memory cell pillars.

21. The method of claim **20**, wherein forming the buried void comprises:

after forming the plurality of memory cell line stacks, partially filling the gap between adjacent memory cell line stacks with the gap-seal dielectric to form the buried void that forms a continuous buried void extending in the first direction.

22. The method of claim **19**, wherein forming the memory cell pillars includes forming the storage material elements to include a phase change material.

23. The method of claim **19**, wherein forming the buried void comprises forming a seal region in the gap above the buried void and filling the seal region with the gap-seal dielectric.

24. The method of claim **19**, wherein partially filling includes covering at least portions of opposing sidewalls of the at least two adjacent memory cell pillars below the seal region with the gap-seal dielectric.

25. The method of claim **24**, wherein partially filling includes not covering at least portions of opposing sidewalls of the at least two adjacent memory cell pillars below the seal region with the gap-seal dielectric.

26. The method of claim **19**, wherein partially filling the gap comprises partially filling with silicon nitride.

27. A method of forming a memory device, comprising:

forming a plurality of variable resistance memory cell pillars, wherein each memory cell pillar includes a storage element;

forming a buried void that interposes storage material elements of at least two adjacent ones of the memory cell pillars by partially filling a gap between adjacent memory cell pillars with a gap-seal dielectric, wherein a seal region is formed in the gap above the buried void and filled with a first gap-seal dielectric extending in a first direction and a second gap-seal dielectric different from the first gap-seal dielectric extending in a second direction; and

forming an unfilled isolation gap above the seal region.

28. The method of claim **19**, further comprising lining opposing sidewalls of the adjacent memory cell pillars with liner dielectric materials prior to forming the buried void.

29. The method of claim **19**, wherein forming the buried void includes surrounding each of the variable resistance memory cell pillars.