METHODS OF ETCHING INTO SILICON OXIDE-CONTAINING MATERIAL, METHODS OF FORMING CONTAINER CAPACITORS, AND METHODS OF FORMING DRAM ARRAYS

TECHNICAL FIELD

[0001] Methods of etching into silicon oxide-containing material, methods of forming container capacitors, and methods of forming DRAM arrays.

BACKGROUND

[0002] Semiconductor processing may frequently include an etch into or through silicon oxide-containing material. The silicon oxide-containing material may be undoped (and thus may consist of silicon dioxide (SiO_2)), or may be doped (and thus may comprise, for example, one or more of borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), and fluorosilicate glass (FSG)).

[0003] An example application in which silicon oxide-containing material is etched is the formation of capacitor container openings. Figs. 1-3 illustrate a conventional method for forming capacitor container openings within silicon oxide-containing material.

[0004] Referring to Fig. 1, such shows a semiconductor construction 10 at a preliminary processing stage. Construction 10 comprises a base semiconductor material 12 having a plurality of transistors 14, 16 and 18 supported thereby. The base semiconductor material may comprise any suitable semiconductor composition or combination of compositions; and may, for example, comprise, consist essentially of, or consist of monocrystalline silicon lightly background doped with appropriate dopant. The base may be a portion of a monocrystalline silicon wafer.

[0005] The base 12 may be considered to be a semiconductor substrate, or a portion of a semiconductor substrate. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0006] Transistors 14, 16 and 18 comprise gates 24, 26 and 28, respectively. Such gates include stacks comprising gate dielectric 30, electrically conductive gate material 32, and an electrically insulative cap 34. The electrically conductive gate material may

comprise one or more of metal (such as titanium or tungsten), metal compounds (for instance, metal silicide or metal nitride), and conductively-doped semiconductor material (for instance, conductively-doped silicon). The gate dielectric may comprise silicon dioxide. The insulative caps may comprise one or more of silicon nitride, silicon dioxide and silicon oxynitride.

[0007] Electrically insulative sidewall spacers 36 are along sidewalls of the gates. Such sidewall spacers may one or more of silicon dioxide, silicon nitride and silicon oxynitride.

[0008] Transistors 14, 16 and 18 comprise source/drain regions 40, 42, 44, 46 and 48. Transistors 14 and 16 are paired, and share a common source/drain region 42. Transistor 18 may be part of another paired transistor set, so that source/drain region 48 is also a shared source/drain region. Source/drain regions 44 and 46 are electrically isolated from one another by an isolation region 45 provided between them. The isolation region is filled with insulative material, such as, for example, one or both of silicon dioxide and silicon nitride; and may correspond to a shallow trench isolation region.

[0009] Ultimately, shared source/drain regions 42 and 48 may be connected to bitlines, and the remaining source/drain regions 40, 44 and 46 may be connected to capacitors. Accordingly, transistors 14, 16 and 18 may be incorporated into a dynamic random access memory (DRAM) array.

[0010] A silicon oxide-containing material 50 is over transistors 14, 16 and 18. The silicon oxide-containing material may comprise a single homogeneous mass as shown, or may comprise multiple layers. A majority of the silicon oxide-containing material may consist of one or more of doped oxides, such as BPSG, PSG or FSG; and in some applications an entirety of the silicon oxide-containing material 50 may consist of one or more doped oxides. In some applications, at least a portion of silicon oxide oxide-containing material 50 may consist of silicon dioxide. For instance, a lower portion of silicon oxide-containing material 50 may be a layer of silicon dioxide, and the remainder of silicon oxide-containing material 50 may be one or more doped oxides.

[0011] A patterned mask 52 is formed over material 50. The patterned mask has a plurality of openings 54, 56 and 58 extending therethrough. The patterned mask may comprise, consist essentially of, or consist of carbon-containing material, such as transparent carbon, amorphous carbon and/or photoresist.

[0012] Referring to Fig. 2, openings 54, 56 and 58 are extended through silicon oxide-containing material 50 to source/drain regions 40, 44 and 46, respectively. The openings may be extended through the silicon oxide-containing material with an etch

utilizing C_4F_8 (flowed at about 60 standard cubic centimeters per minute (sccm)), argon (flowed at about 1100 sccm), oxygen (flowed at about 25 sccm) and C_4F_6 (flowed at about 2 sccm). Such etch may be conducted under a pressure of about 30 millitorr, utilizing a plasma power of about 2100 watts at about 60 megahertz, and a substrate bias of about 3500 watts at about 2 megahertz.

[0013] A problem with an etch as described above is that it may create the shown bowing within openings 56 and 58, which creates widened regions 60 and 62. Such widened regions thin a sidewall between them so that openings 56 and 68 touch or nearly touch at a location 63. Also, the etch may lead to so-called "twisting" within the openings such that the internal periphery of the openings appears to twist along the vertical length of the openings.

[0014] Referring to Fig. 3, masking material 52 (Fig. 2) is removed and capacitor materials 70, 72 and 74 are formed within the openings 54, 56 and 58. Capacitor material 70 is a first electrode material, capacitor material 72 is a dielectric material, and capacitor material 74 is a second electrode material. Materials 70 and 74 are electrically conductive, and may comprise one or more of metal, metal compounds, and conductively-doped semiconductor materials. Material 72 is electrically insulative, and may comprise one or more of silicon dioxide, silicon nitride, and various high-k materials.

[0015] Materials 70, 72 and 74 are intended to form capacitor constructions 80, 82 and 84 within openings 54, 56 and 58. Unfortunately, the bowing within openings 56 and 58 may cause capacitors 82 and 84 to be shorted to one another.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Figs. 1-3 illustrate semiconductor wafer fragments at various conventional processing stages for forming capacitors of a DRAM array.

[0017] Figs. 4-7 illustrate semiconductor wafer fragments at various processing stages in accordance with an embodiment of the invention for forming openings through a silicon oxide-containing material, and for forming capacitors within such openings.

[0018] Fig. 8 diagrammatically illustrates a portion of an etching chamber which may be utilized in an embodiment of the invention.

DETAILED DESCRIPTION

[0019] Embodiments of the invention may utilize new etching chemistries to avoid bowing and other problems associated with formation of high aspect ratio openings using conventional processing. Openings formed with such new etching chemistries

may be utilized for fabrication of container capacitors, and such capacitors may be incorporated into DRAM.

[0020] Figs. 4-7 illustrate an embodiment of the invention. In referring to Figs. 4-7, similar numbering will be used as was utilized in describing the conventional process of Figs. 1-3, where appropriate.

[0021] Referring initially to Fig. 4, such shows a semiconductor construction 10 similar to that discussed above with reference to Fig. 1. The construction 10 of Fig. 4 comprises the semiconductor base 12, transistors 14, 16 and 18, isolation region 45, silicon oxide-containing material 50, and patterned masking material 52 discussed above with reference to Fig. 1.

[0022] Gaps (or openings) 54, 56 and 58 extend through patterned masking material 52. A difference between the construction of Fig. 4 and that of Fig. 1 may be that gaps 54, 56 and 58 have different dimensions in Fig. 4 than in Fig. 1. Such difference in dimensions may be used to optimize the construction of Fig. 4 for different etching conditions than the conventional conditions utilized to treat the construction of Fig. 1.

[0023] Referring to Fig. 5, construction 10 is subjected to an etch which extends openings 54, 56 and 58 through silicon oxide-containing material to source/drain regions 40, 44 and 46, respectively. The etch forms the openings within silicon oxide-containing material 50 to be more tapered than the openings formed by the conventional etching conditions (the openings of Fig. 2), and also avoids problems associated with bowing and twisting. In some embodiments, bowing and twisting may be eliminated. Even if the bowing and twisting are not eliminated, the tapering of the openings may create additional spacing between the openings as the openings penetrate deeper into silicon oxide-containing material 50, which may avoid overlap of adjacent openings. In some embodiments, etching conditions may be chosen such that the tapering is lessened relative to that shown in Fig. 5; and in some embodiments the etching conditions may form sidewalls that are about as vertical as those formed by conventional processes.

[0024] The etch utilized to extend openings 54, 56 and 58 through silicon oxide-containing material 50 may be a plasma etch utilizing a high concentration of helium. A plasma etch may have a chemical-based part and a physical-based part. The chemical-based part of the etch is due to chemical interaction of etching components with material to cause a reaction which removes the material. The physical-based part of the etch is due to impact of energetic etch components into the material to displace portions the material (in some ways analogous to sand-blasting). Helium is a lighter element than the argon utilized in the conventional processing of Figs. 1-3, and this may cause the

physical etch component associate with helium to be less than that associated with argon.

[0025] The etching may be conducted in an etching chamber, such as the chamber 200 diagrammatically illustrated in Fig. 8. Such chamber has a substrate holder 202 provided therein which retains a semiconductor substrate 10. The chamber has a region above the substrate within which a plasma 204 is maintained. Etching components are flowed into the chamber as diagrammatically illustrated by arrow 206, and products and unreacted etching components are flowed out of the chamber as diagrammatically illustrated by arrow 208. There may be a flow of materials through an etching chamber during an etching process. The materials within the etching chamber during the etching process may be referred to as an etching ambient. The materials within the etching chamber may be in a gas or plasma state, and accordingly may be referred to as an etching fluid.

[0026] The etching ambient utilized during the etch through silicon oxide-containing material 50 of Fig. 5 may comprise at least about 75 volume percent helium. Additionally, the etching ambient may comprise O_2 and one or more fluorocarbons; with the fluorocarbons and O_2 being utilized for a chemical-based part of the etch. The fluorocarbons may include C_4F_8 and C_4F_6.

[0027] If the etching ambient comprises only helium, fluorocarbons and O_2, it is found that there may be poor selectivity of the etch for silicon oxide-containing material relative to masking material 52. This may be due to fluorine being released during the etching process and attacking the masking material. It is also found that inclusion of CO (carbon monoxide) within the etching ambient may improve the selectivity of the etch for the silicon oxide-containing material relative to the masking material. Such may be due to the CO scavenging released fluorine. Utilization of CO may be particularly useful in applications in which masking material 52 comprises carbon, such as when masking material 52 consists essentially of, or consists of amorphous carbon or transparent carbon. The CO may be provided within the etching ambient to a concentration of at least about 5 volume percent.

[0028] An embodiment of the etch utilized to etch through silicon oxide-containing material 50 utilizes flow of the following through a reaction chamber:

from about 6 sccm to about 100 sccm of one or more fluorocarbons (which may be about 60 sccm C_4F_8 and about 2 sccm C_4F_6);

from about 100 sccm to about 1500 sccm of helium (which may be about 1000 sccm He);

from about 1 sccm to about 500 sccm of CO (which may be about 300 sccm CO); and

from about 2 sccm to about 40 sccm of O_2 (which may be about 25 sccm O_2).

[0029] The etch may be conducted with a pressure of the ambient (in other words, a pressure within the reaction chamber) of from about 10 millitorr to about 30 millitorr (for instance, about 30 millitorr); a plasma power of from about 1500 watts to about 3000 watts, (for instance, about 2100 watts); and a substrate bias of from about 2000 watts to about 5000 watts, (for instance, about 3500 watts).

[0030] In some embodiments, the etching ambient may consist essentially of helium, one or more fluorocarbons, CO and O_2 for at least a portion of an etch. The helium, one or more fluorocarbons, CO and O_2 are the materials flowed into the chamber during the etch, but the composition of the etching ambient may change as products are released during the etching process. In some embodiments, the helium, one or more fluorocarbons, CO and O_2 are the only materials flowed into the chamber; and accordingly the etching materials flowed in the chamber may be considered to consist of the helium, one or more fluorocarbons, CO and O_2.

[0031] The silicon oxide-containing material 50 may, as discussed above with reference to Fig. 1, comprise doped silicon oxide-containing material (such as BPSG, PSG or FSG) and/or undoped silicon dioxide. In some embodiments, material 50 may consist of doped silicon oxide-containing material, and in other embodiments material 50 may consist of SiO_2. In yet other embodiments, material 50 may comprise a thick mass of doped silicon oxide-containing material over a layer consisting of SiO_2.

[0032] Although the etch of Fig. 5 is shown extending all the way to the source/drain regions, it is to be understood that in other embodiments conductive pedestals could be formed over the source/drain regions, and the etch could then be conducted to extend to upper surfaces of such conductive pedestals.

[0033] The openings formed within silicon oxide-containing material 50 may be high aspect ratio openings, and accordingly may have aspect ratios of at least 20:1, and in some embodiments may have aspect ratios of 24:1 or higher.

[0034] Referring to Fig. 6, masking material 52 is removed. Such removal may be accomplished with any suitable etch, or combination of etches, and may for example be accomplished with a dry strip process, such as a strip utilizing O_2.

[0035] Referring to Fig. 7, the openings 54, 56 and 58 are utilized as containers of container capacitors. Specifically, first capacitor electrode material 70, dielectric material 72 and second capacitor electrode material 74 are formed within the openings to form container capacitors 80, 82 and 84. Such container capacitors are directly over

source/drain regions 40, 44 and 46, respectively. In some embodiments, silicon oxide-containing material 50 may be at least about 1 micron thick, and accordingly the containers of the container capacitors may be at least about 1 micron deep. Accordingly, tall, thin capacitors may be formed within the high aspect ratio openings 54, 56 and 58. The problem of adjacent capacitors shorting to another may be avoided utilizing the etching conditions discussed above with reference to Fig. 5.

[0036] Capacitors 80, 82 and 84 may be incorporated into a DRAM array. Specifically, shared source/drain regions 42 and 48 may be connected to bitlines 100 and 102 (diagrammatically illustrated in Fig. 7), and transistor gates 24, 26 and 28 may be comprised by wordlines. Each of the individual transistors 14, 16 and 18 may be considered to comprise paired source/drain regions (for instance, transistor 14 comprises paired source/drain regions 40 and 42). Further, each of the individual transistors has one of the paired source/drain regions electrically coupled with a capacitor (for instance, capacitor 80 is electrically coupled with source/drain region 40), and has the other of the paired source/drain regions electrically coupled with a bitline (for instance, source/drain region 42 is electrically coupled with bitline 100).

CLAIMS

Claim 1. A method of forming a DRAM array, comprising:

providing a semiconductor construction within an etching chamber, the semiconductor construction comprising a plurality of transistors over a semiconductor substrate; individual of the transistors comprising paired source/drain regions;

forming silicon oxide-containing material over the transistors;

forming a patterned carbon-containing mask over the silicon oxide-containing material; the patterned carbon-containing mask having a plurality of openings extending therethrough; the patterned carbon-containing mask comprising transparent carbon;

flowing etching materials into the chamber, the etching materials consisting of helium, carbon monoxide, one or more fluorocarbons, and O_2;

utilizing the etching materials to extend the openings into the silicon oxide-containing material to form containers in the silicon oxide-containing material having aspect ratios of at least about 20:1; the containers being directly over source/drain regions of the transistors;

forming first capacitor electrode material within the openings;

forming dielectric material within the openings and over the first capacitor electrode material;

forming second capacitor electrode material within the openings and over the dielectric material; the first and second capacitor electrode materials, together with

the dielectric material, forming a plurality of capacitors within the plurality of the openings; individual capacitors being electrically coupled with the individual source/drain regions of the transistors; and

forming bitlines in electrical connection with source/drain regions of the transistors; individual transistors having one source/drain region of the paired source/drain regions electrically coupled with a bitline of the plurality of bitlines, and having the other source/drain region of the paired source/drain regions electrically coupled with a capacitor of the plurality of capacitors.

Claim 2. The method of claim 1 wherein the silicon oxide-containing material comprises doped silicon oxide.

Claim 3. The method of claim 1 wherein the silicon oxide-containing material consists of doped silicon oxide.

Claim 4. The method of claim 1 wherein the flowing of the etching materials into the chamber comprises flow rates of:

from about 6 sccm to about 100 sccm of the one or more fluorocarbons;

from about 100 sccm to about 1500 sccm of the helium; and

from about 1 sccm to about 500 sccm of the carbon monoxide.

Claim 5. The method of claim 4 further comprising providing the O_2 at a flow rate of from about 2 sccm to about 40 sccm.

Claim 6. The method of claim 1 further comprising formulating the one or more fluorocarbons to consist of C_4F_8 and C_4F_6.