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DEVICES WITH GROUP IV ELEMENT-DOPED GROUP III-V COMPOUND SEMICONDUCTORS

Field of the Invention

This invention concerns devices having Group IV element-doped Group
5 III-V compound semiconductors.

Background of the Invention

Group III-V compound semiconductors are desirable materials in high-speed electronic and opto-electronic semiconductor devices such as lasers, amplifiers, light-emitting diodes, and photodetectors. These materials are being
10 included in devices in which layers may be intrinsic, p-type or n-type conductivity. Of special interest are such Group III-V compound semiconductors as (GaIn)As, (AlIn)As, (AlGaIn)As, (GaInP), (AlInP) and (AlGaInP). In these materials, dopants such as Be, Zn and C are often used to obtain p-type conductivity, and Si, Ge and Sn to obtain n-type conductivity. However, at higher doping levels $1 \times 10^{19} \text{ cm}^{-3}$, many
15 of these dopants have a tendency to diffuse and surface segregate, therefore precluding well-controlled incorporation of these dopants into Group III-V compound semiconductors, while carbon tends toward formation of compensated materials. Japanese Laid-Open Patent application No. 4-5817 discloses the use of Group IV elements, especially carbon, as a p-type dopant in a $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$
20 structure, lattice-matched to an InP substrate, by means of a multiperiod superlattice in which each period included a C-doped layer of GaAs (8 monolayers thick), an undoped $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ layer (0.7 monolayers thick), an undoped InAs layer (10.6 monolayers thick) and an undoped $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ layer (0.7 monolayers thick). The GaAs layers were homogeneously doped with carbon. The n-type doping of
25 InAs region was obtained with Si in a conventional manner. However, while the Japanese application teaches p-doping of $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ superlattice, doping of $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ by an amphoteric dopant to achieve both p- and n-type conductivity in different regions of the superlattice is still not available. Therefore, it would be desirable to form either p- or n- type conductivity or both in III-V compound
30 semiconductor devices using a single, amphoteric dopant which would have low diffusion coefficient, and have opposite conductivity type in different portions of the ternary alloy.

Summary of the Invention

This invention embodies devices comprising Group III-V compound
35 semiconductors in which p or n or both p and n regions are formed by a superlattice selectively doped with an amphoteric Group IV element dopant such as carbon,



- germanium and silicon. The superlattice includes a plurality of periods, each including two layers. Depending on the conductivity type, only one of the layers in the periods forming the superlattice region of said type of conductivity is selectively doped with said dopant, leaving the other layer in these periods undoped. The
- 5 superlattice can be formed by Molecular Beam Epitaxy technique, and the dopant is incorporated into respective layers by delta-doping as a sheet centrally deposited between monolayers forming the respective layers of the period. Each period preferably includes 5 to 15 monolayers deposited in the two layers in a numerical ratio corresponding to a cation compositional ratio in the compound semiconductor.
- 10 Low growth temperatures, e.g. ranging from 410 to 450°C lead to mirror-like surfaces. For example, for a compound semiconductor $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$, GaAs/InAs ordered superlattices with eight monolayers per period are grown in a ratio of 0.47/0.53. At free carrier concentrations of 10^{16}cm^{-3} , carrier mobilities of 200 and 2300 cm^2/Vs for p-type and n-type are obtained with carbon as the amphoteric
- 15 dopant.

Brief Description of the Drawings

FIG. 1 is a schematic diagram of a device with a GaAs/InAs superlattice which is selectively δ -doped in the center of the InAs and GaAs layers;

- FIG. 2 is a schematic diagram of a portion of the superlattice shown in
- 20 FIG. 1 including p-n junction and two periods of the superlattice each of different type of conductivity on opposite sides of the p-n junction;

FIGS. 3 and 4 are each a schematic diagram of two versions of a device with a p-n junction in which the superlattice forms a region with one type of conductivity; and

- 25 FIG. 5 is a current-voltage characteristic of the GaAs/InAs superlattice p-n junction on an InP substrate.

Detailed Description

- In FIGS. 1 and 2 is shown an exemplary embodiment of Group III-V semiconductor device. For reasons of clarity, the elements of the device are not
- 30 shown to scale. The device, 10, includes semiconductor structure with a substrate, 11, a buffer layer, 12, a region, 13, having p-type (or n-type) conductivity, a region, 14, having an n-type (or p-type) conductivity, respectively, regions 13 and 14 forming p-n (or n-p) junction 15, a conductive contact layer, 16, and electrical contacts 17 and 18 to the structure. In this device the p-n junction 15 is formed by a
- 35 superlattice structure, 19, including a plurality of periods, 20, forming a p- (or n-) and n- (or p-, respectively) type conductivity doped regions 13 and 14. Each period



20 consists of a layer, 21, of one binary semiconductor, e.g., InAs (or InP), and a layer, 22, of another binary semiconductor, e.g., GaAs or AlAs or (AlGa)As [or GaP or AlP, or AlGa)P, respectively]. The layers in each period include a plurality of monolayers, respectively. In each period, a certain number of monolayers of the one
5 semiconductor, e.g., InAs, add up to one layer, e.g., layer 21, and another number of monolayers of the other semiconductor, e.g., GaAs, AlAs or AlGaAs, add up to the second layer, e.g., layer 22. The monolayers in the two layers of each period are present in substantially the same numerical ratio as the cation compositional fraction of each respective binary semiconductor in the lattice-matched ternary or quaternary
10 Group III-V compound semiconductor. Strained layers may also be grown in the same manner.

Carbon (C) has been recognized as an amphoteric dopant material in Group III-V compound semiconductors having small ionization energy, high solid solubility, and an extremely low diffusion in AlAs and GaAs. Carbon diffusivity in
15 III-V compound semiconductors is several orders of magnitude lower than other typical dopants such as Be or Zn. Carbon acts in GaAs or AlAs as a p-type dopant, in InAs as an n-type dopant, and is strongly amphoteric in a $\text{Ga}_x\text{In}_{1-x}\text{As}$ alloy, wherein $x = 0.47 \pm 0.05$, leading to compensated material. As a result of the amphoteric nature of C, good doping characteristics cannot be achieved with C in
20 this material. However, we have found that it is possible to use carbon as the sole doping source for either p- or n-type doping of these alloys.

In the specific exemplary embodiment, p-n junctions were grown using $(\text{GaAs})_{3.76}/(\text{InAs})_{4.24}$ superlattice for the p-type region and the n-type region. The device includes n^+ -InP substrate 11, Si-doped n^+ -type $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ buffer
25 layer 12, C-doped $(2 \times 10^{16} \text{ cm}^{-3})$ n-type superlattice region 13, C-doped $(2 \times 10^{16} \text{ cm}^{-3})$ p-type superlattice region 14, and p^+ -type $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ contact layer 16. Circular AuBe ($\phi = 500 \mu\text{m}$) metallization, annealed at 380°C for 25 sec., is used as the top ohmic contact 17. Alloyed In metallization 18 to substrate 11 completes the device.

30 The device was produced by growing superlattice 19 upon an InP substrate by MBE technique. Monolayers were grown by MBE in a preselected sequence, such as to deposit a first plurality of monolayers of one compound, e.g., InAs, followed by a second plurality of monolayers of another compound, e.g., GaAs, the two pluralities of monolayers making up the respective layers 21 and 22,
35 respectively, which, in turn, make up periods 20 of the superlattice. The superlattice includes from 10 to 500 or more, preferably from 100 to 300 periods. Carbon as a



dopant is introduced into the center of one layer, e.g. 21, or of another layer, e.g. 22, in each of the periods, depending on the desired conductivity type (p or n) of the superlattice region. Carbon when introduced as a sheet of dopant between the central monolayers of one binary composition shall lead to one type of conductivity, and, when introduced between the central monolayers of another binary composition, shall lead to the opposite type of conductivity. Care should be taken to avoid introduction of carbon into layers of both of the binary compositions, e.g., (InAs and GaAs) of the period, or into monolayers of one binary composition (e.g., InAs or GaAs) adjacent to or interfacing with the carbon-doped monolayers of another binary composition (e.g., GaAs or InAs, respectively). In such instances carbon deposition shall result in compensated regions of ternary composition composed of the adjacent layers of the two binary composition.

Instead of carbon, other amphoteric dopants of Group IV elements, Ge or Si, may be used for obtaining p-type and n-type conductivities. As with carbon, care should be taken to keep the dopant sheets well within the confines of the respective, e.g., GaAs and InAs, layers, so as to avoid diffusion of the dopant into the adjacent, undoped layer. This should assure separate conductivity types and avoid compensation of the compound semiconductor material.

Each period may include from 5 to 15 monolayers of the two compound semiconductors (e.g., GaAs and InAs) forming the ternary or quaternary composition (e.g. $\text{Ga}_x\text{In}_{1-x}\text{As}$ wherein $x = 0.47 \pm 0.05$). The monolayers in each period are present in a numerical ratio corresponding to the cation compositional ratio in the ternary composition. The monolayers are grown by MBE on substrates kept at a temperature ranging from 410 to 450°C. The temperature is selected to result in smooth, mirror-like surfaces. The cation composition ratio is selected such that the epitaxial layers are lattice matched. Thus, the average composition of the epitaxial layer has such a value that the lattice of the epitaxial layer coincides with the lattice of the substrate on which the superlattice is grown.

For a specific exemplary composition of $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$, each period consists of 8 monolayers arranged as 3.76 monolayers of GaAs and 4.26 monolayers of InAs, that is in a ratio of 0.47 to 0.53. Introduction of carbon as a carbon-dopant sheet into InAs layers only, and retention of GaAs as an undoped material, results in an n-type conductivity $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ region shown in FIGS. 1 and 2. Introduction of carbon as a carbon-dopant sheet into the GaAs layers only, results in a p-type conductivity $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ region shown in FIGS. 1 and 2.



The epitaxial layers were grown by MBE on n^+ -type (S doped) (100)-oriented InP substrates; however, they may be grown on semi-insulating (Fe doped) (100)-oriented InP substrates or p^+ -type (Zn doped) (100)-oriented substrates, as well. The growth system was an Intevac Gen II system. The growth rate for $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ is $1.0 \mu\text{m/hr}$ and for the two constituents, GaAs and InAs, approximately $0.5 \mu\text{m/hr}$ each. Growth rate and alloy composition are calibrated using reflection high-energy electron diffraction (RHEED) oscillations. The epitaxial layers discussed here are ordered $(\text{GaAs})_m/(\text{InAs})_n$ superlattices with $m/n = 0.47/0.53$ which are lattice-matched to the InP substrate. The period of the superlattice is 8 molecular layers, with the GaAs and InAs layers, 22 and 21, including 3.76 and 4.24 monolayers, respectively. Epitaxial growth at 430°C , near the InAs congruent sublimation temperature (435°C), resulted in mirror-like epitaxial layer surfaces. At higher growth temperatures, the surface morphology of the superlattices became progressively rougher. The surface roughness was assessed by optical phase-contrast (Nomarski) microscopy. The roughness is most likely related to the strain inherent to the superlattice material system. Although the system is macroscopically lattice matched, the microscopic strain in each of the binary layers favors three-dimensional island growth over layer-by-layer growth. This effect of strain can be reduced by a lower growth temperature.

The epitaxial layers were δ -doped in the center of the InAs and GaAs layers, depending on the desired conductivity type of the superlattice region. The C impurities were evaporated onto the semiconductor surface during growth interruption achieved by closing the Group-III shutter of the respective (In or Ga) effusion cell while the Group V (As) shutter remained open. Therefore, an As-stabilized surface reconstruction was maintained during the δ -doping process. The interruption took place in the center of the respective GaAs and InAs layers. It is the purpose of the δ -function-like doping profiles to keep the C dopants confined to within the InAs or GaAs layers 21 and 22, respectively.

The epitaxial layers were evaluated at room temperature using Hall measurements. The conductivity type, the free carrier concentration, and the Hall mobility were determined using the van der Pauw geometry. Hall measurements on homogeneously doped GaAs layers were used to calibrate the flux of the C effusion cell. Secondary Ionization Mass Spectroscopy (SIMS) was also used to check the concentration in these GaAs layers. The Hall and SIMS results agreed to within 20 percent.



In the preferred exemplary embodiment, the epitaxial layers form (GaAs)_{3.76}(InAs)_{4.24} superlattices with 256 periods and a total layer thickness of $256 \times 8 \times 2.94 \text{ \AA} = 0.6 \text{ \mu m}$. In one set of epitaxial layers, e.g., region 13, the InAs layers are δ -doped in the center with C, and the GaAs layers are left undoped as shown in FIG. 2 forming an n-type conductivity region 13. In another set of layers, e.g., region 14, the GaAs layers are δ -doped in the center with C, and the InAs layers are left undoped as shown in FIG. 2 forming a p-type conductivity region 14. The superlattice may be grown in an inverted manner, such that the p-type conductivity region 14 is grown in adjacent substrate 11, and n-type conductivity region 13 is grown subsequently to the p-type conductivity region.

Room-temperature Hall measurements of the epitaxial layers reveal that C doping of the InAs layers and the GaAs layers results in n-type and p-type conductivity, respectively. This demonstrates that only one impurity element can be used in a short-period superlattice to achieve both conductivity types in a semiconductor. The C sheet densities in the thin GaAs and InAs layers were varied between $4 \times 10^9 \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$, which translates into three-dimensional concentrations of $1.7 \times 10^{16} \text{ cm}^{-3}$ to $4.2 \times 10^{18} \text{ cm}^{-3}$, respectively.

Free electron concentrations as high as $2 \times 10^{16} \text{ cm}^{-3}$ were achieved by C δ -doping of the InAs layers of the superlattice. The Hall electron mobility at this concentration is $2300 \text{ cm}^2/\text{Vs}$. The electron mobility is somewhat lower than the mobilities in the Si-doped ternary alloy $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$, which possibly indicates additional scattering by either the superlattice structure or by compensating C acceptors. Note that the residual background impurity concentration in $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ is $n \approx 1 \times 10^{15} \text{ cm}^{-3}$.

The realization of the n-type $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}:\text{C}$ superlattices demonstrates that the C impurities do not redistribute significantly. The InAs layers of the superlattice are approximately 4 monolayers, i.e., 1.2 nm ($12 \text{ \AA}$) thick. In order to obtain n-type conductivity, the C impurities must remain within the thin InAs layer. Therefore, it may be concluded that the C impurities do not diffuse or migrate over more than 0.6 nm ($6 \text{ \AA}$) during the epitaxial growth process.

Selective δ -doping of the GaAs layers of the superlattice results in p-type conductivity of the $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ superlattice. The hole concentration can be controlled in the $10^{15} - 10^{18} \text{ cm}^{-3}$ range. The highest free hole concentrations achieved by selective C δ -doping of the GaAs layers are $3 \times 10^{18} \text{ cm}^{-3}$ and a corresponding hole mobility of $40 \text{ cm}^2/\text{Vs}$. At the lower hole concentration of $1 \times 10^{16} \text{ cm}^{-3}$, the hole mobility increased to $200 \text{ cm}^2/\text{Vs}$. This value for the hole



mobility is comparable to Be-doped $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ with the same doping concentration. The comparison between Be- and C-doped $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ indicates, that auto-compensation in selectively C doped $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ superlattices is small.

Current-voltage characteristics of the p-n junctions were evaluated using
5 an Hewlett-Packard 4145B parameter analyzer. For this purpose, the samples were mesa-etched to a depth below the plane of the p-n junction. The current-voltage (IV) characteristic of the 500 μm diameter diodes is shown in FIG. 5. The characteristic is rectifying with a relatively smooth turn-on voltage at 0.4V. In reverse direction,
10 the current depends linearly on the voltage indicating a resistive leakage which is probably due to point defects in the superlattice or possibly due to surface effects.

The invention has been described with reference to carbon doped $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ lattice matched to an InP substrate. P-n junctions using a $\text{Ga}_{0.515}\text{In}_{0.485}\text{P}$ lattice matched to a GaAs substrate may be produced in the same manner. In this case the number of monolayers in GaP and in InP layers 22 and 21,
15 respectively, will be deposited in the ratio of 0.515:0.485. Also, instead of a p-n junction produced by C-doping, GaAs and InAs (or GaP and InP) p-n junctions in which only one of the regions, either p- or n-type conductivity, may be produced with a superlattice, e.g., as is shown in FIGS. 3 and 4. The other of the regions, e.g.
20 14 is FIG. 3 or 13 in FIG. 4, may be produced with conventional dopants. Furthermore, C as the amphoteric dopant may be replaced by Ge or Si. Since these dopants have a higher coefficient of diffusion in III-V semiconductors, care should be taken in placing sheets of these dopants between the monolayers of the respective layers so as to avoid the possibility of Ge or Si acting as the compensating dopant rather than p- or n-type dopant.



Claims:

1. A group III-V compound semiconductor device including a doped region, said doped region comprising a superlattice having a plurality of periods (20), each period including two layers of first and second materials respectively (21, 5 22), only the layer of first material being doped with an amphoteric dopant (22) which, in said first material, imparts a first conductivity type, but which, in said second material would impart the opposite conductivity type

CHARACTERIZED IN THAT

- 10 said dopant is selectively introduced by δ -doping into the center of said layer of said first material in each period.

2. A device as claimed in claim 1 including a second doped region having said opposite conductivity type.

3. A device as claimed in claim 2 wherein said second doped region comprises a superlattice having a plurality of periods, each period including two 15 layers, of said first and second materials respectively, only the layer of said second material being doped with said amphoteric dopant, said dopant being selectively introduced by δ -doping into the center of said layer of said second material in each period.

- 20 4. A device as claimed in claim 2 or claim 3 wherein the said doped regions form a p-n junction (15).

5. The device of any of the preceding claims, in which each of the periods includes a plurality of monolayers, ranging in number from 5 to 15 in a numerical ratio corresponding to a cation compositional ratio in said compound semiconductor.

- 25 6. The device of any of the preceding claims, in which said amphoteric dopant comprises carbon.

7. The device of any of the preceding claims, in which each period includes 8 monolayers.

8. The device of any of the preceding claims, in which carbon is included



in the respective layers in concentrations of from 1×10^{16} to 5×10^{18} per cm^3 .

9. The device of any of the preceding claims, in which the or each said superlattice includes from 10 to 500 of said periods.

10. The device of claim 9, in which the or each said superlattice includes
5 from 100 to 300 of said periods.

11. The device of any of the preceding claims, in which said compound semiconductor is selected from the group consisting of $\text{Ga}_x\text{In}_{1-x}\text{As}$, $(\text{GaAl})_x\text{In}_{1-x}\text{As}$, and $\text{Al}_x\text{In}_{1-x}\text{As}$, wherein x is 0.47 ± 0.05 .

12. The device of claim 11, formed on a substrate of InP and in which
10 said compound semiconductor comprises $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$.

13. The device of any of claims 1 to 10 in which said compound semiconductor is selected from the group consisting of $\text{Ga}_y\text{In}_{1-y}\text{P}$, $(\text{GaAl})_y\text{In}_{1-y}\text{P}$ and $\text{Al}_y\text{In}_{1-y}\text{P}$ wherein y is 0.515 ± 0.05 .

14. The device of claim 13, formed on a substrate of GaAs and in which
15 said compound semiconductor comprises $\text{Ga}_{0.515}\text{In}_{0.485}\text{P}$.

15. The p-n junction device of any of the preceding claims, in which said layers and the amphoteric dopant are deposited by MBE.