ABSTRACT

Shared Memory Array for Data Block and Control Program Storage in Disk Drive.

An improved disk drive architecture includes a microcontroller interface circuit (34) connected between a drive microcontroller (26) and a buffer controller (36). The microcontroller interface circuit (34) includes address mapping registers (48) for mapping at least one predetermined portion of directly addressable memory of the microcontroller (26) to address locations of the drive's cache buffer (28). The buffer controller circuit (36) includes an access arbitration circuit (52) for arbitrating requests for access to the cache buffer (28) by the drive's data sequencer (38):, the drive's host interface controller (40) and the drive's microcontroller (26). A microcontroller wait state generator (60) responds to the access arbitration circuit by generating and applying a wait state sequence to the microcontroller (26) until a request it makes for access to the cache buffer (28) can be executed.

FIGURE 2

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