

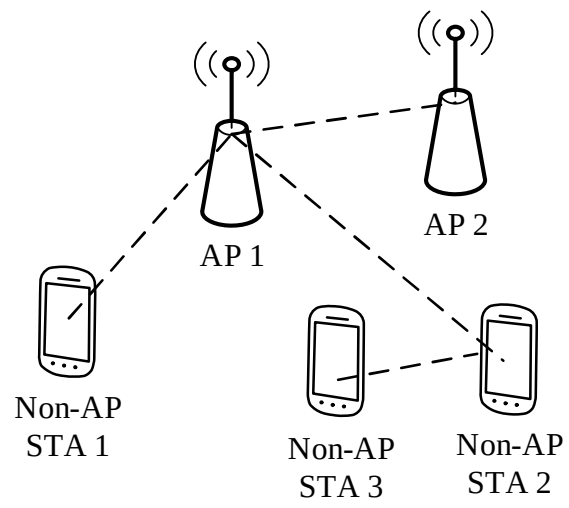


FIG. 1

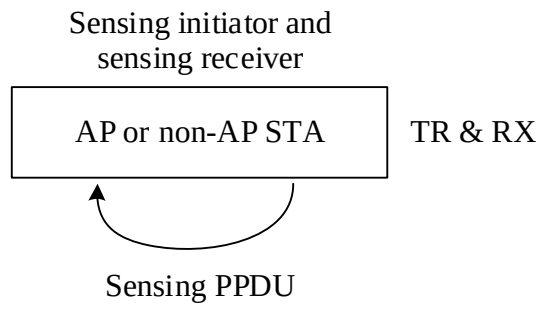


FIG. 2(a)

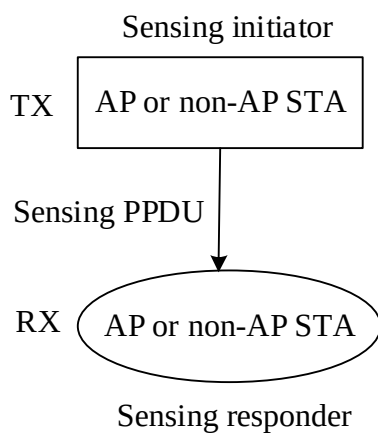


FIG. 2(b)

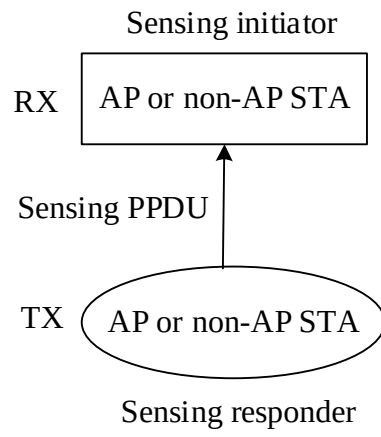


FIG. 2(c)

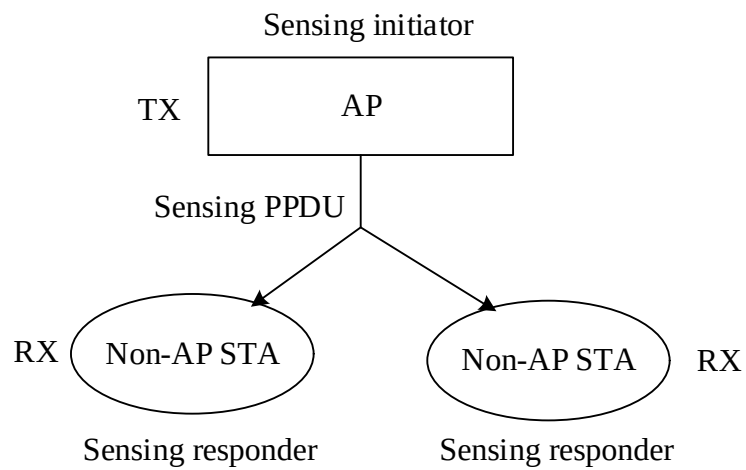


FIG. 2(d)

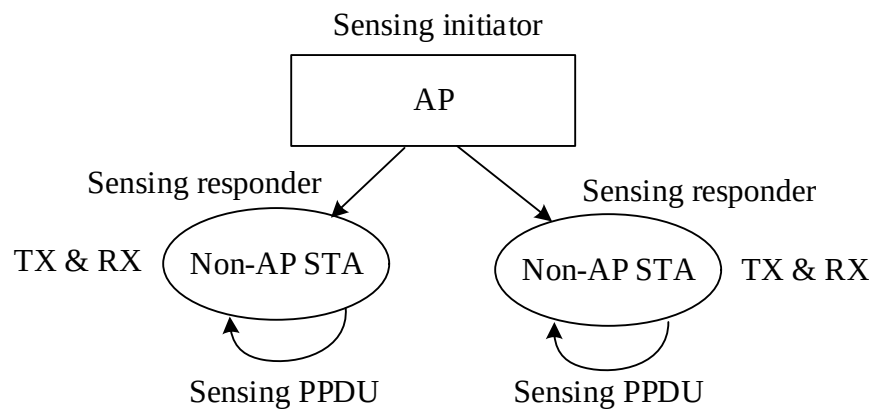
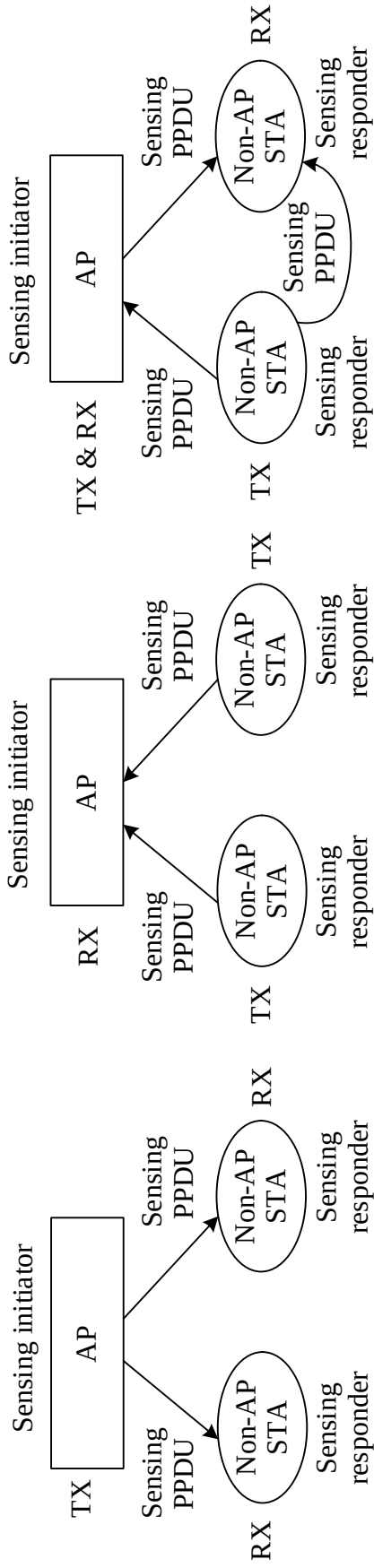


FIG. 2(e)



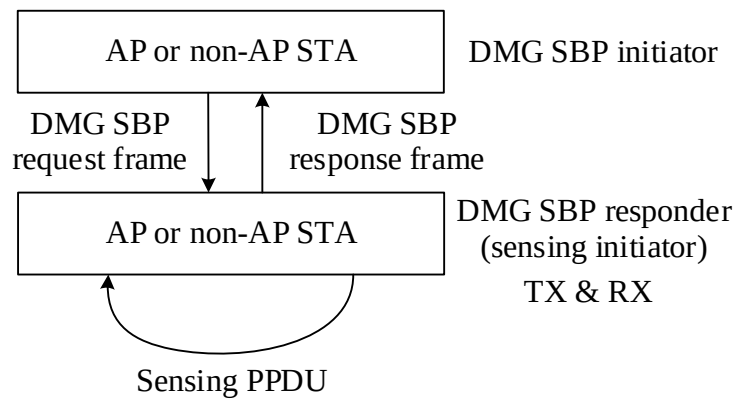


FIG. 3(a)

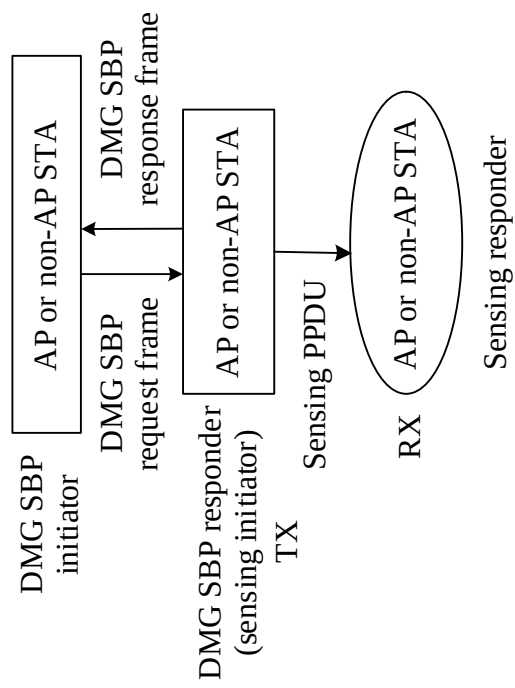


FIG. 3(b)

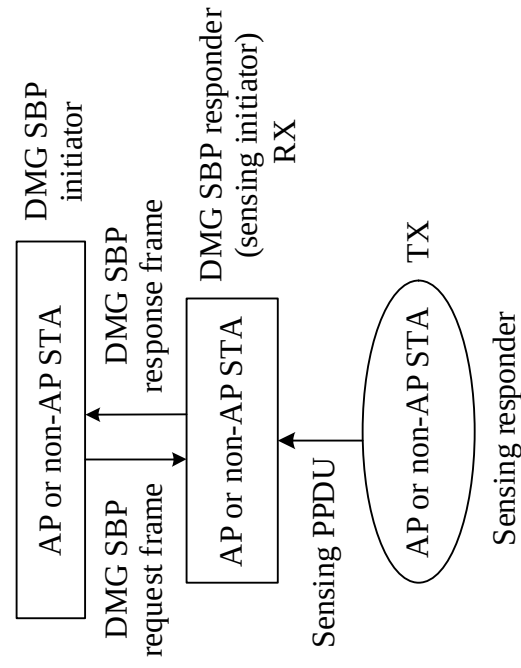


FIG. 3(c)

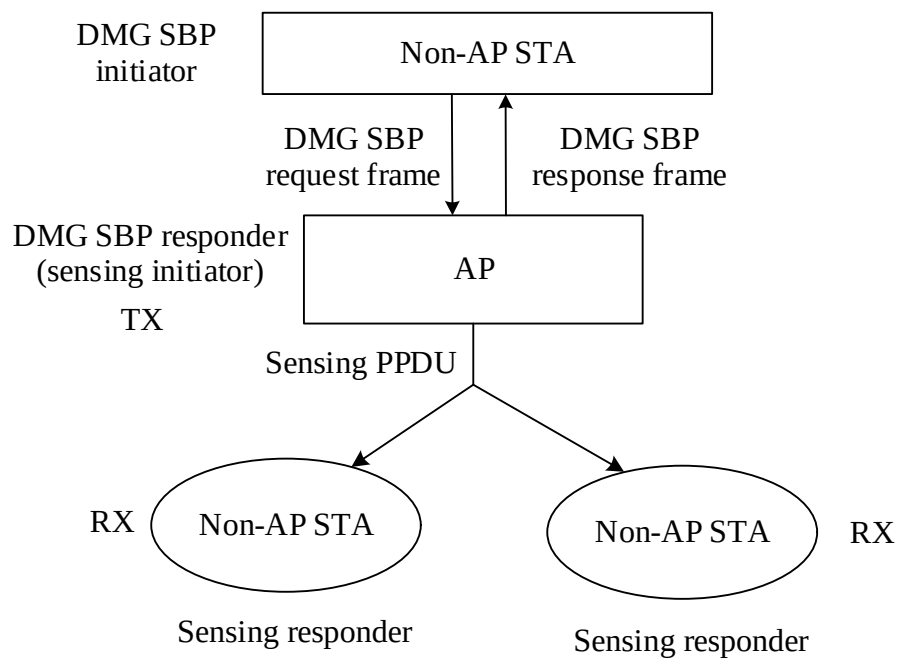


FIG. 3(d)

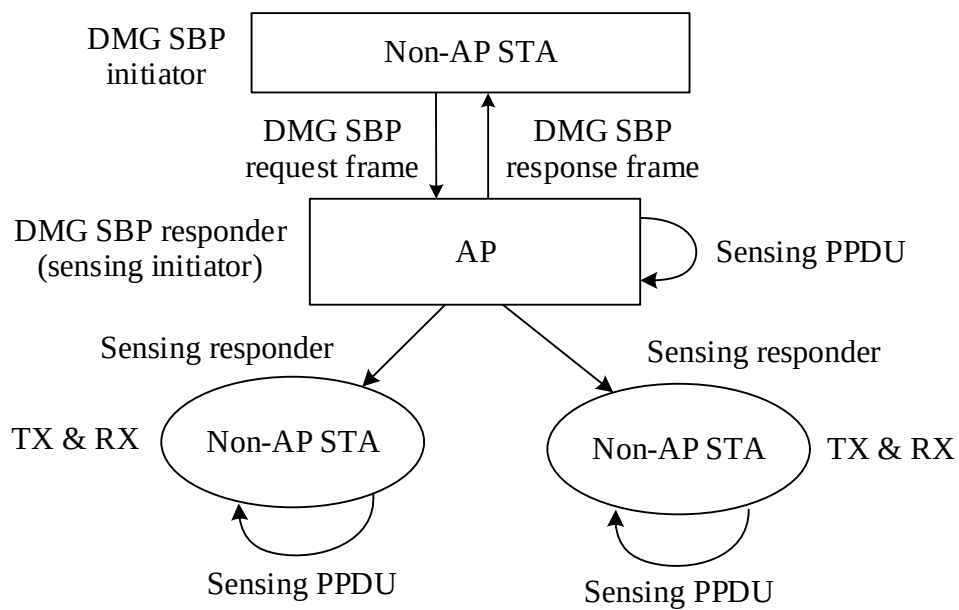


FIG. 3(e)

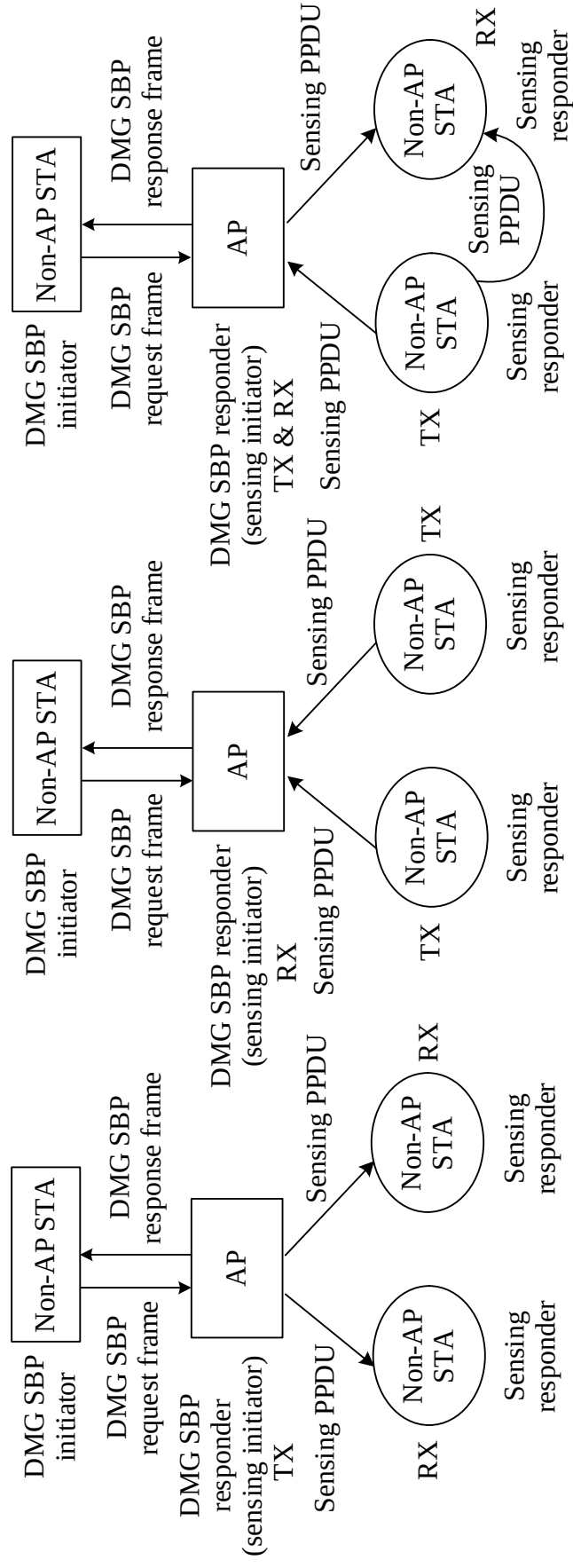


FIG. 3(f)

FIG. 3(g)

FIG. 3(h)

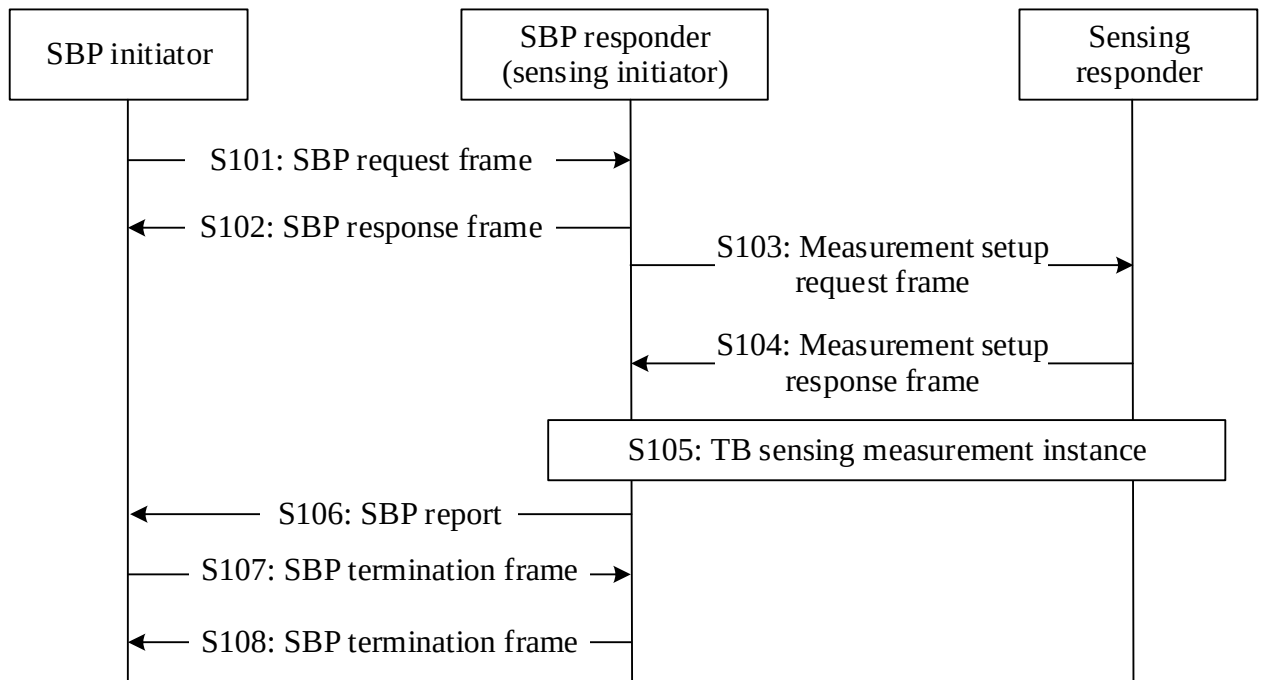


FIG. 4

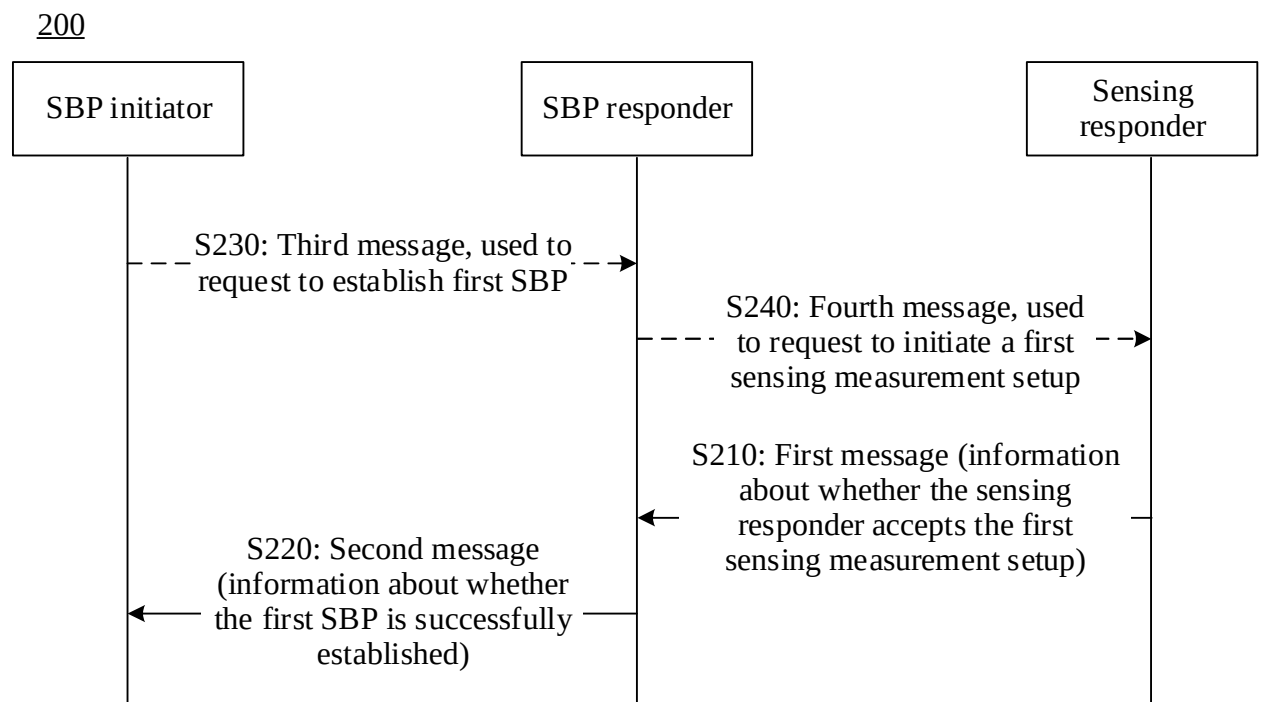


FIG. 5

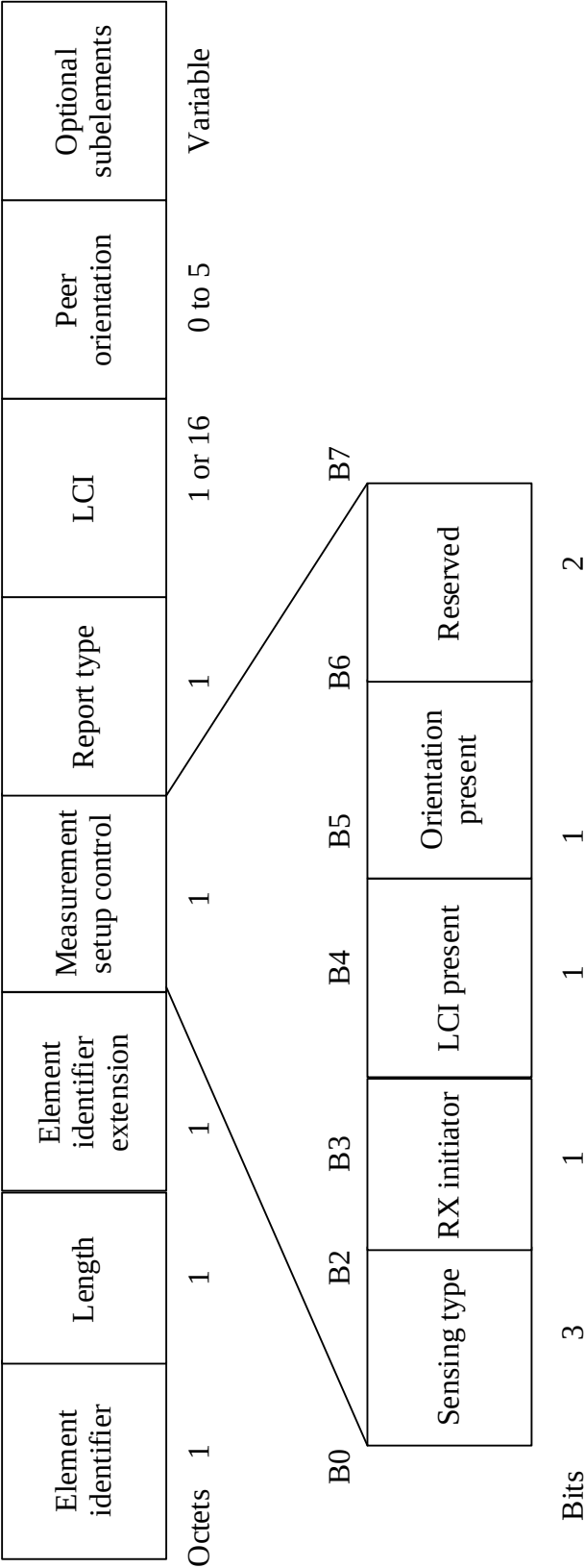


FIG. 6

300

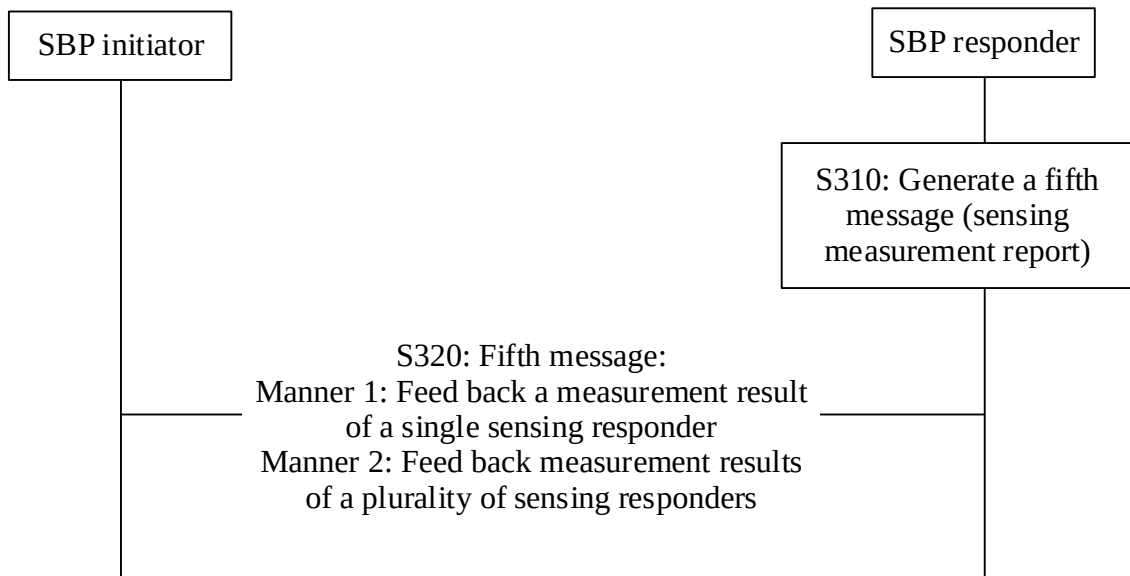


FIG. 7

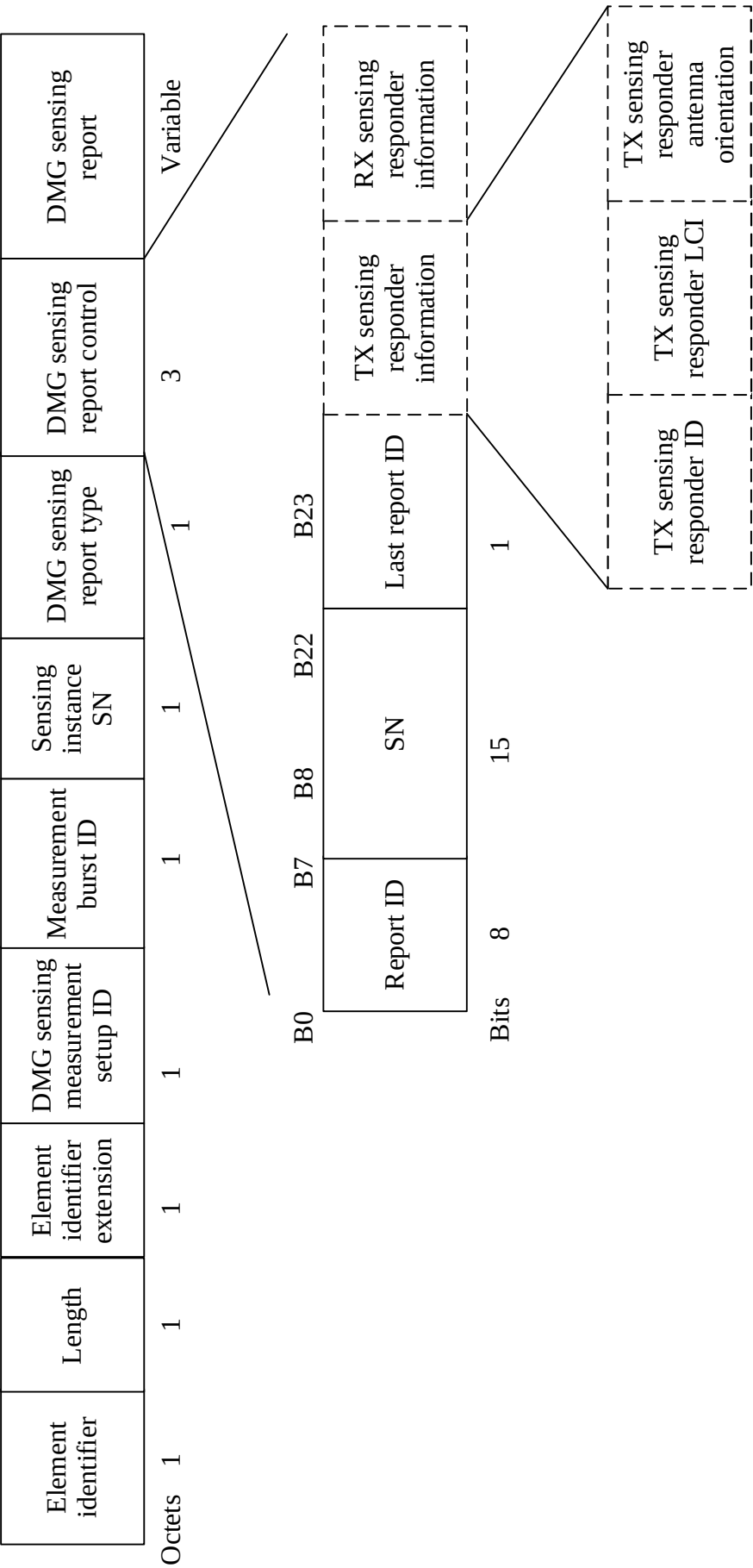


FIG. 8

400

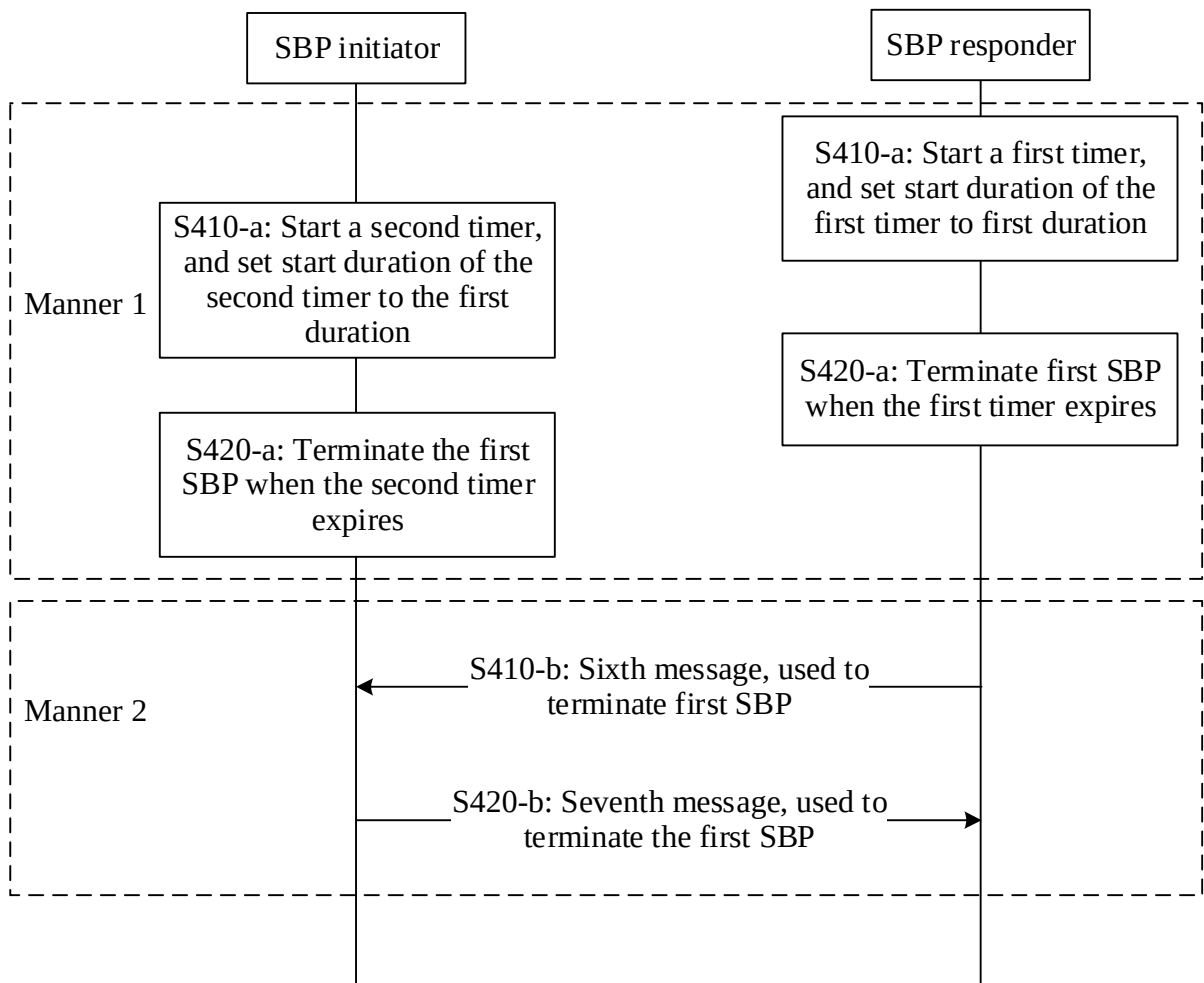


FIG. 9

Terminate all coordinated monostatic setups	Terminate all bistatic setups	Terminate all multistatic setups	Terminate all coordinated bistatic setups	Terminate all monostatic setups	DMG SBP setup unsuccess	Reserved
Bits 1	1	1	1	1	1	4

FIG. 10

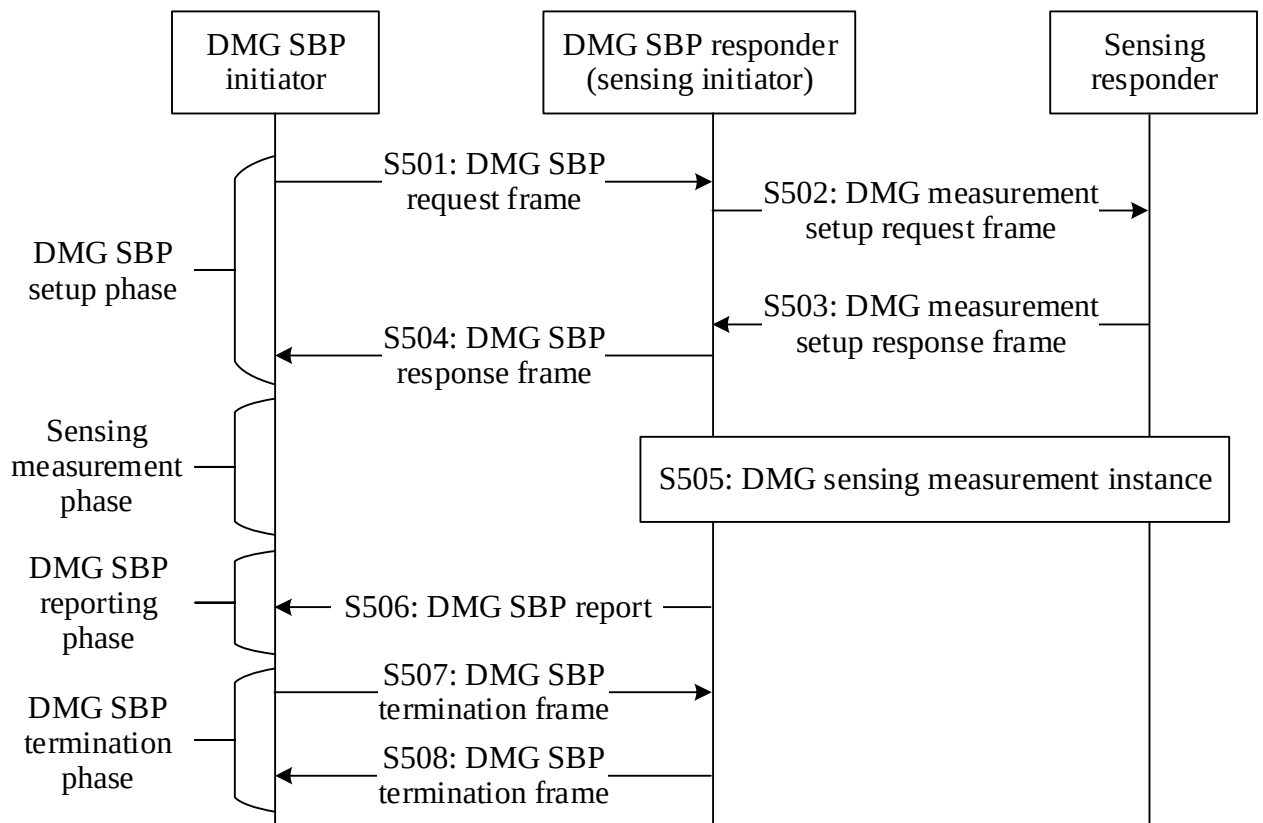


FIG. 11

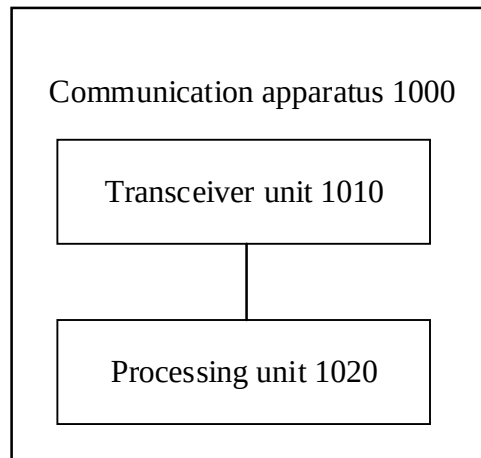


FIG. 12

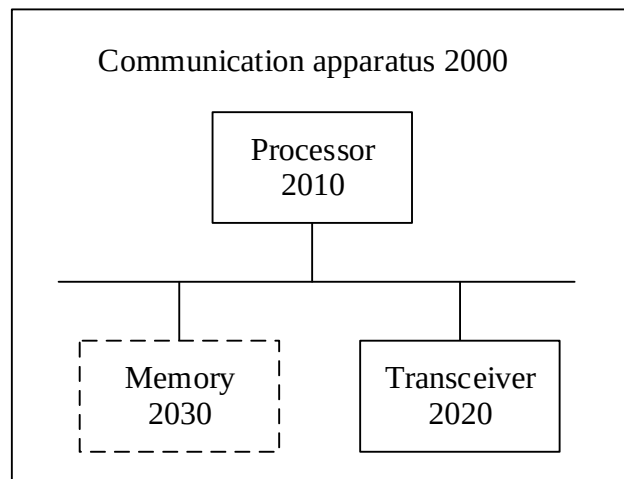


FIG. 13

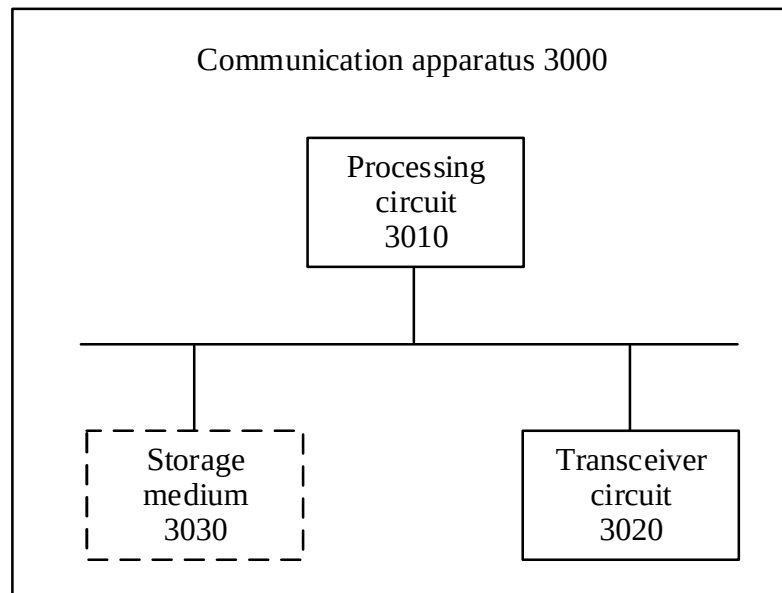


FIG. 14