Claims

What is claimed is:

1. An electrically erasable programmable read only memory (EEPROM) cell, comprising:

a first gate and a second gate arranged on a substrate, wherein the first gate comprises a first floating gate and a first control gate stacked from bottom to top, and the second gate comprises a second floating gate and a second control gate stacked from bottom to top; and

an erasing gate sandwiched between the first gate and the second gate, wherein one side part of the first floating gate directly under the erasing gate and one side part of the second floating gate directly under the erasing gate have multiple tips,

wherein the electrically erasable programmable read only memory (EEPROM) cell further comprising a first hard mask disposed on the first control gate, and a second hard mask disposed on the second control gate,

wherein a top surface of the first hard mask and a top surface of the second hard mask are higher than a top surface of the erasing gate, and

wherein the electrically erasable programmable read only memory (EEPROM) cell further comprising a plurality of spacers disposed on the erasing gate to cover at least a portion of an upper surface of the erasing gate, and disposed on the sides of the first hard mask and the second hard mask.

2. The electrically erasable programmable read only memory (EEPROM) cell according to claim 1, further comprising:

a source line located in the substrate directly under the erasing gate.

3. The electrically erasable programmable read only memory (EEPROM) cell according to claim 1, wherein the side part of the first floating gate directly under the erasing gate and the side part of the second floating gate directly under the erasing gate are both two-step side parts.

4. The electrically erasable programmable read only memory (EEPROM) cell according to claim 3, wherein each two-step side part comprises two steps.

5. The electrically erasable programmable read only memory (EEPROM) cell according to claim 1, further comprising:

a first word line disposed on a side of the first gate opposite to the erasing gate, and a second word line disposed on a side of the second gate opposite to the erasing gate.

6. The electrically erasable programmable read only memory (EEPROM) cell according to claim 5, further comprising:

a plurality of bit lines disposed in the substrate, wherein one of the bit line is disposed at a side of the first word line opposite to the erasing gate, and another one of the bit line is disposed at a side of the second word line opposite to the erasing gate.

7. The electrically erasable programmable read only memory (EEPROM) cell according to claim 6, further comprising a plurality of bit line contact plugs disposed directly above the bit lines.

8. The electrically erasable programmable read only memory (EEPROM) cell according to claim 1, wherein the other side part of the first floating gate opposite to the erasing gate and the other side part of the second floating gate opposite to the erasing gate have vertical sidewalls.

9. A method of forming an electrically erasable programmable read only memory (EEPROM) cell, comprising:

sequentially forming a floating gate layer and a control gate stacked on a substrate;

forming a first spacer on the floating gate layer and at a first side of the control gate;

removing an exposed top of the floating gate layer to form a pre-floating gate layer, wherein the pre-floating gate layer has a stepped side part;

forming a second spacer on the pre-floating gate layer and on the first side of the control gate; and

removing an exposed part of the pre-floating gate layer, so as to form a floating gate, wherein the floating gate has a two-step side part;

forming a polysilicon layer on the substrate on the side of the floating gate, wherein a part of the polysilicon layer on the side of the two-step side part serves as an erasing gate, and a part of the polysilicon layer opposite to the two-step side part serves as a word line; and

forming a plurality of third spacers disposed on the erasing gate to cover at least a portion of an upper surface of the erasing gate.

10. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 9, wherein the step of sequentially forming the floating gate layer and the control gate stacked on the substrate comprises:

sequentially forming the floating gate layer, a control gate layer and a hard mask layer to cover the substrate;

patterning the hard mask layer and the control gate layer to form the control gate and a hard mask.

11. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 9, wherein the step of forming the first spacer on the floating gate layer and on the first side of the control gate comprises:

forming the first spacer on the floating gate layer, and on the first side and a second side of the control gate respectively; and

removing the first spacer on the second side of the control gate, but the first spacer on the first side of the control gate is remained.

12. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 11, wherein

before removing the first spacer on the second side of the control gate, further comprising:

forming a first doped region in the substrate at a side of the first spacer on the second side of the control gate.

13. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 9, after forming the floating gate with the two-step side part, further comprising:

removing the first spacer on the first side of the control gate.

14. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 9, wherein the step of forming the second spacer on the pre-floating gate layer and on the first side of the control gate comprises:

forming the second spacer on the pre-floating gate layer and on the first side and a second side of the control gate respectively; and

removing the second spacer on the second side of the control gate, but remaining the second spacer on the first side of the control gate.

15. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 14, before removing the second spacer on the second side of the control gate, further comprising:

forming a second doped region in the substrate on the side of the second spacer on the second

side of the control gate.

16. The method for forming an electrically erasable programmable read only memory (EEPROM) cell according to claim 9, wherein a width of the first spacer is half a width of the second spacer.