

FIG. 1

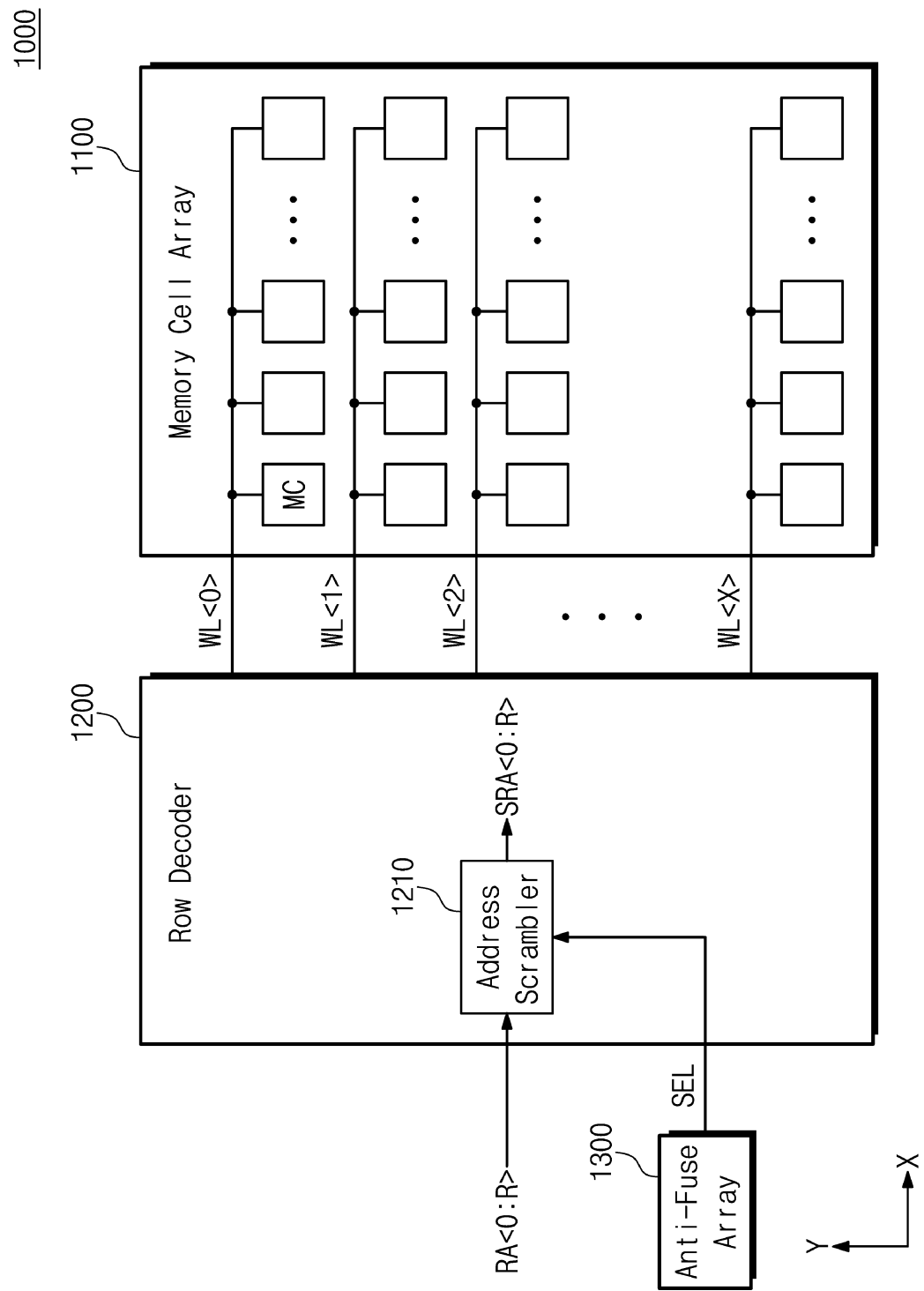


Figure 1100 is a detailed block diagram of a memory array architecture. The diagram is organized into two main sections, MAT<0> and MAT<1>, each containing four columns of blocks. The columns are labeled with PXI and NWEIB signals. Each column contains a CJT block, a BLSAs block, and a SWDs block. The SWDs blocks are further divided into WL and MAT sub-blocks. The diagram includes various signal lines and addresses, such as PXID<0,2>, PXIB<0,2>, WL<0>, WL<1>, MAT<0>, MAT<1>, and SWDs. The diagram is labeled 1100 in the top left corner.

FIG. 3

1100

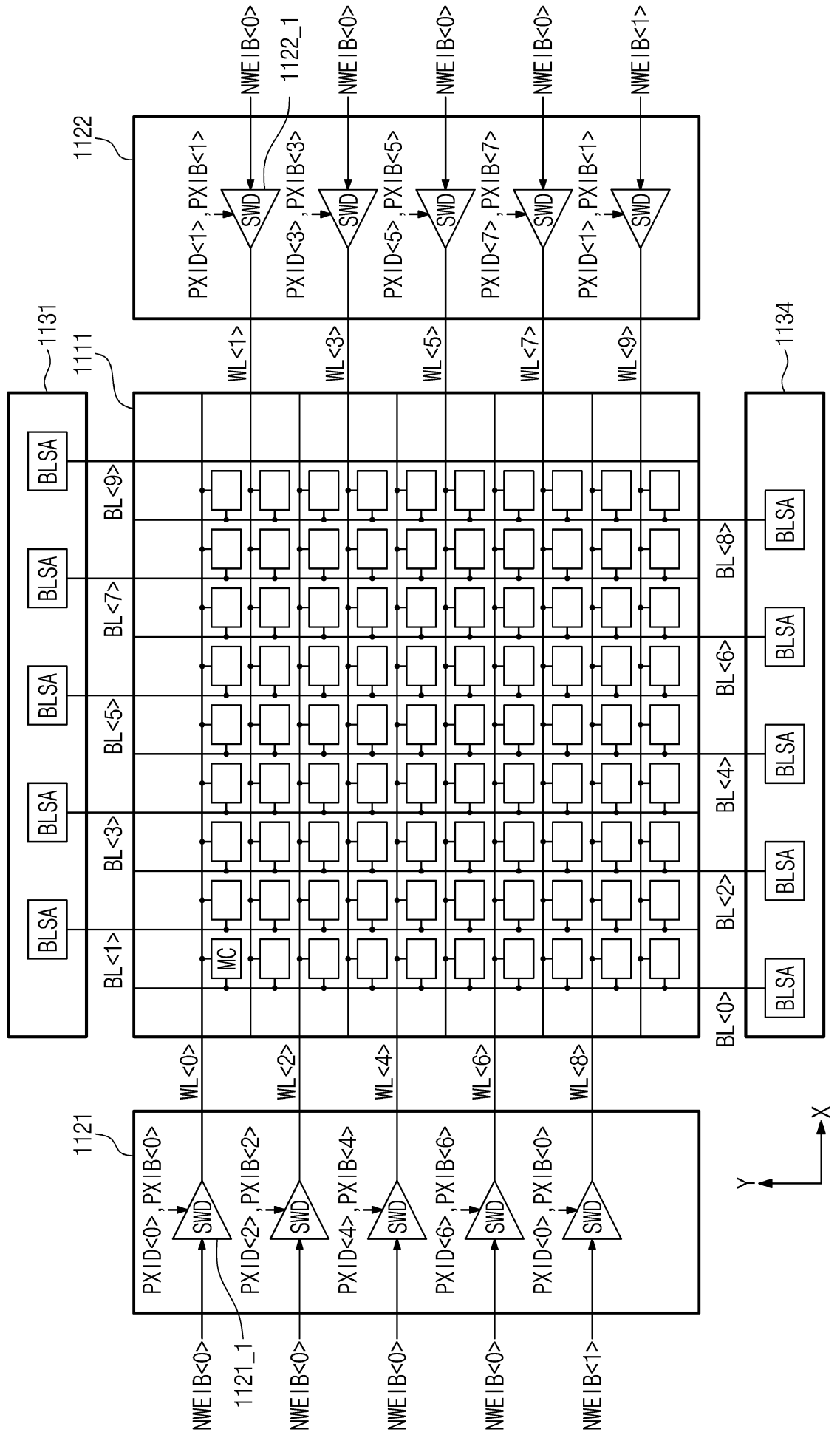


FIG. 4

1121_1

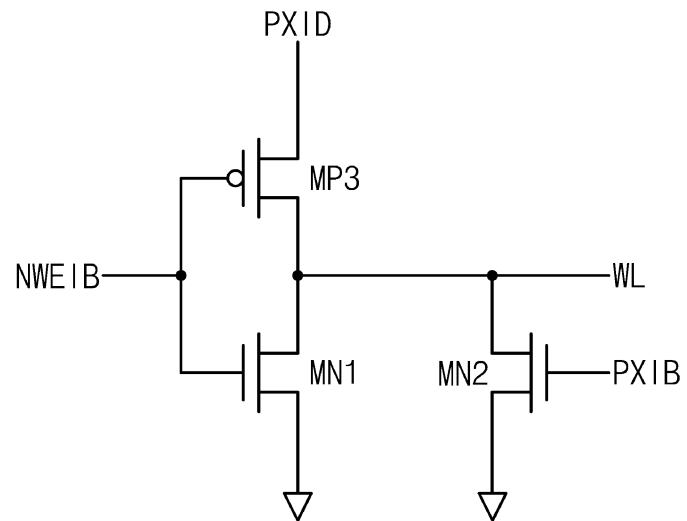


FIG. 5

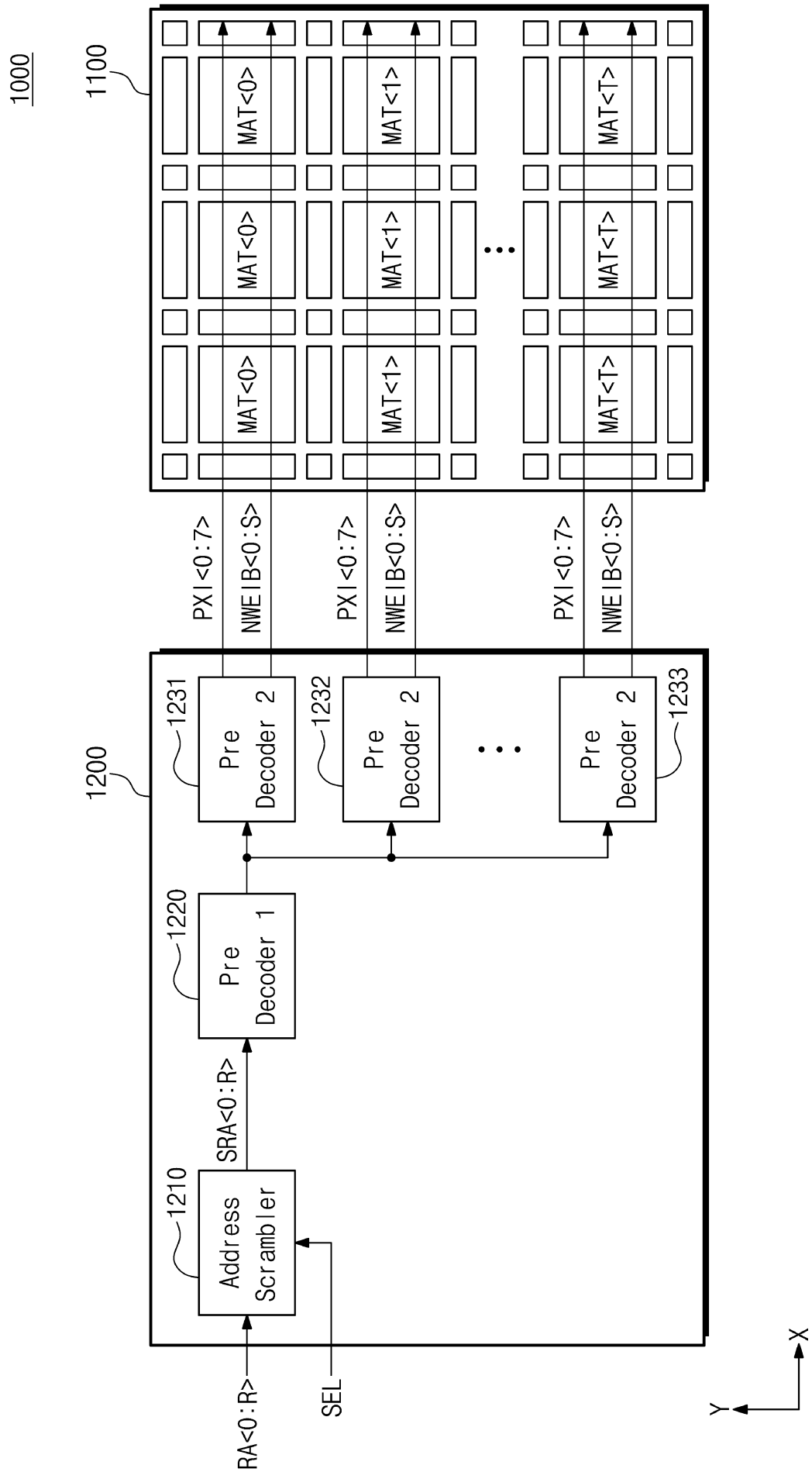


FIG. 6

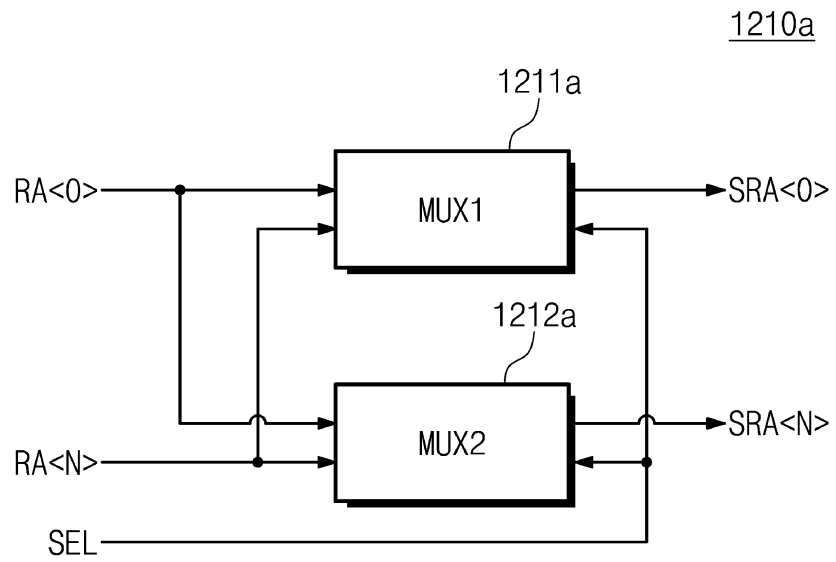


FIG. 7

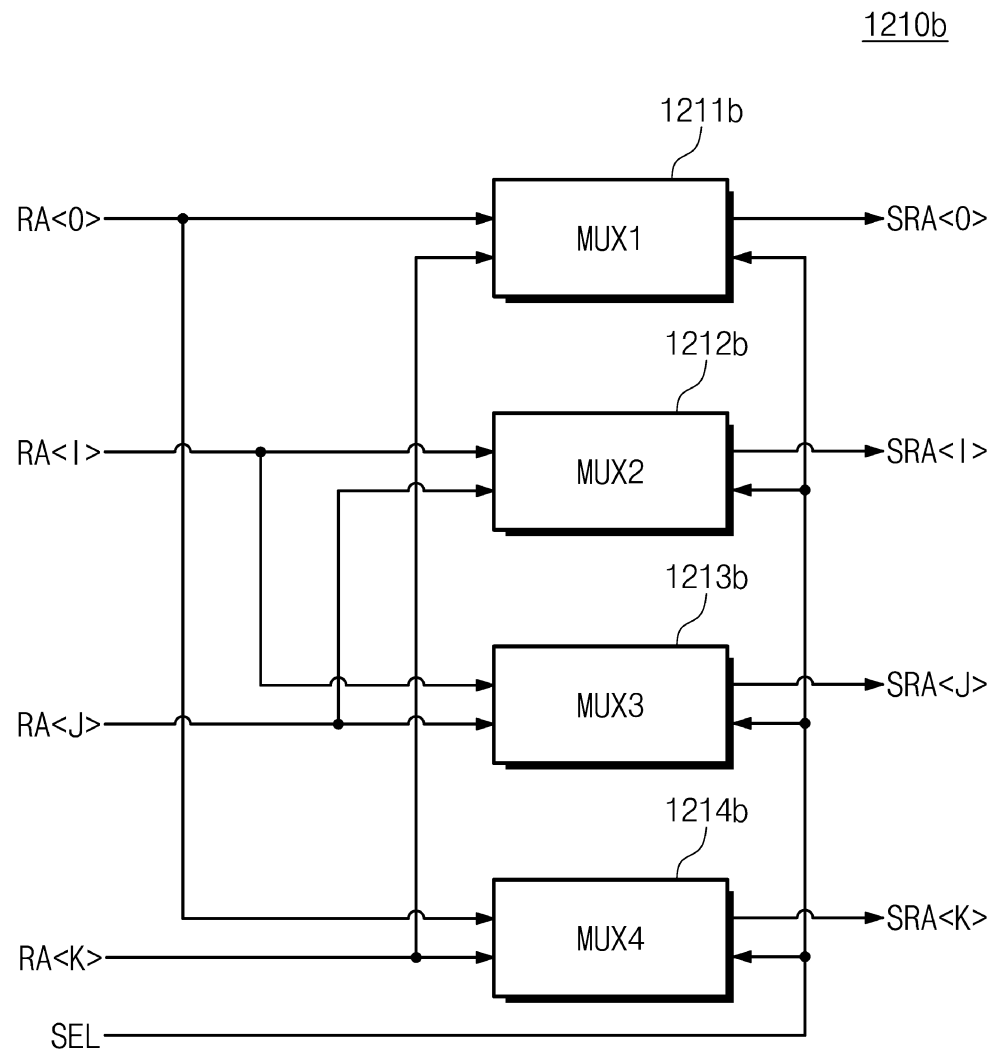


FIG. 8

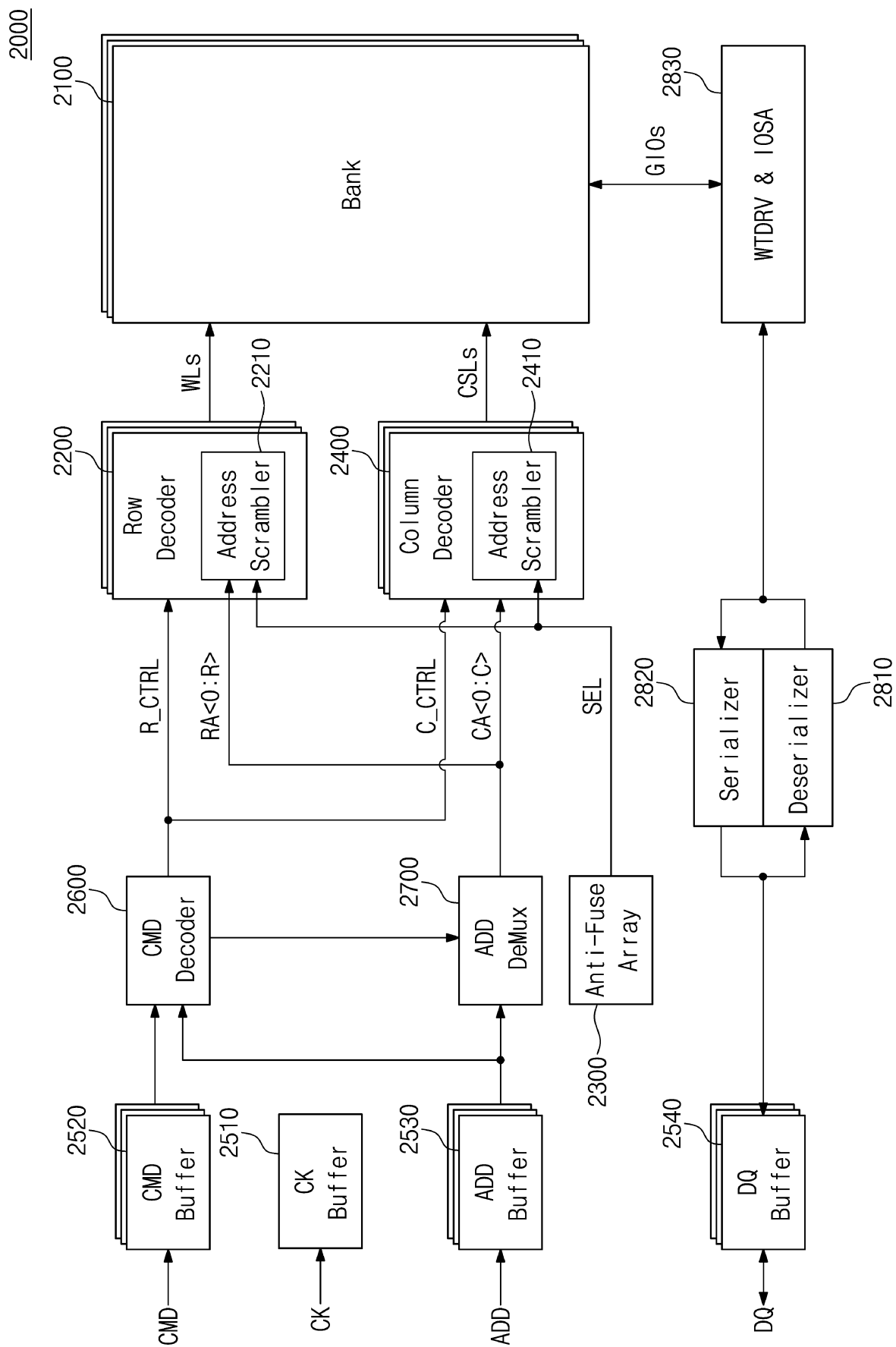


FIG. 9

2000

2100

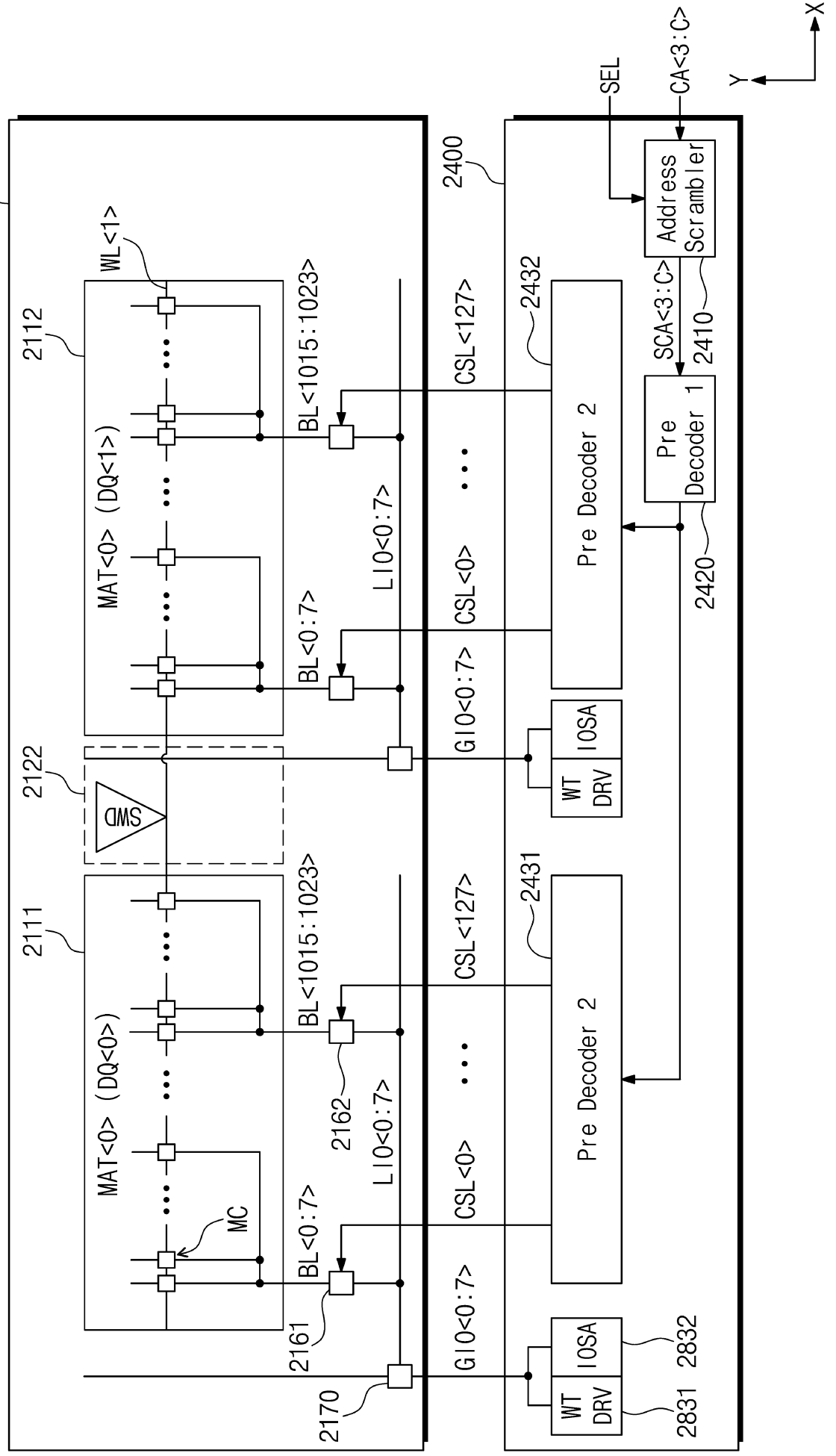


FIG. 10

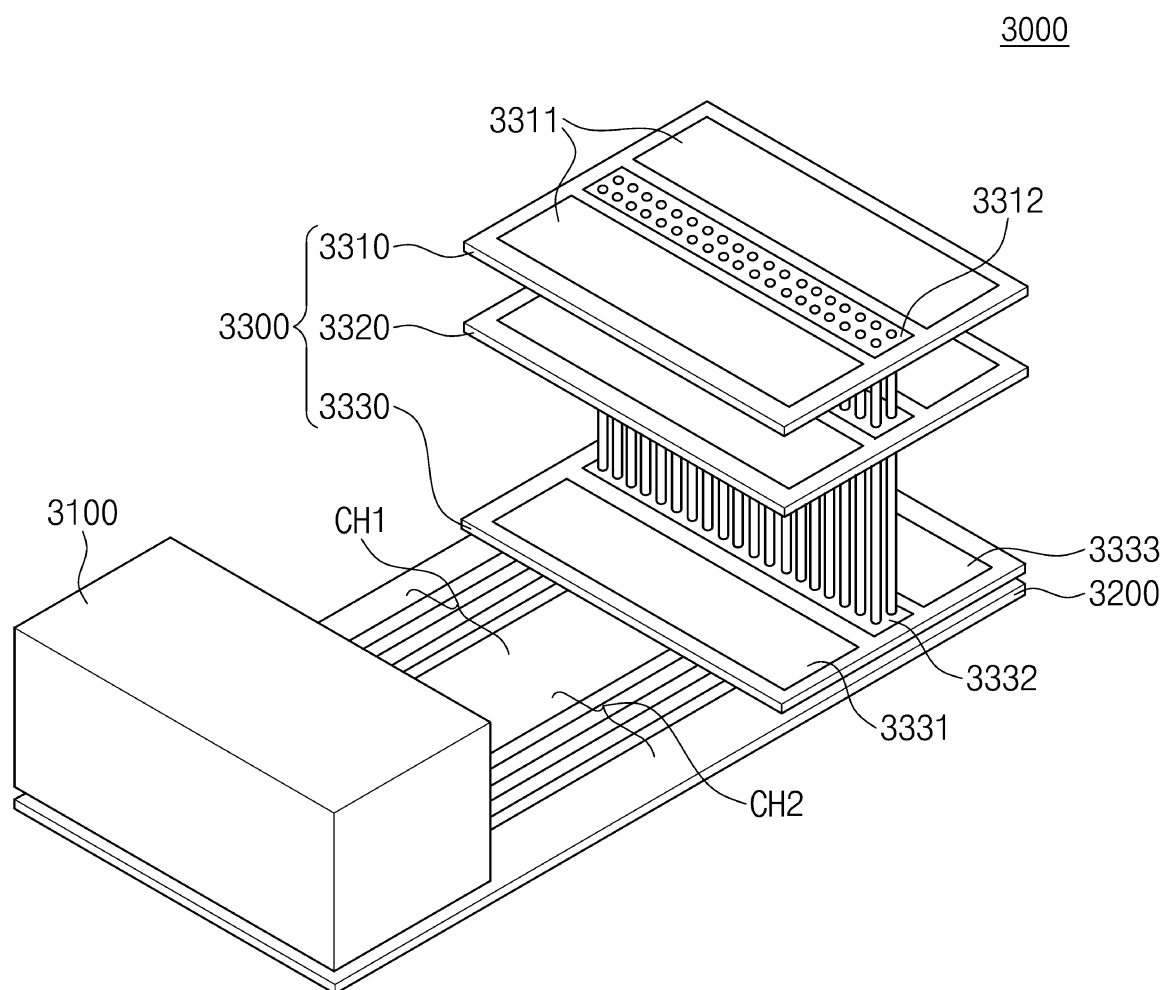


FIG. 11

