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(57) Abstract: A wordline tracking structure for use in an array of Flash EEPROM memory cells is provided. The tracking structure serves to match reference and sector core wordline voltages across the entire chip regardless of sector location. The tracking structure includes a second VPXG conductor line (422) operatively connected between sector wordlines of a "far" sector and a reference cell mini-array. The second VPXG conductor line has a substantially smaller time constant than in a first VPXG conductor line (421) operatively connected between an output of a boosting circuit and the sector wordline of the "far" sector. As a consequence, the reference wordlines voltage associated with the reference cell mini-array will track closely the sector wordline voltage during the read operation regardless of the location of the selected sector.