

FIG. 1

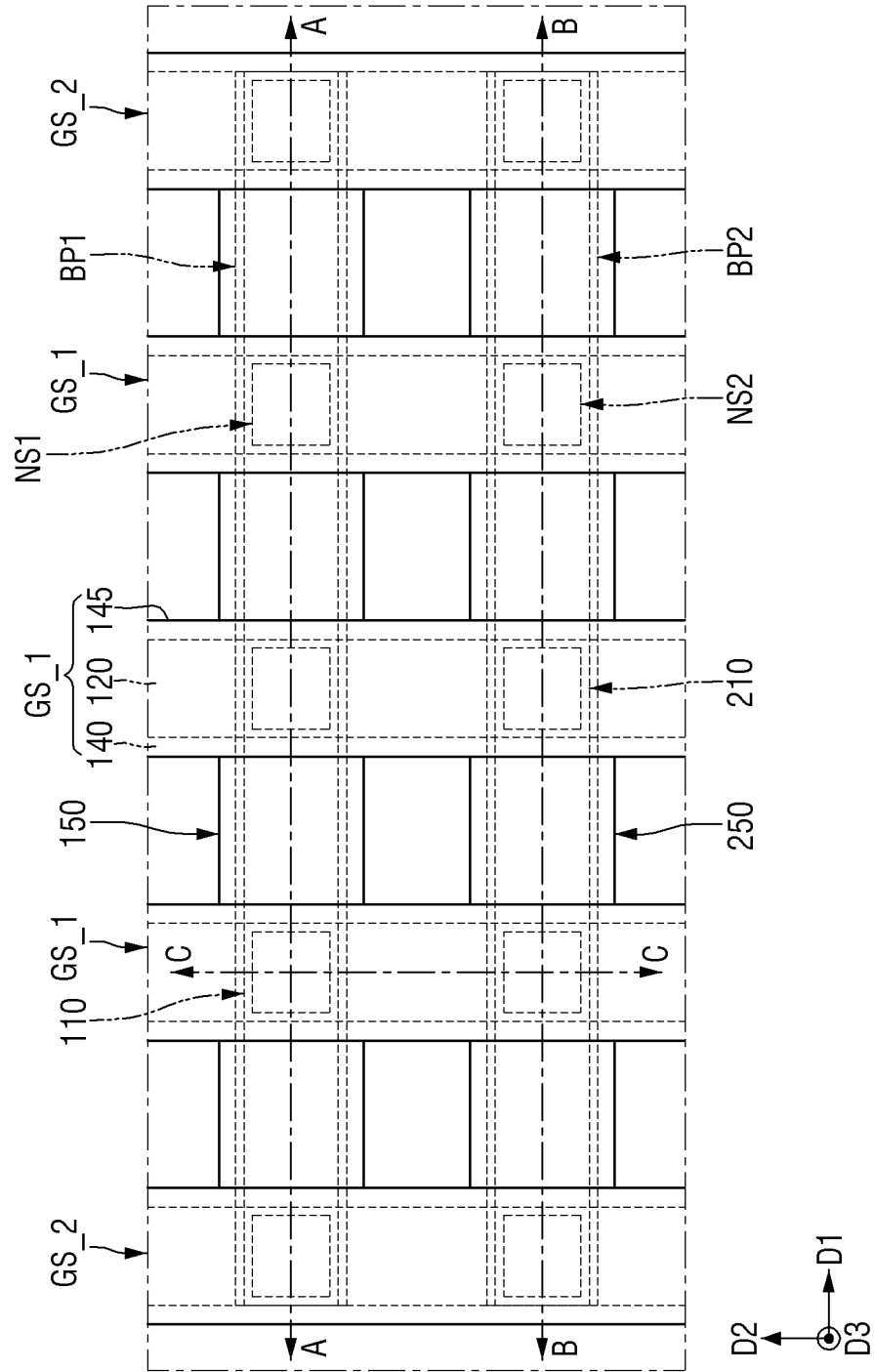


FIG. 2

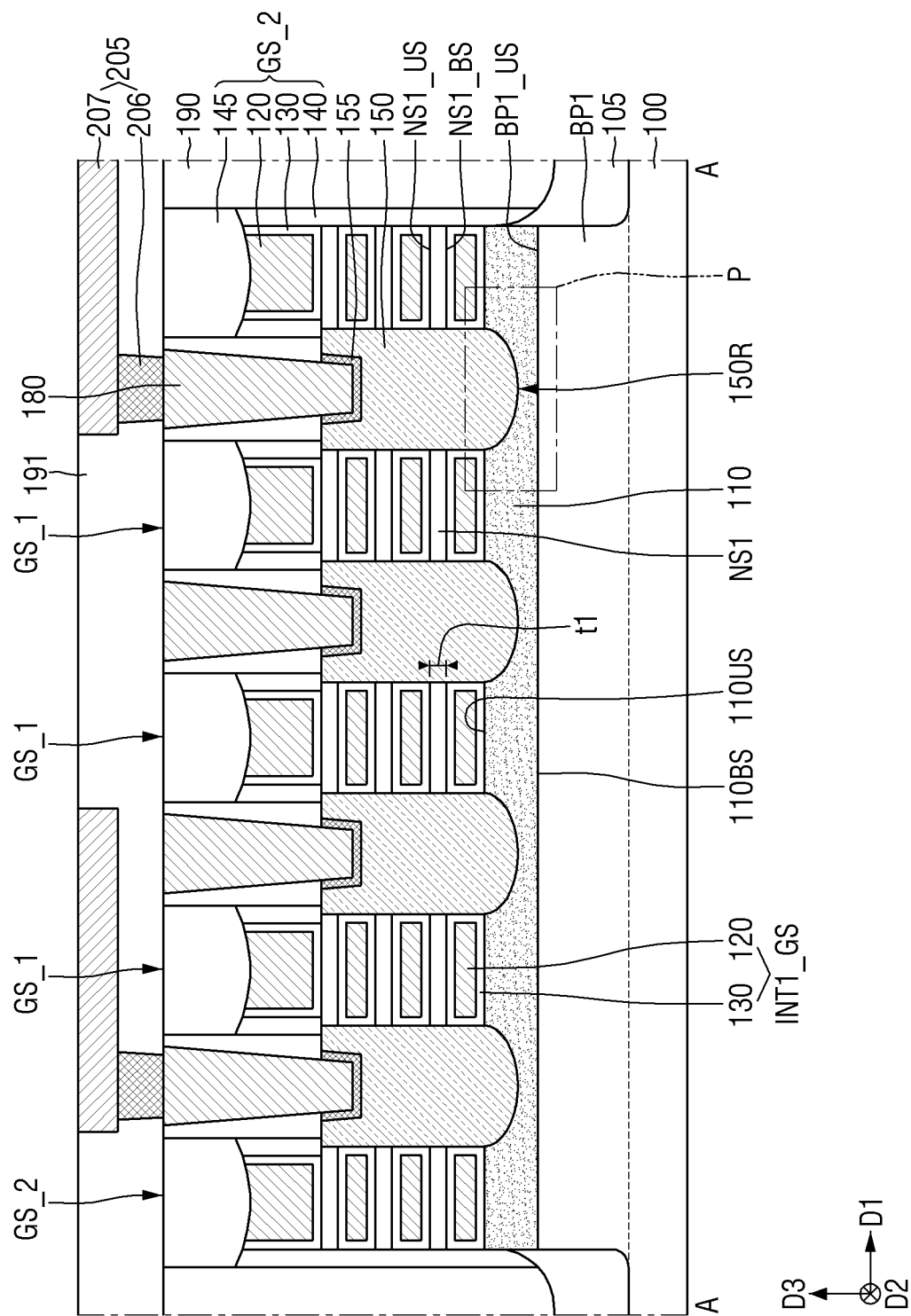


FIG. 3

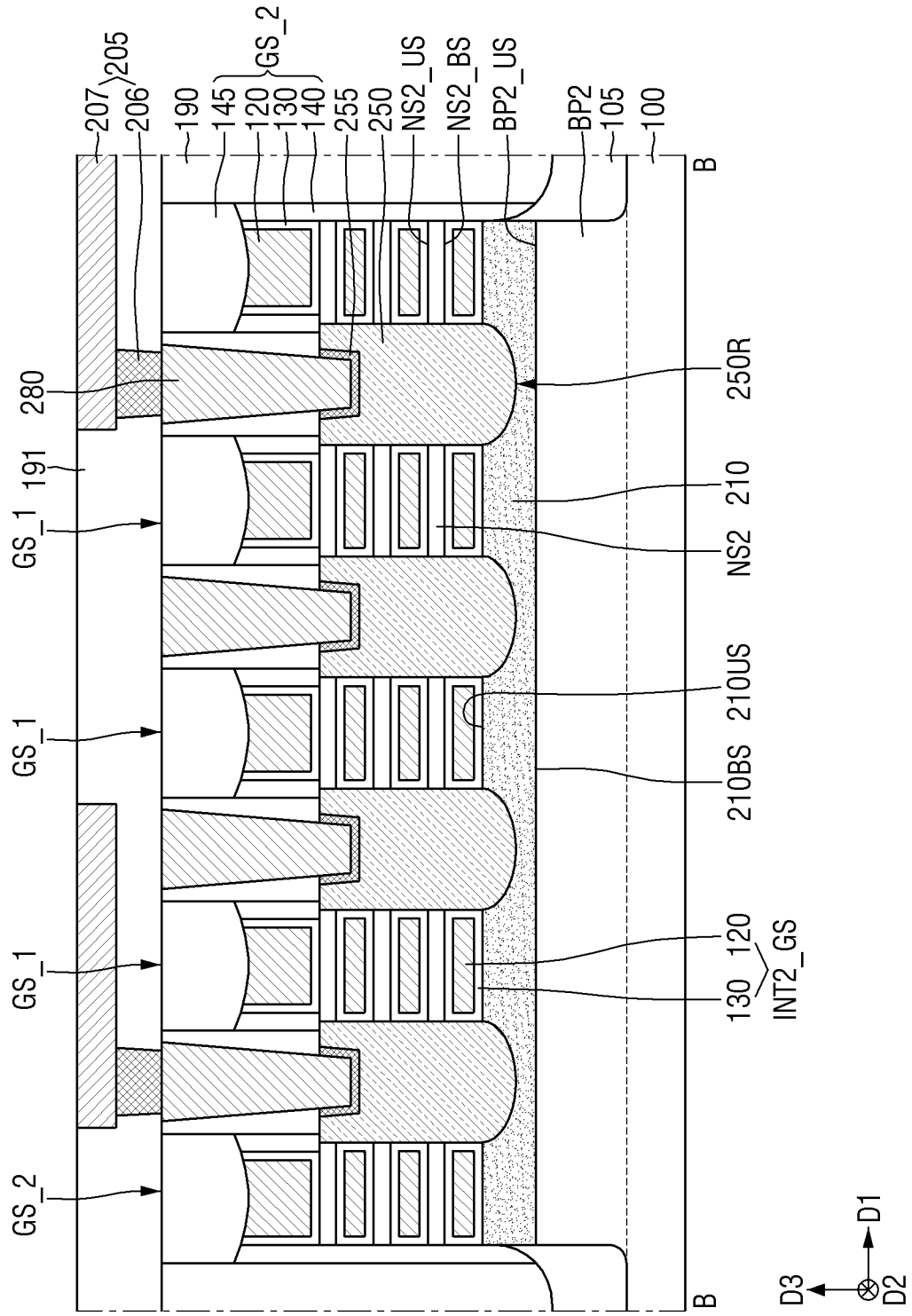


FIG. 4

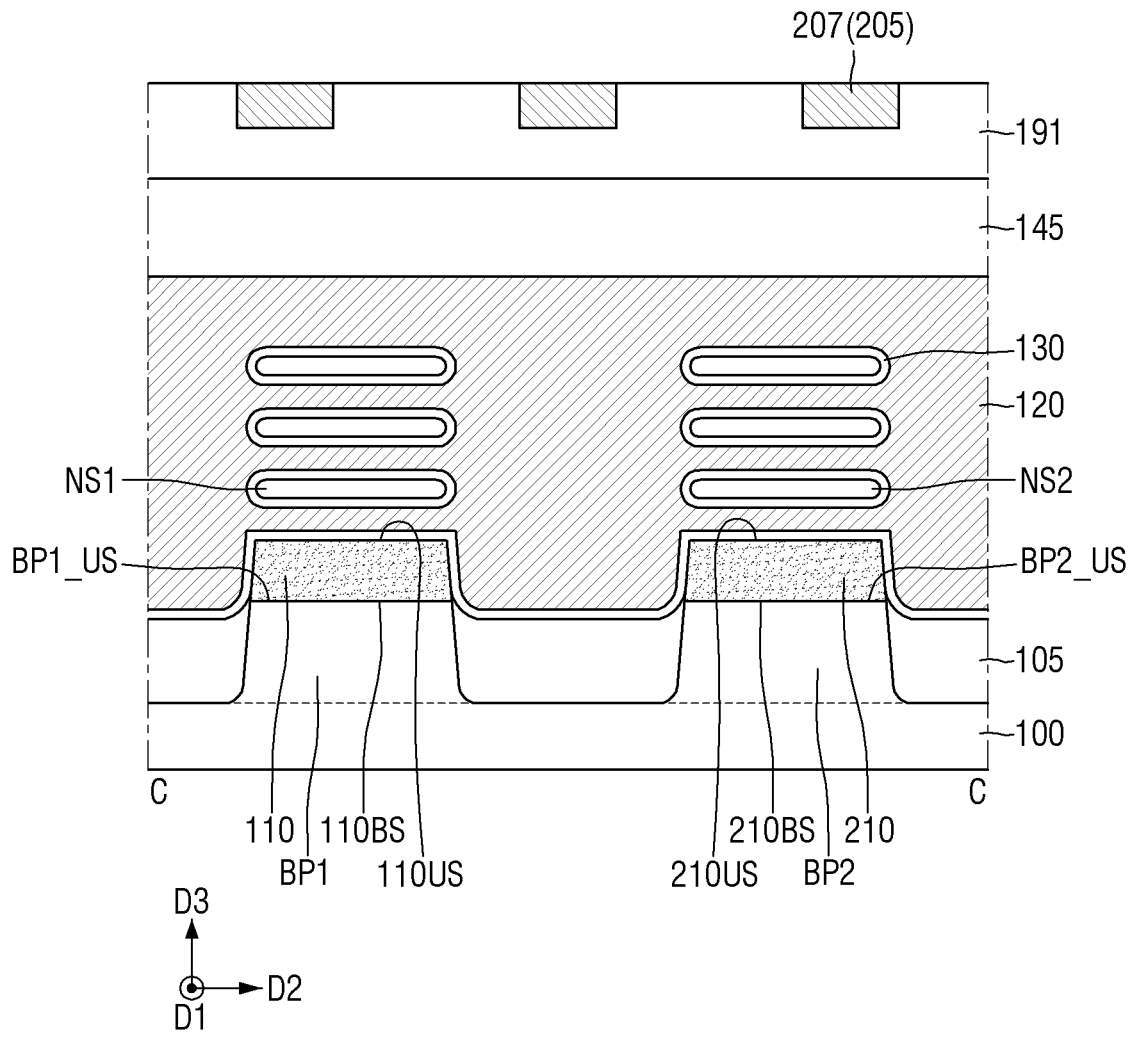


FIG. 5

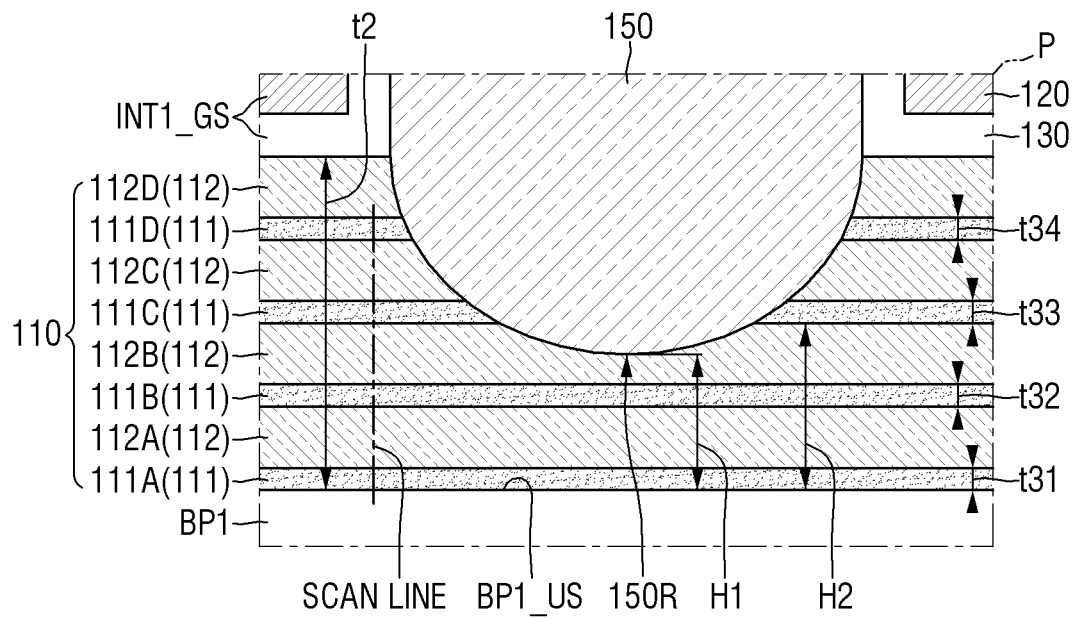


FIG. 6

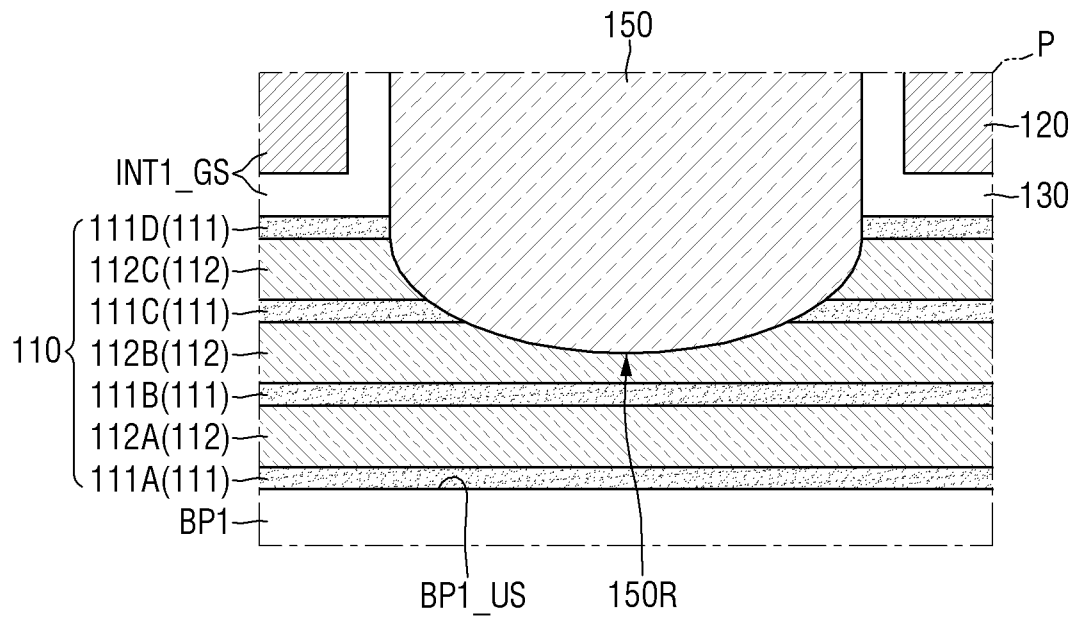


FIG. 7

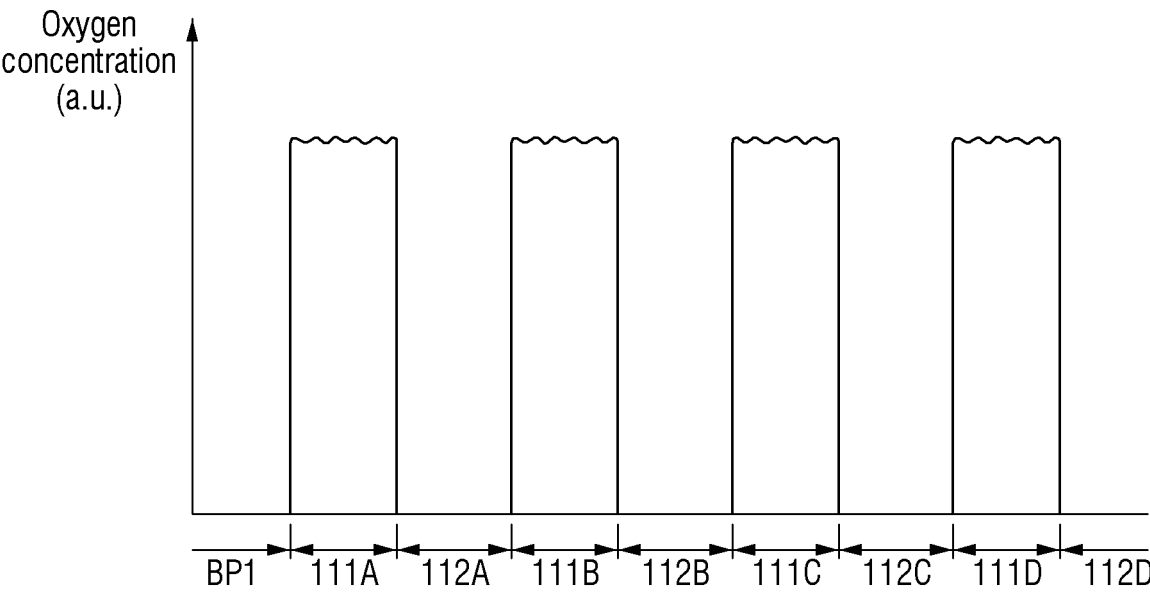


FIG. 8

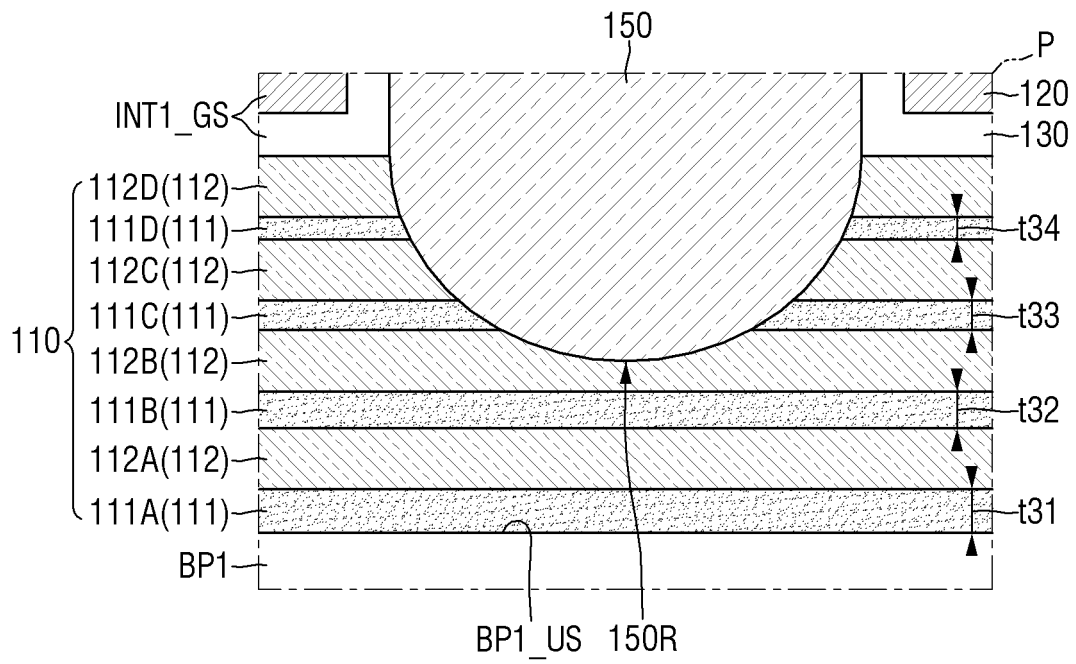


FIG. 9

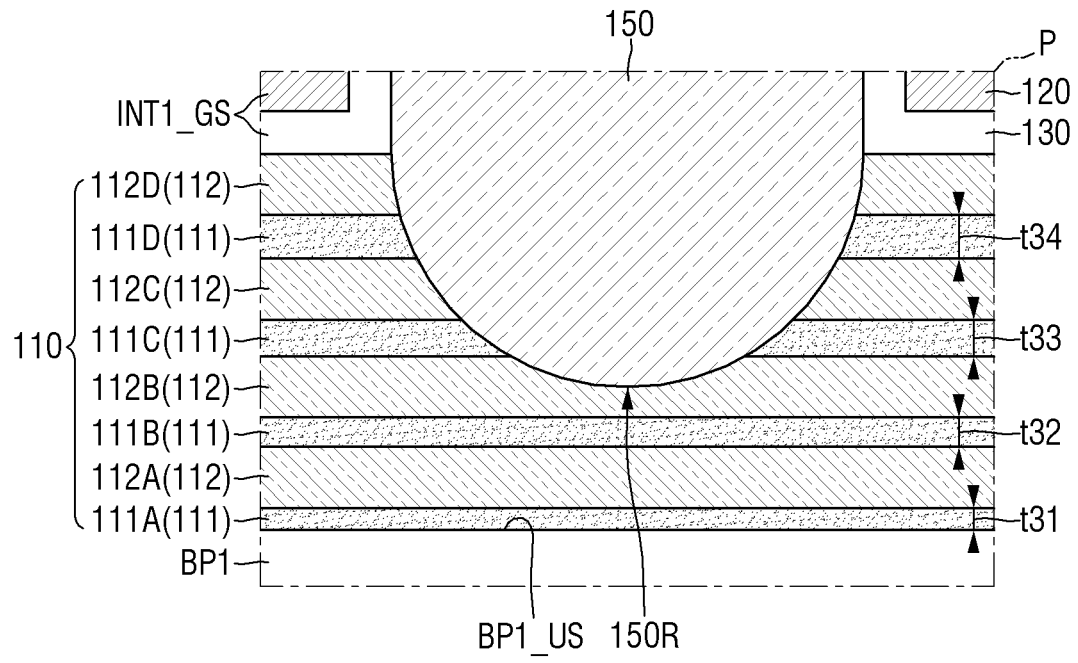


FIG. 10

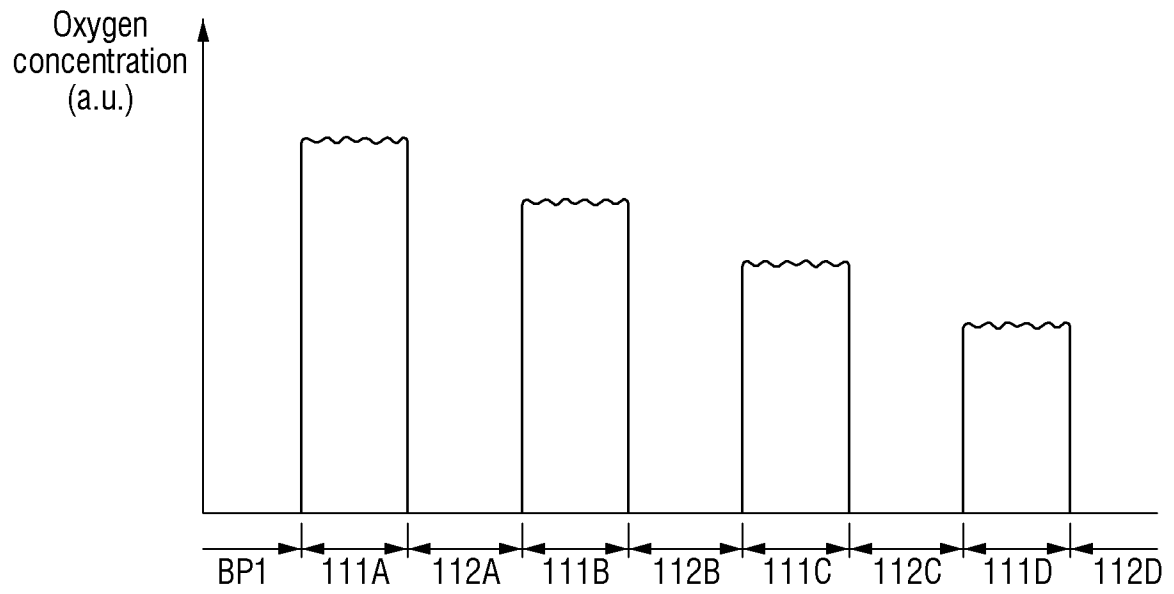


FIG. 11

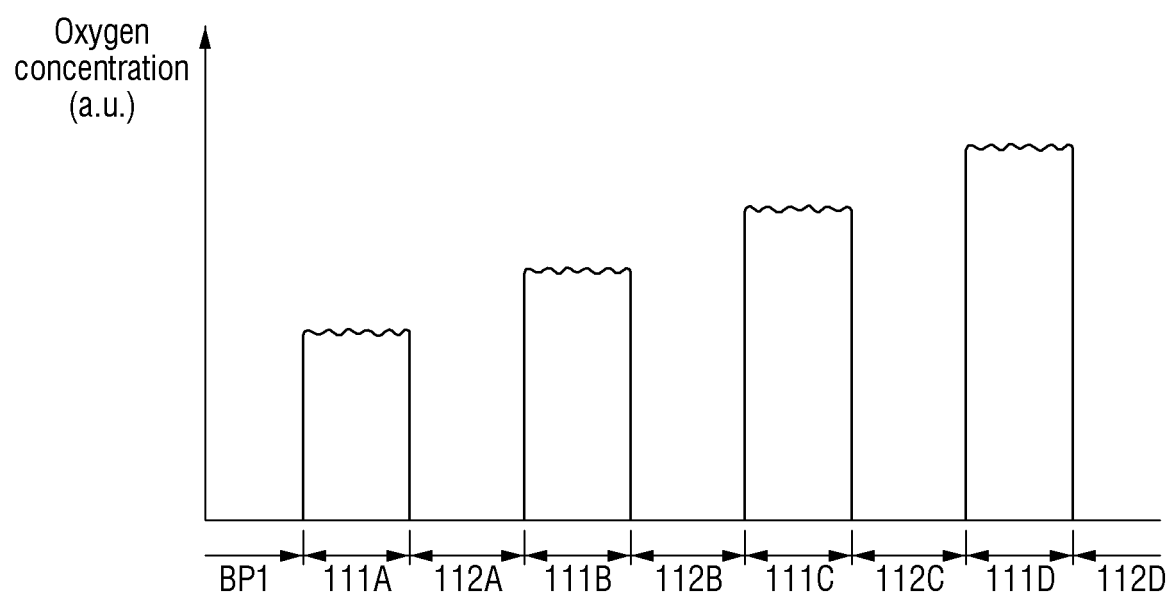


FIG. 12

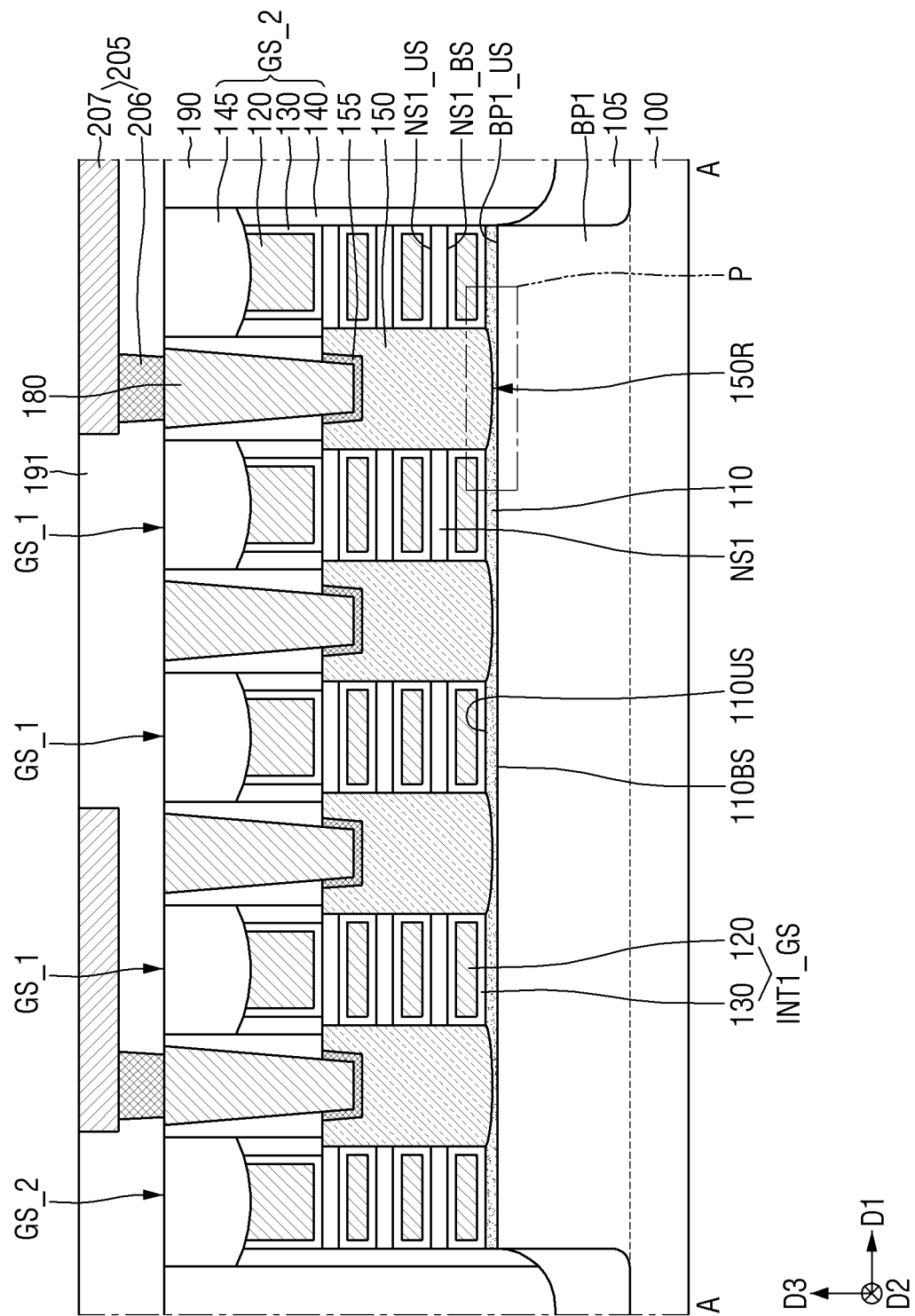


FIG. 13

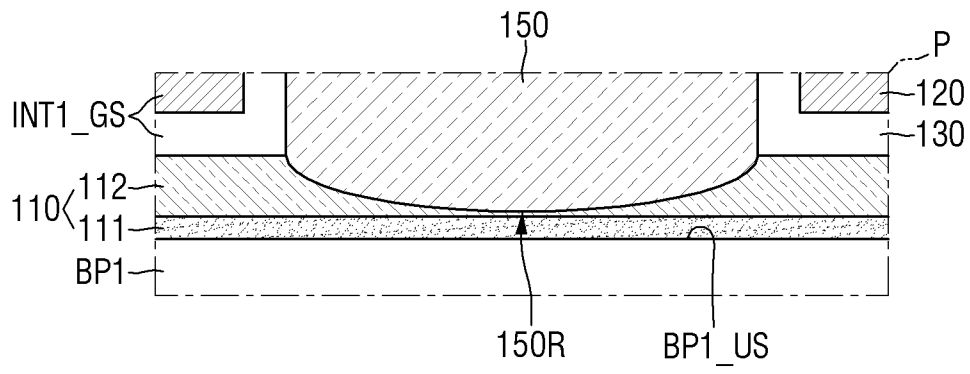


FIG. 14

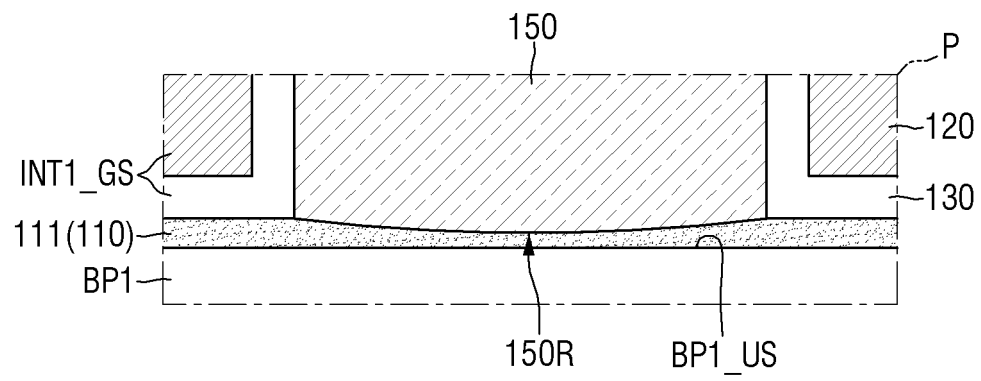


FIG. 15

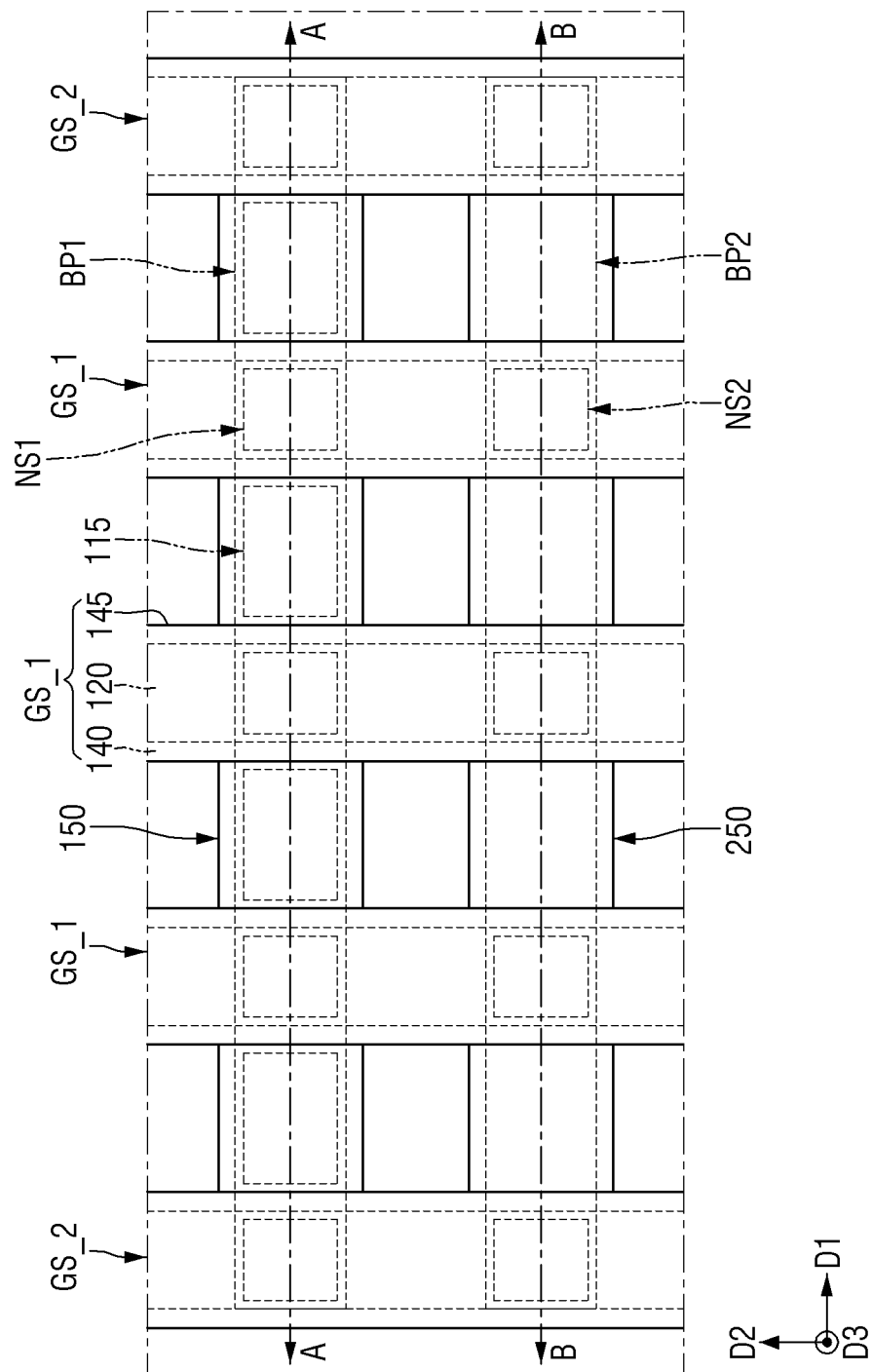


FIG. 16

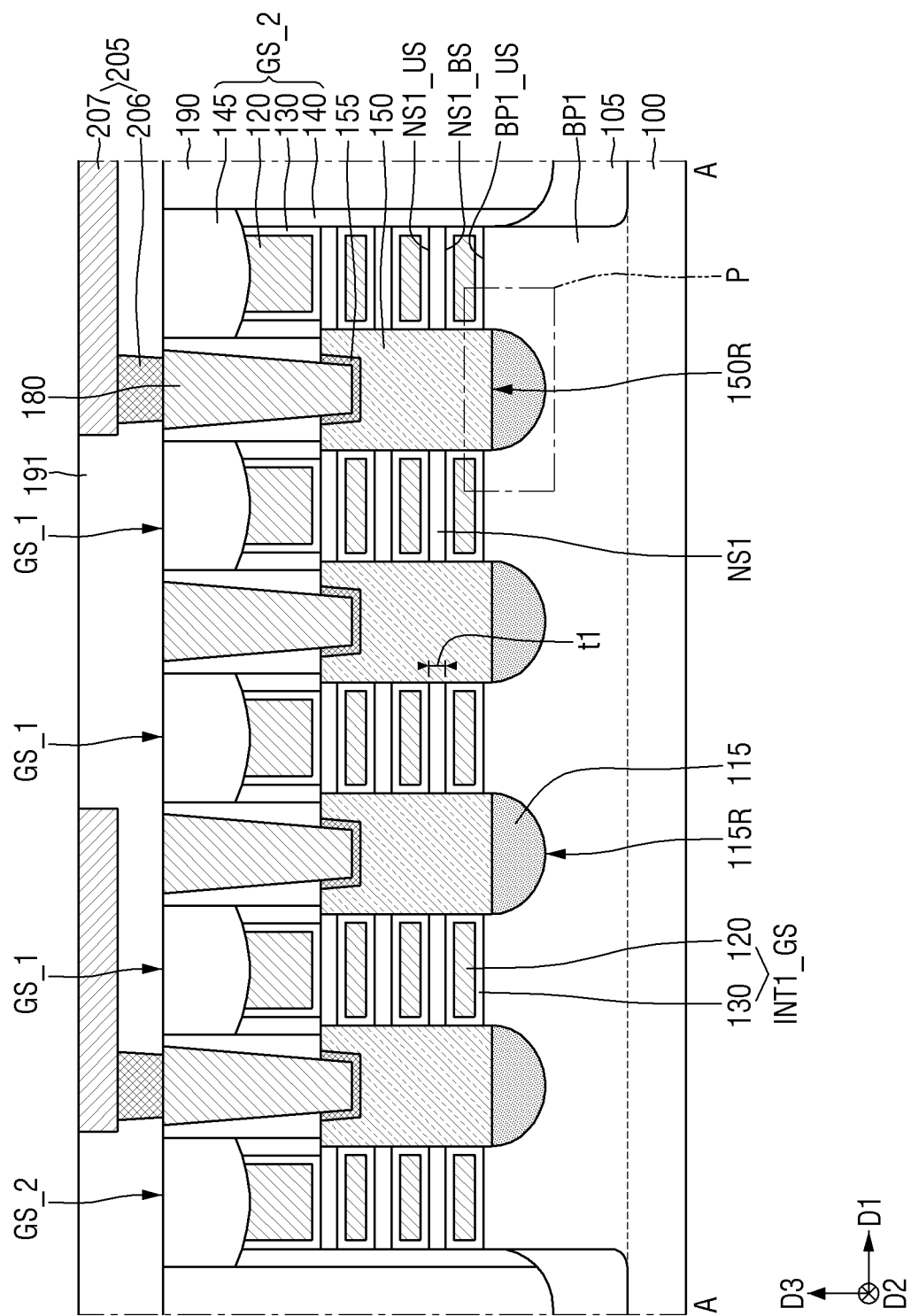


FIG. 17

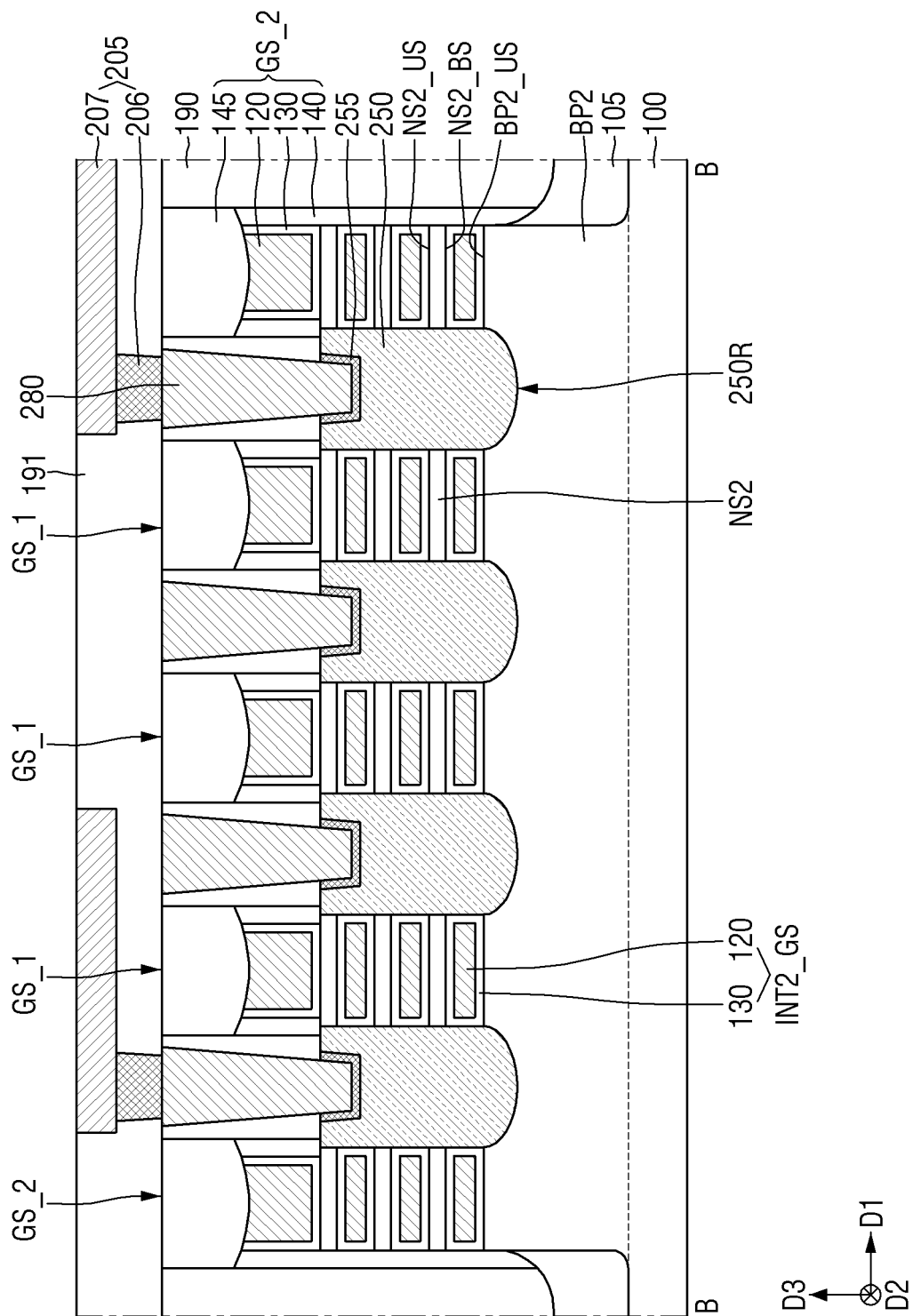


FIG. 18

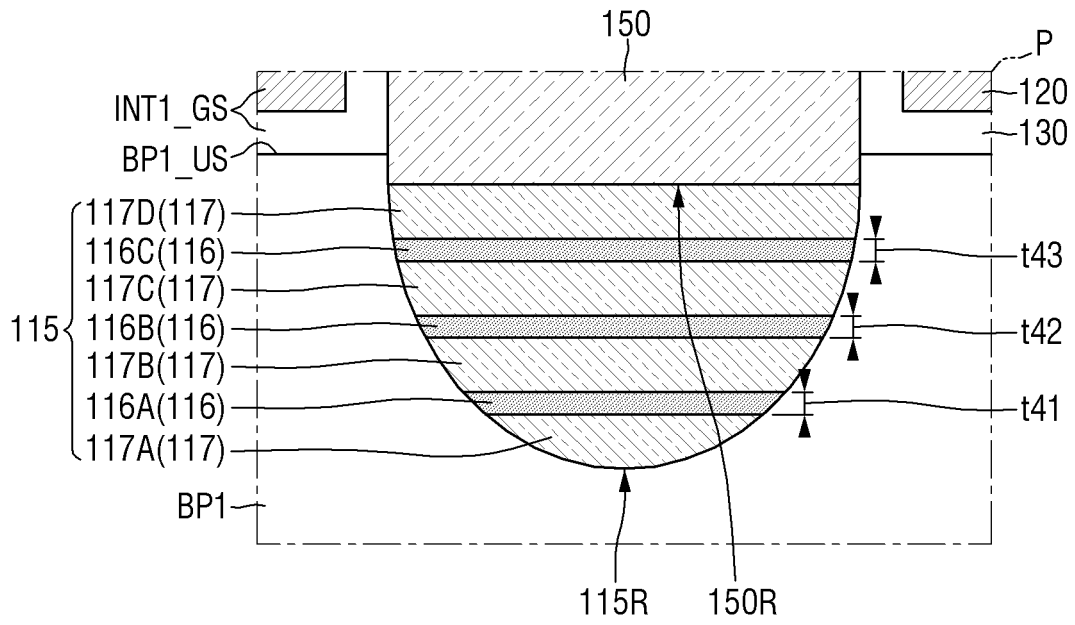


FIG. 19

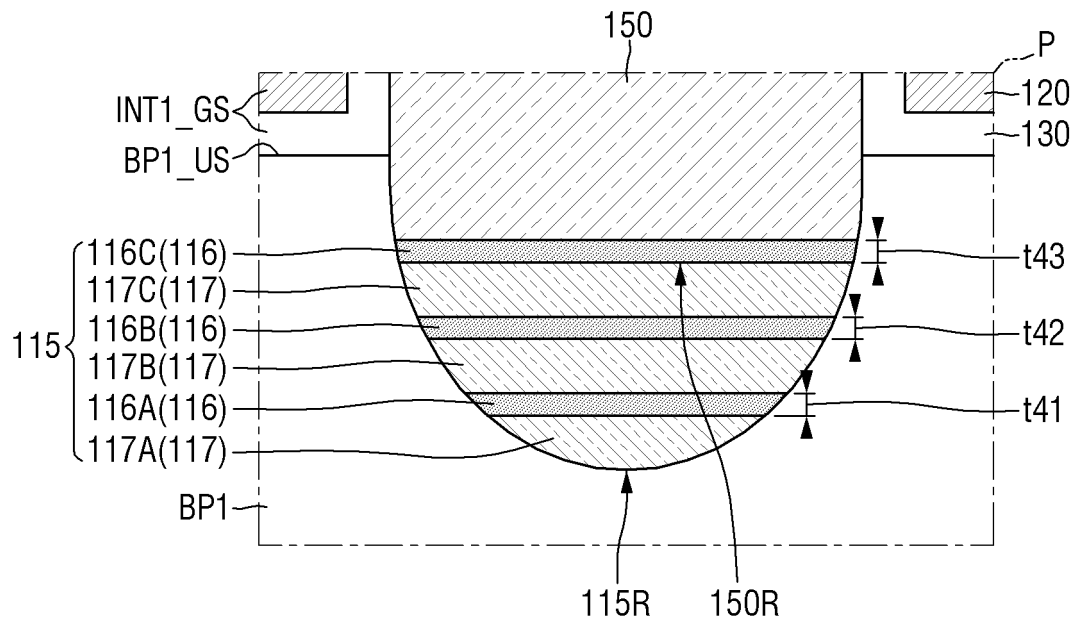


FIG. 20

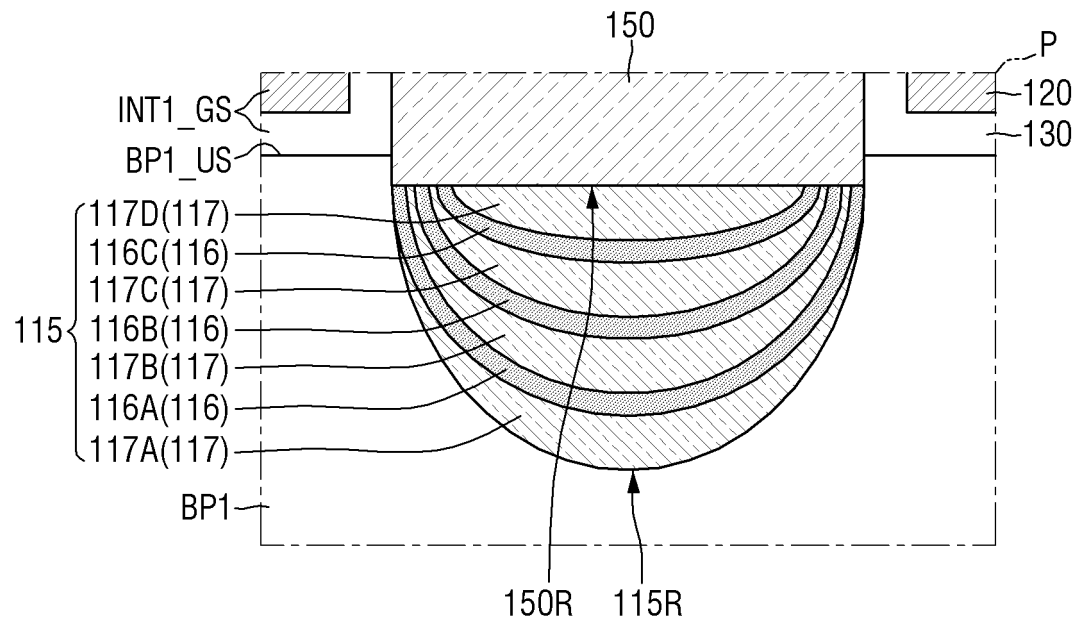


FIG. 21

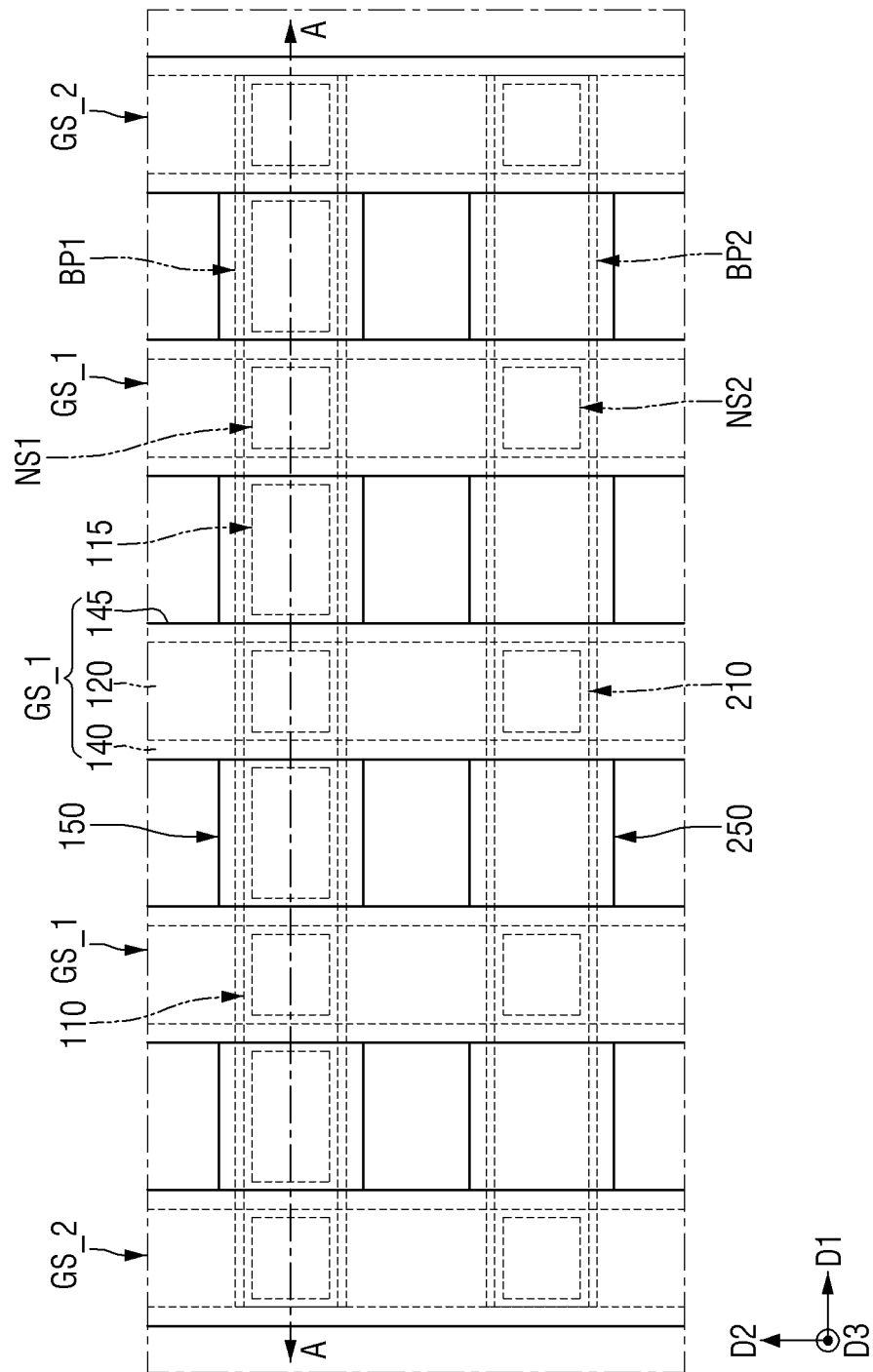


FIG. 22

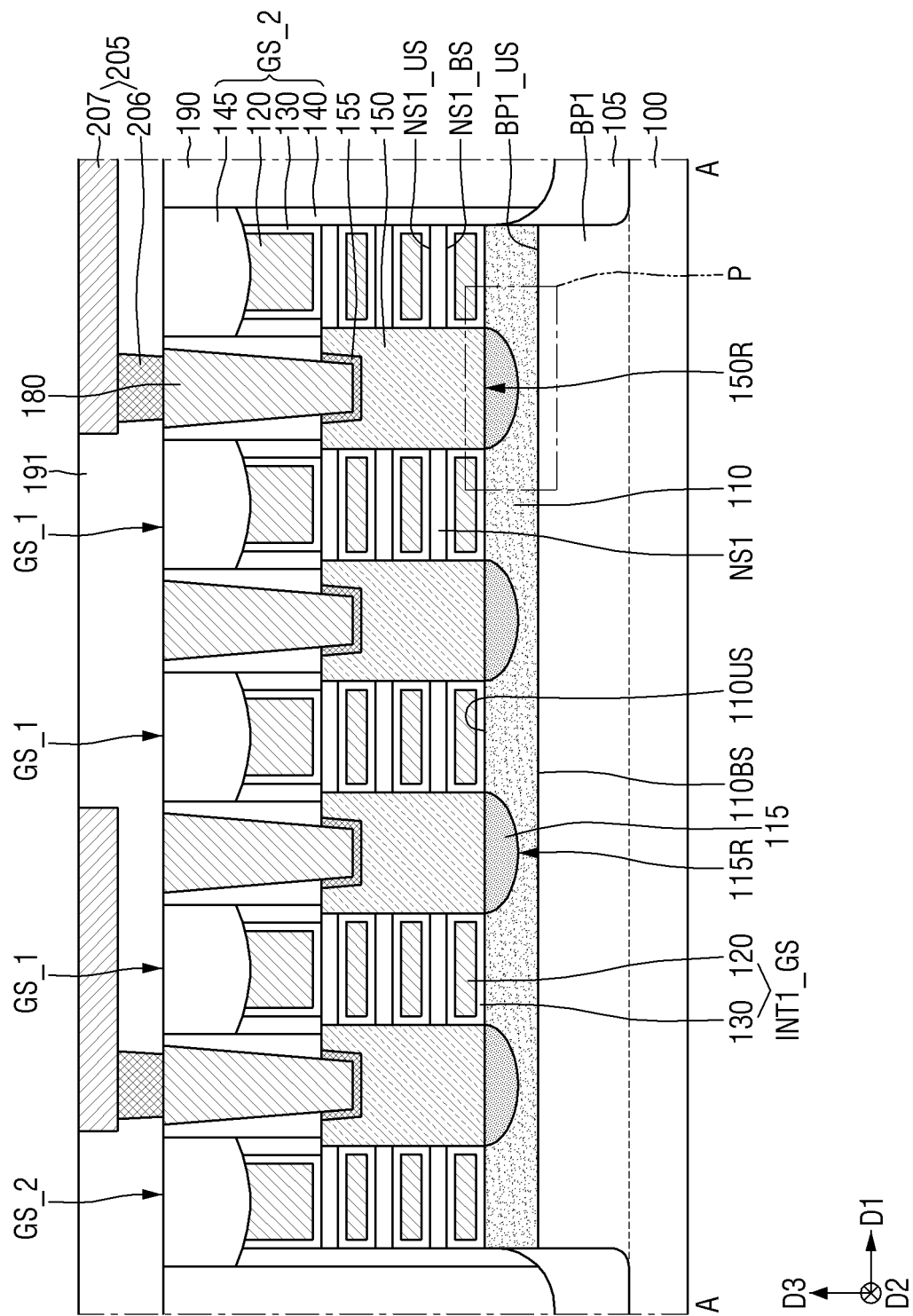


FIG. 23

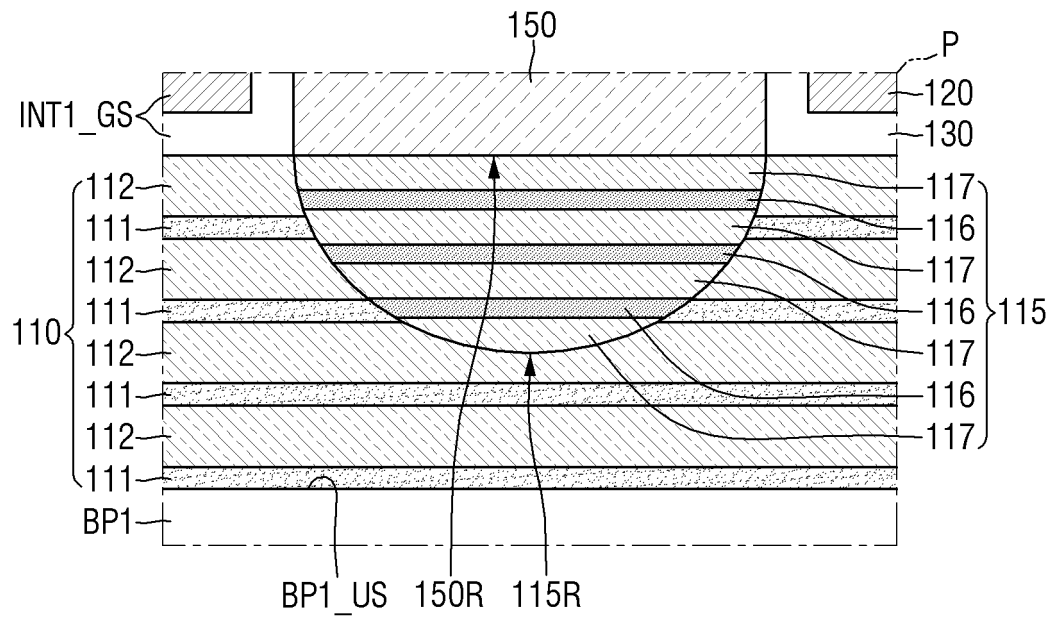


FIG. 24

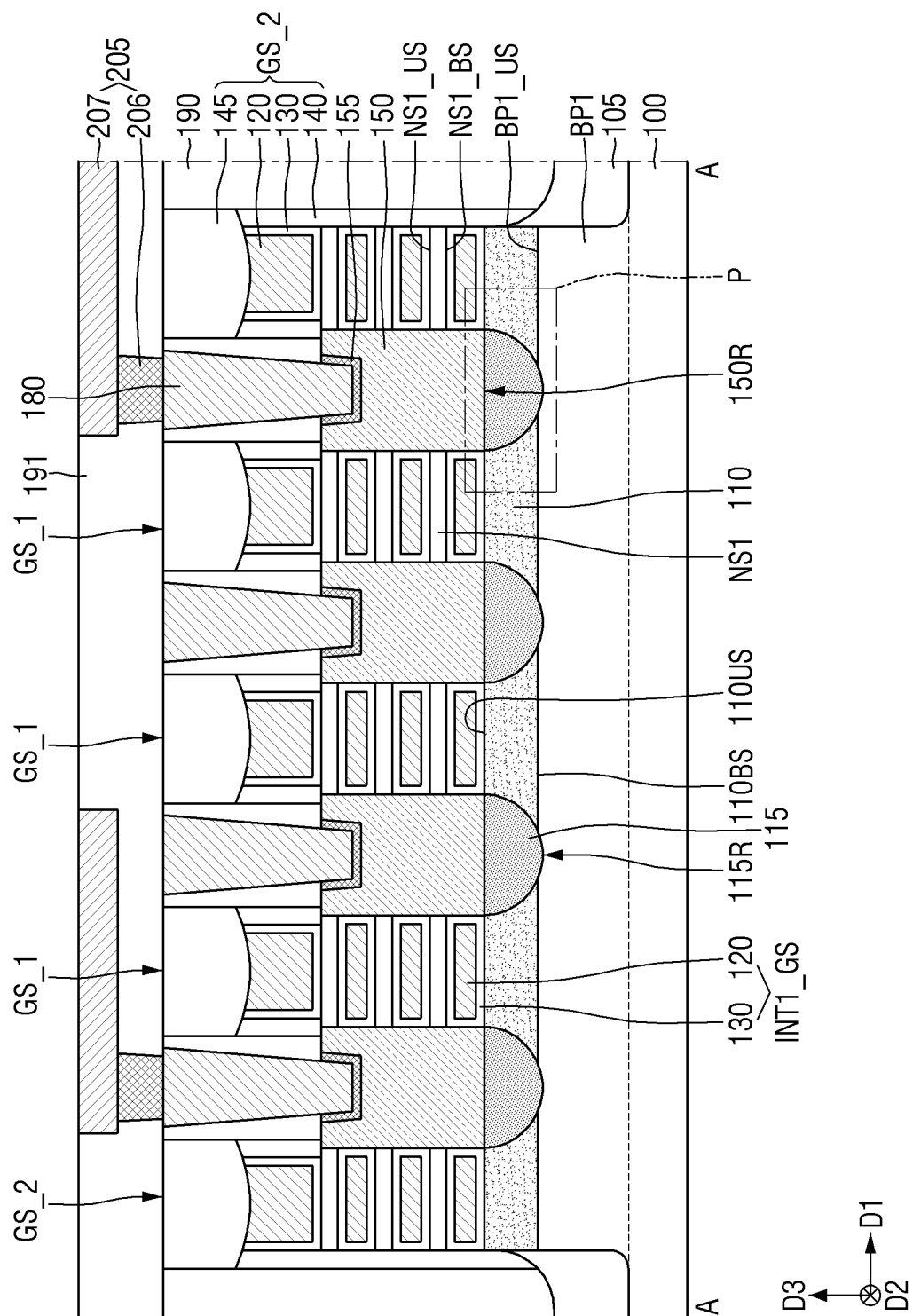


FIG. 25

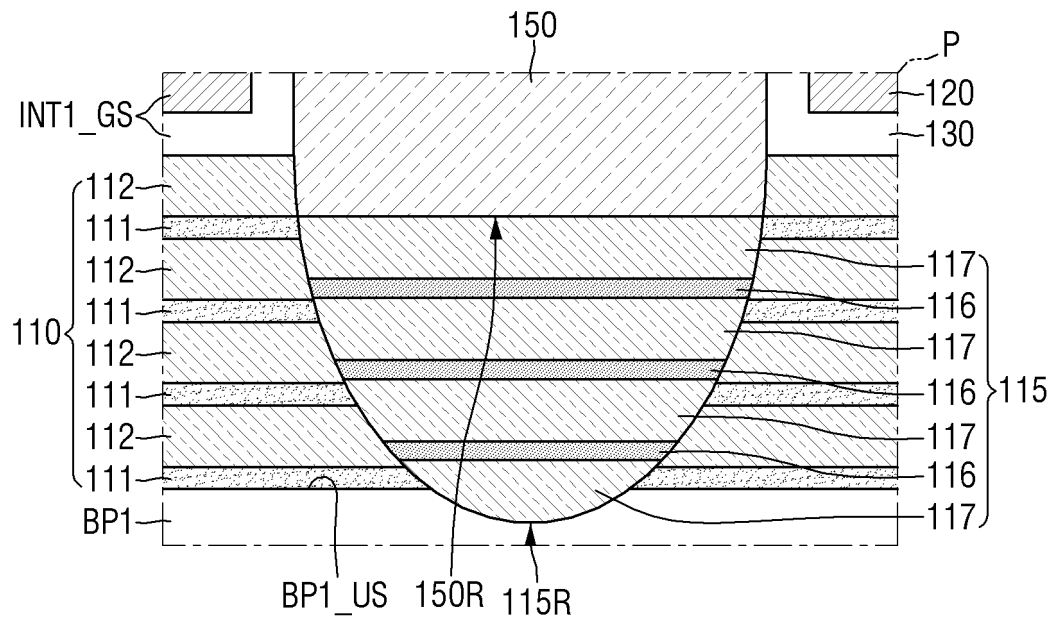


FIG. 26

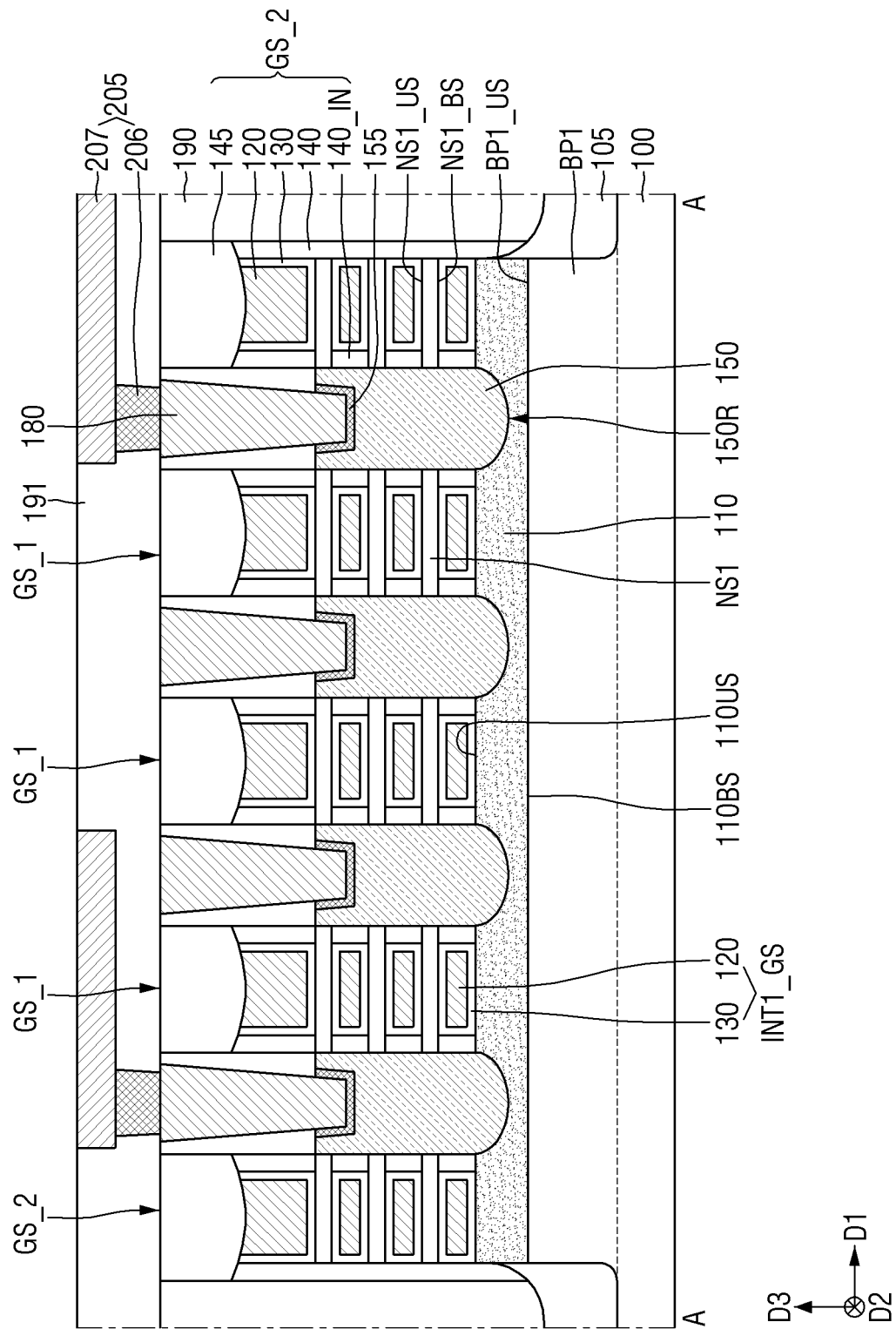


FIG. 27

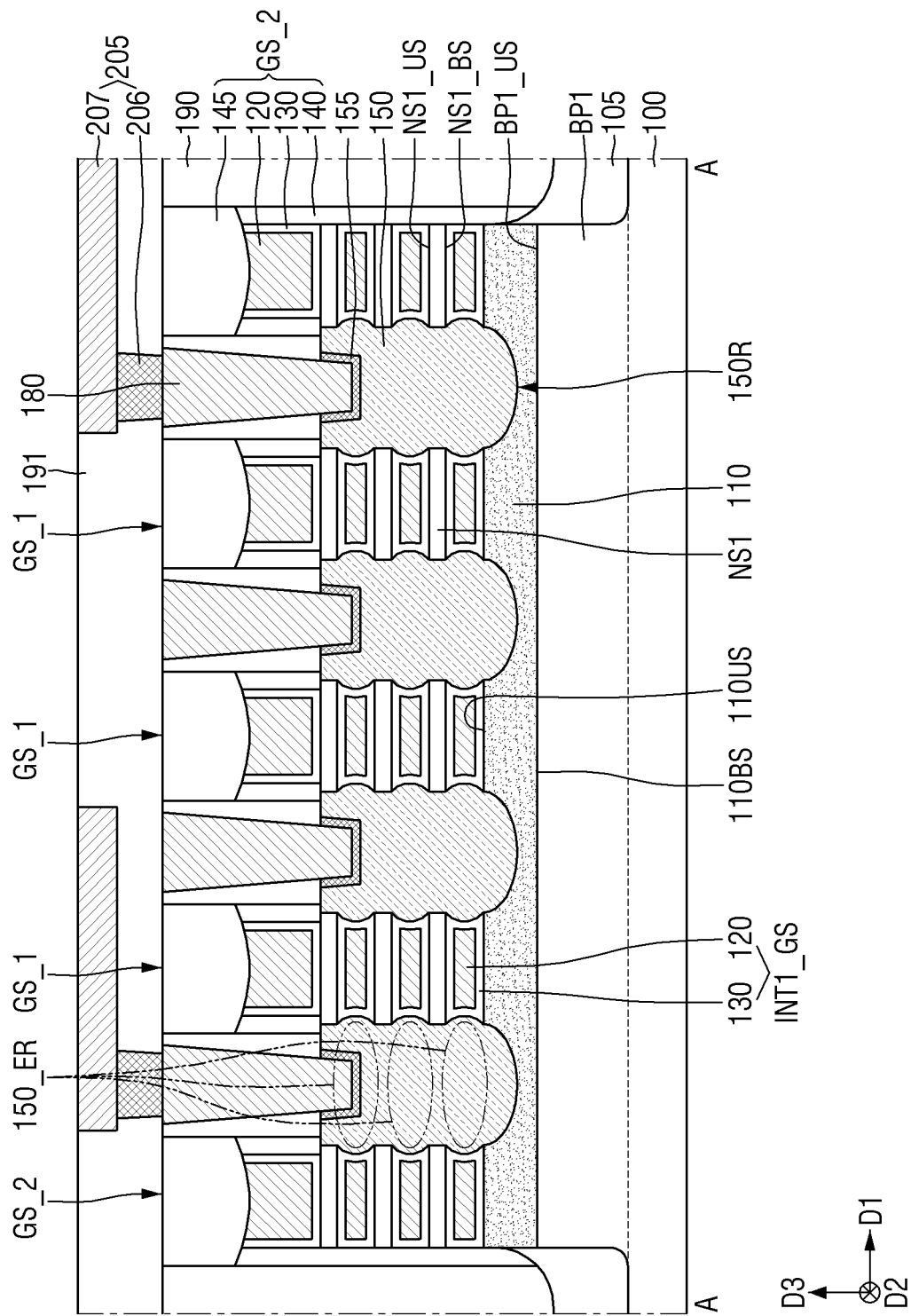


FIG. 28

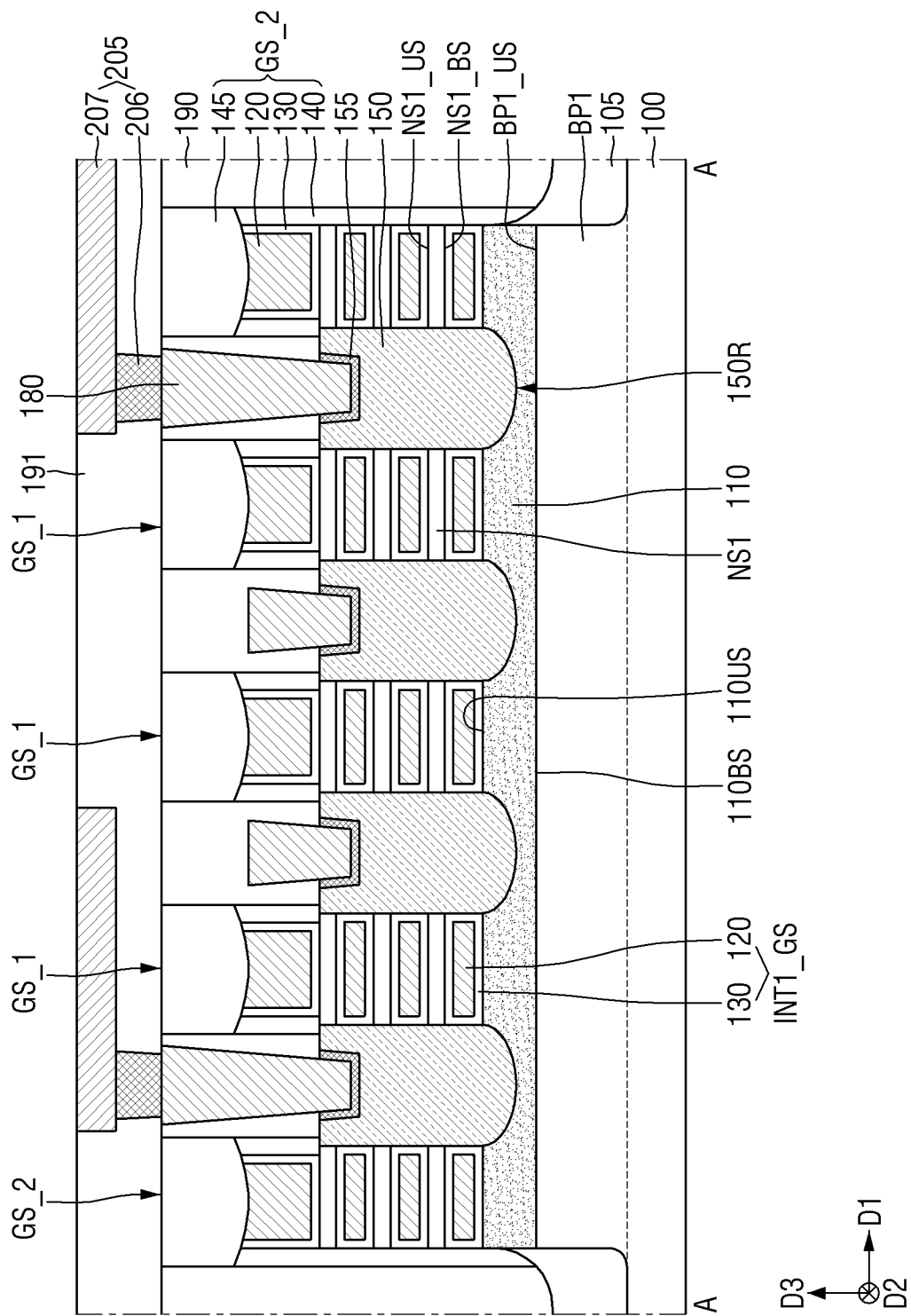


FIG. 29

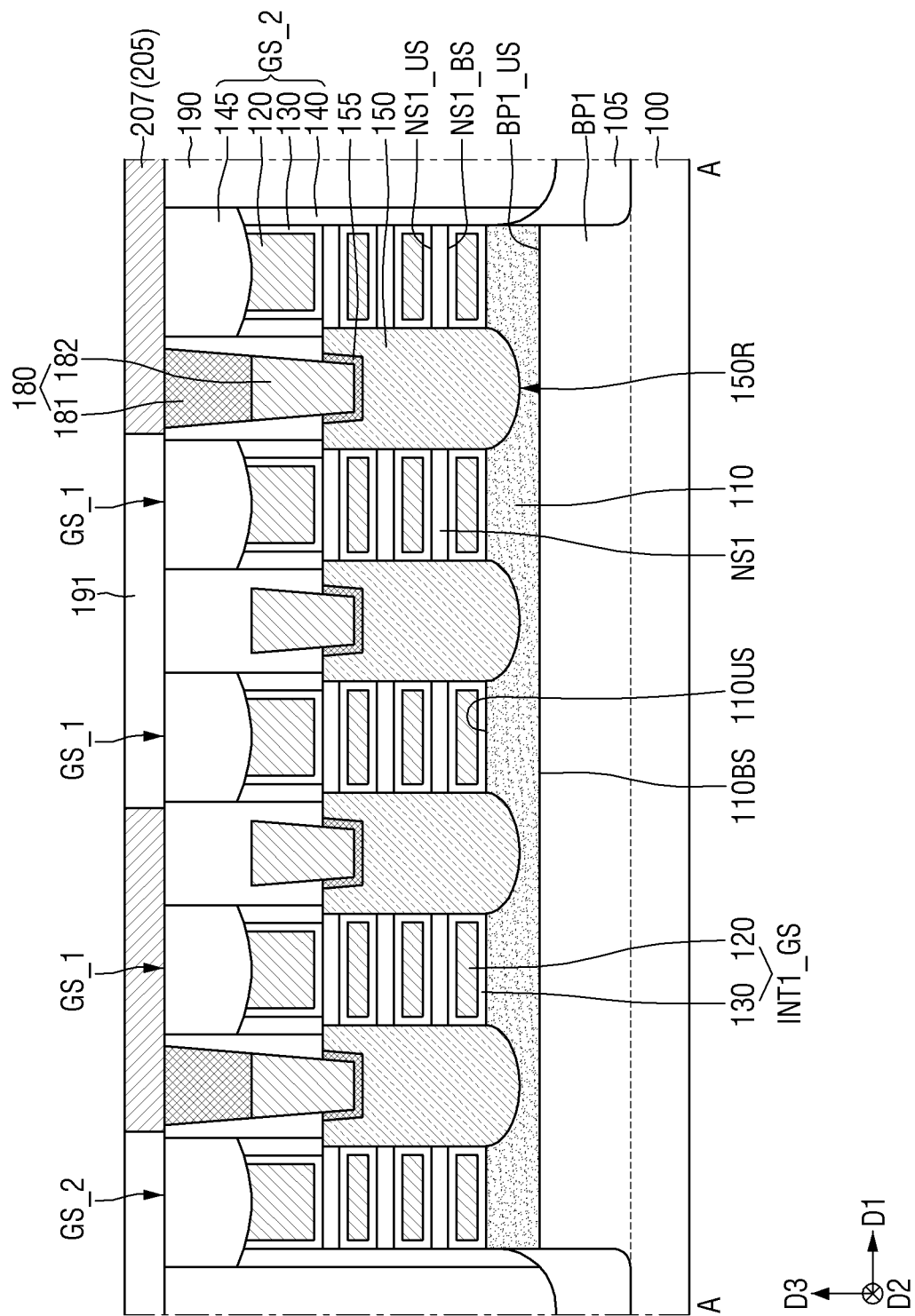


FIG. 30

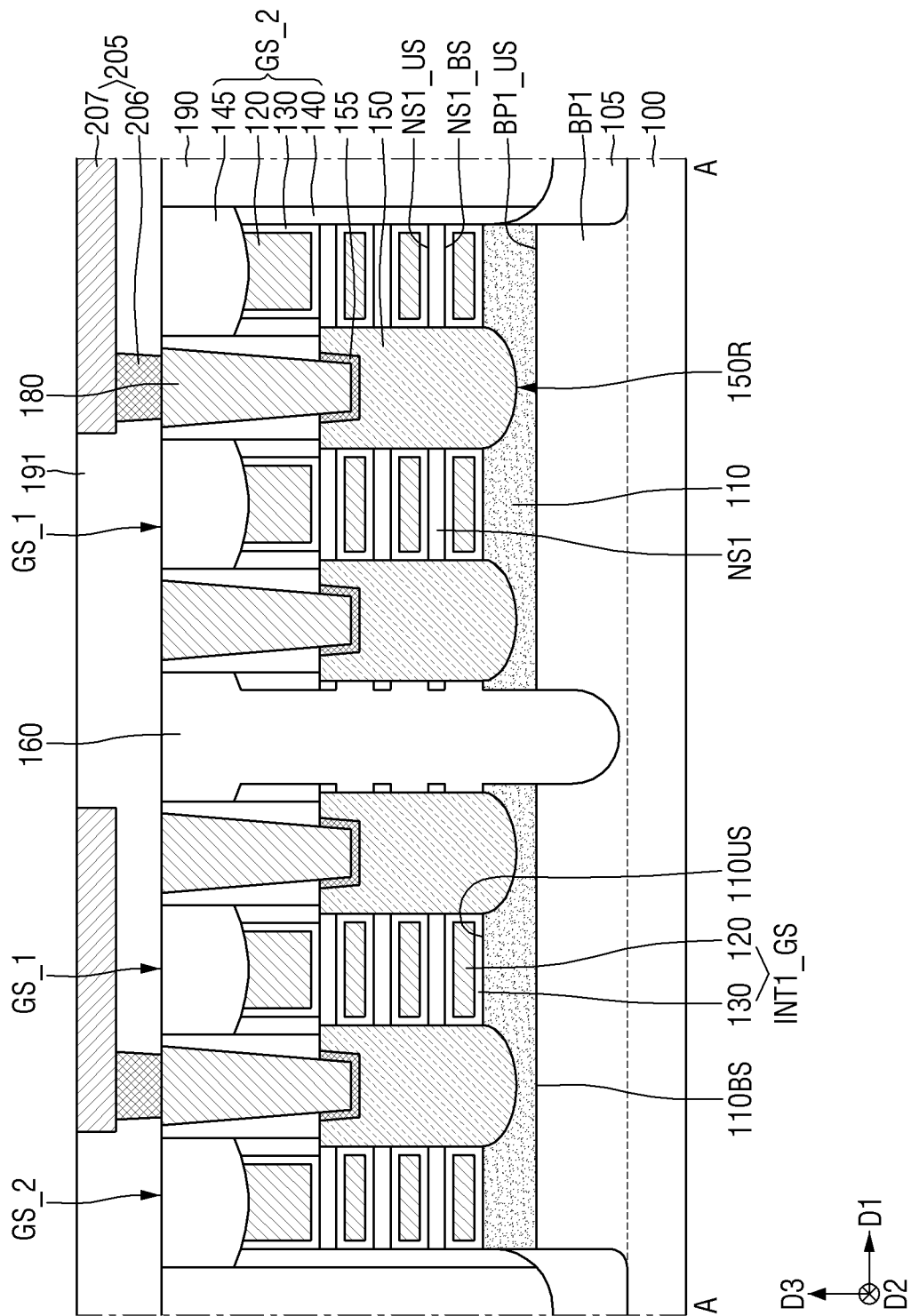


FIG. 31

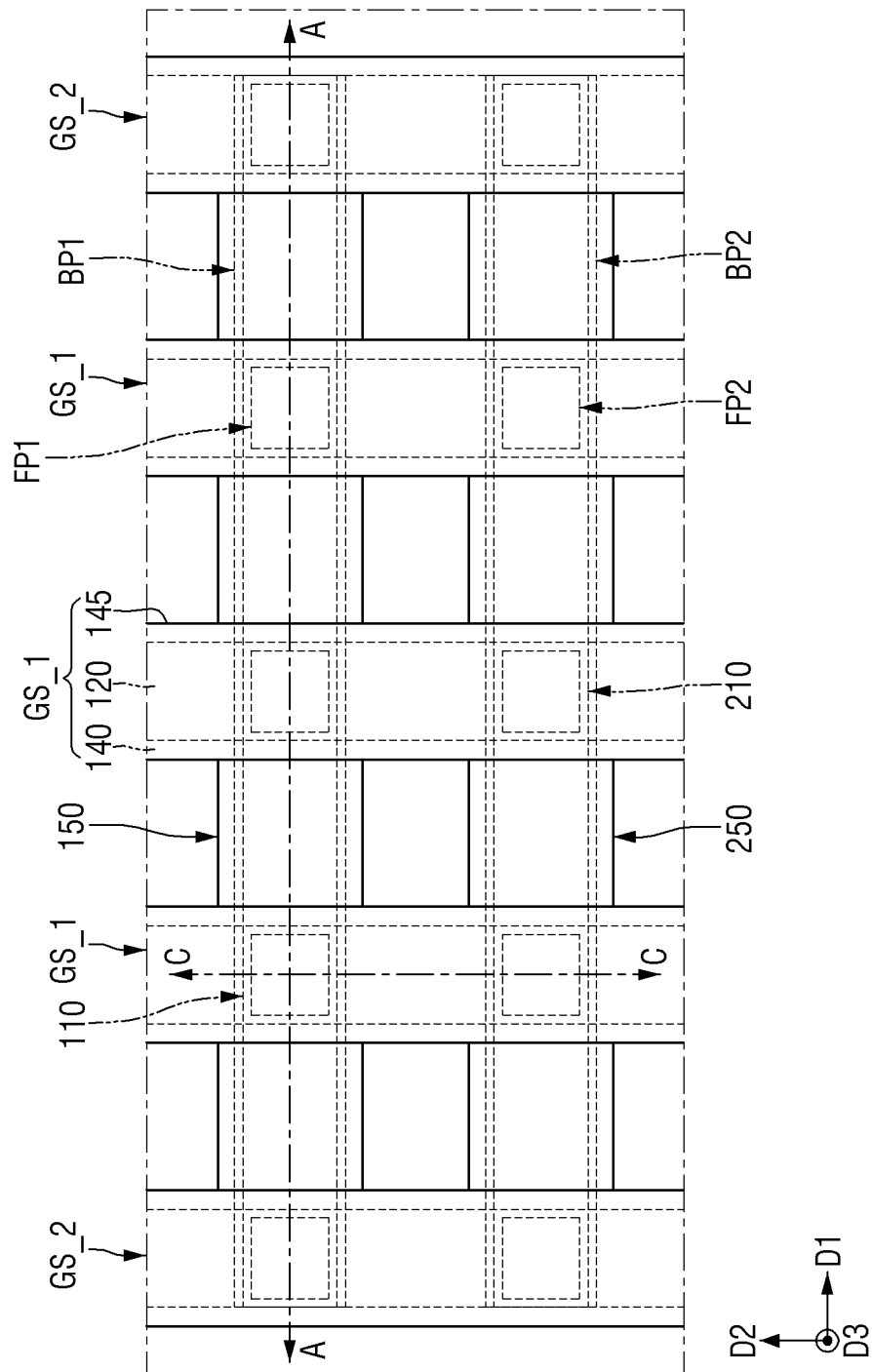


FIG. 32

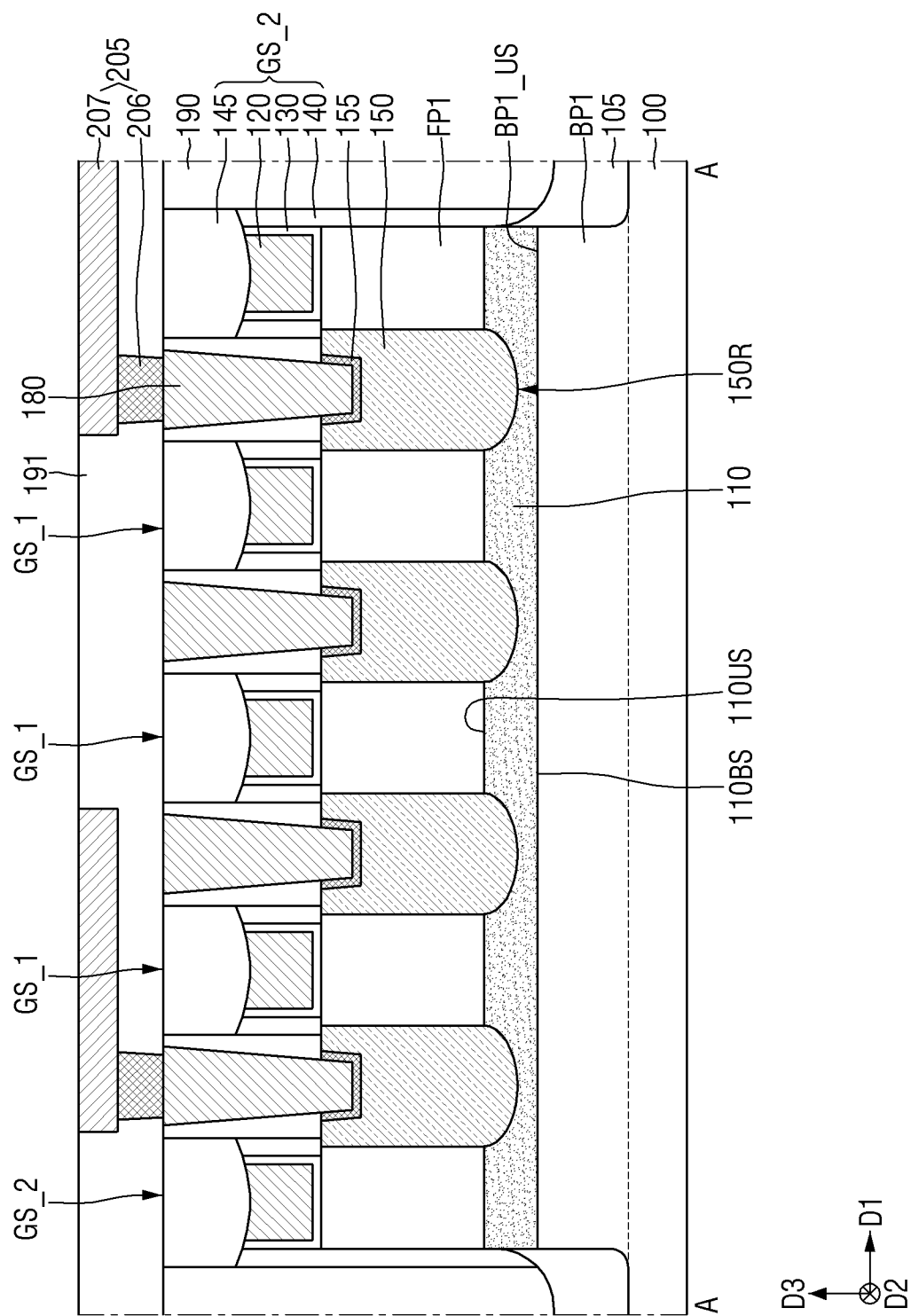


FIG. 33

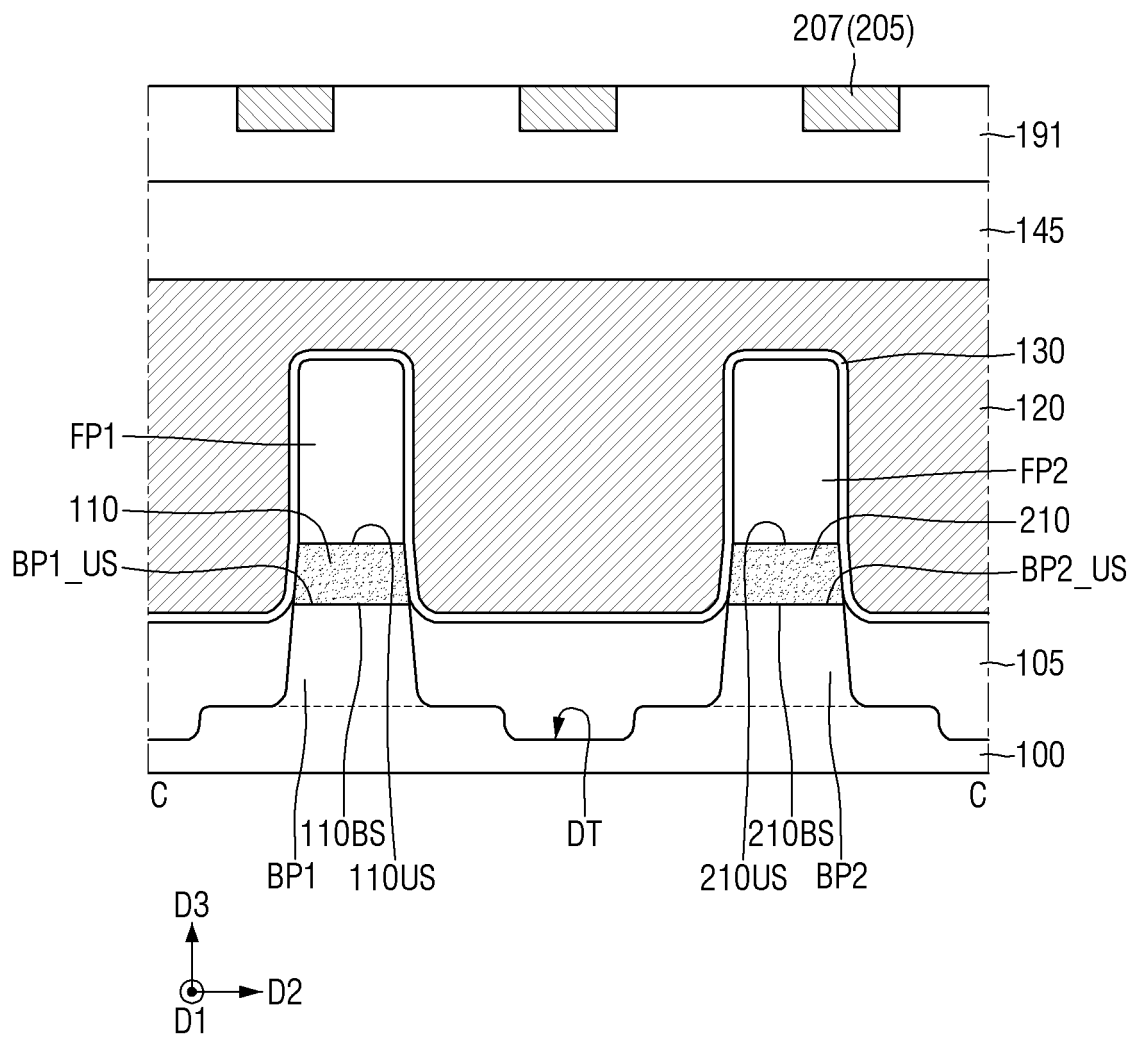


FIG. 34

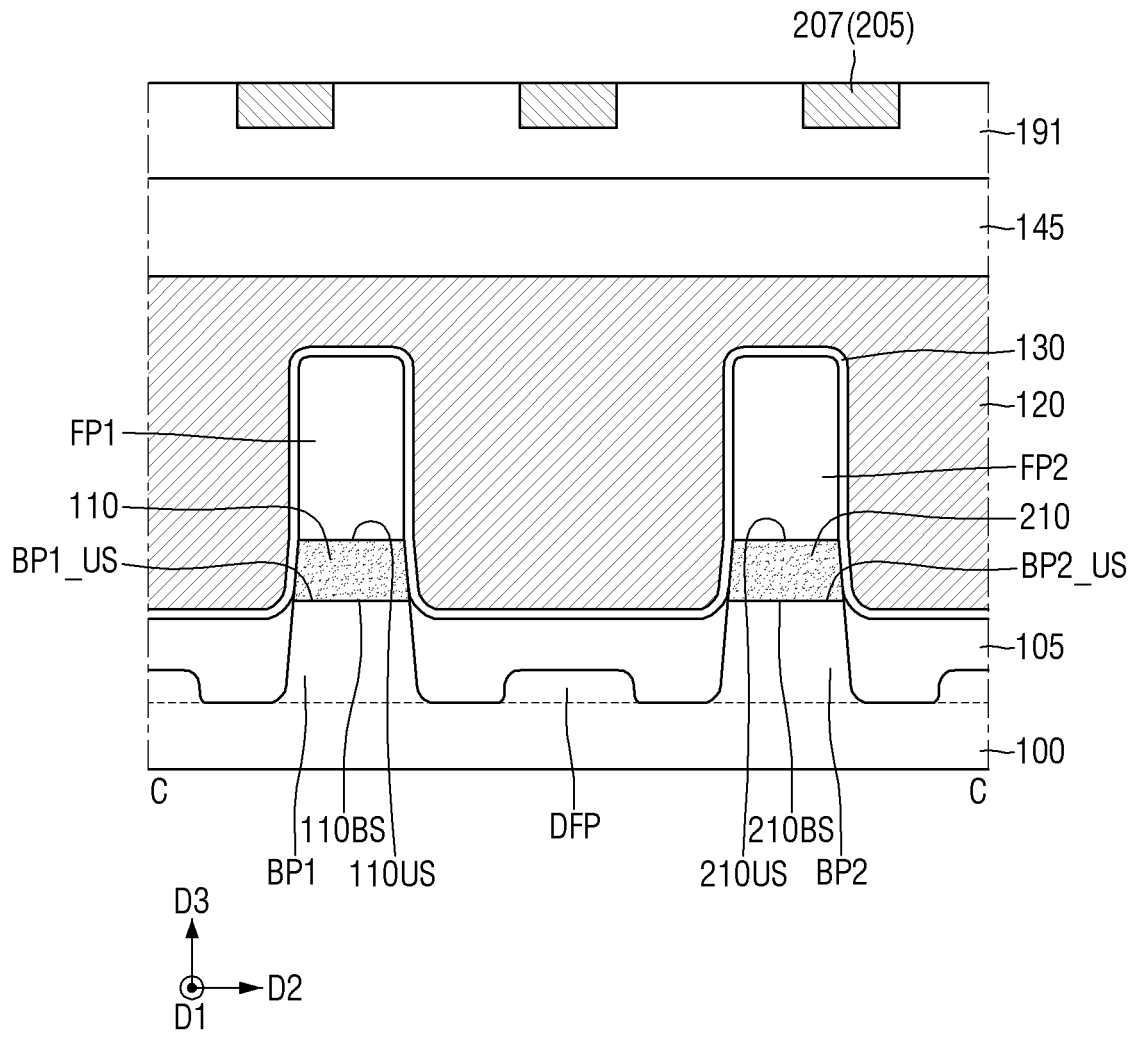


FIG. 35

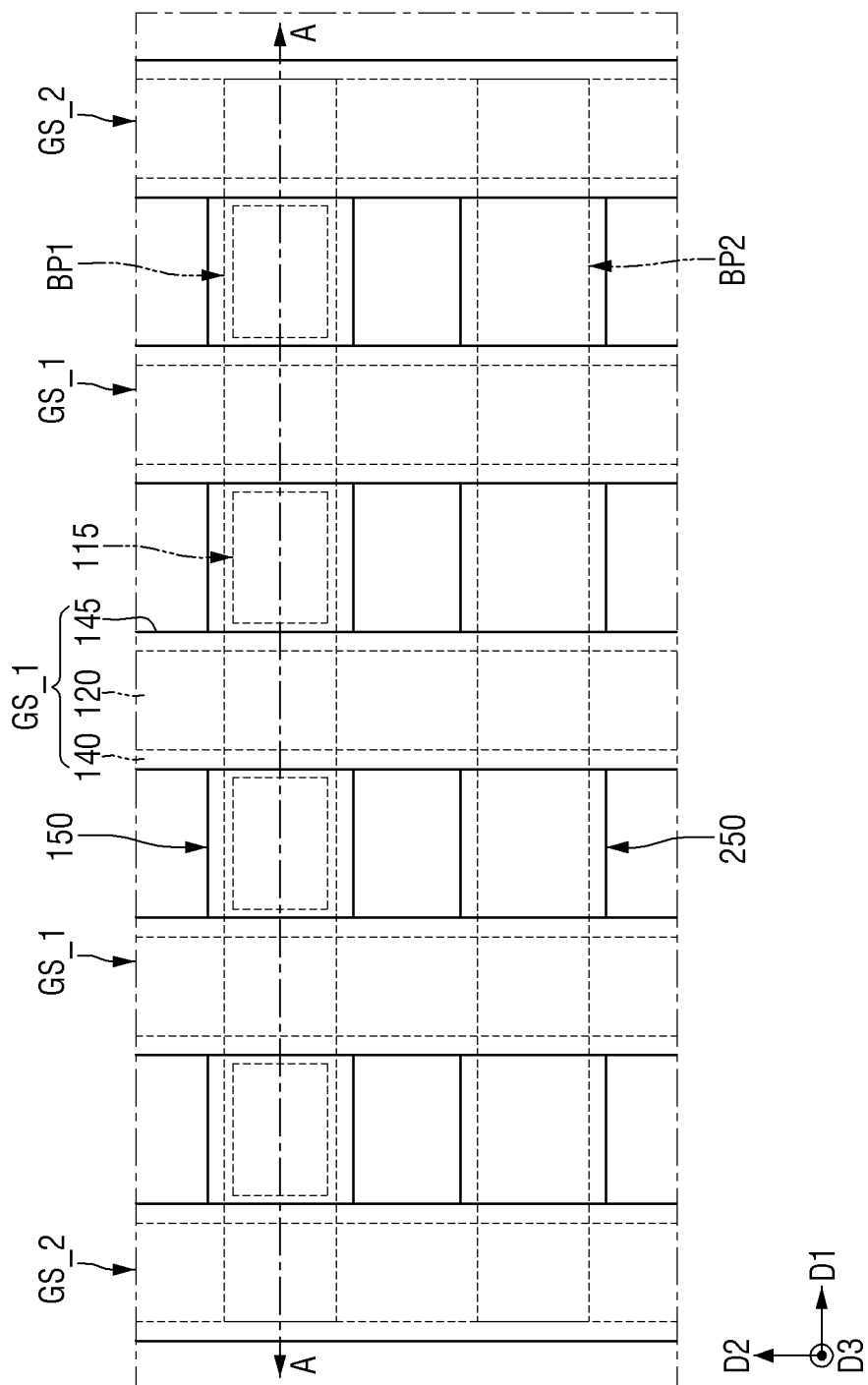


FIG. 36

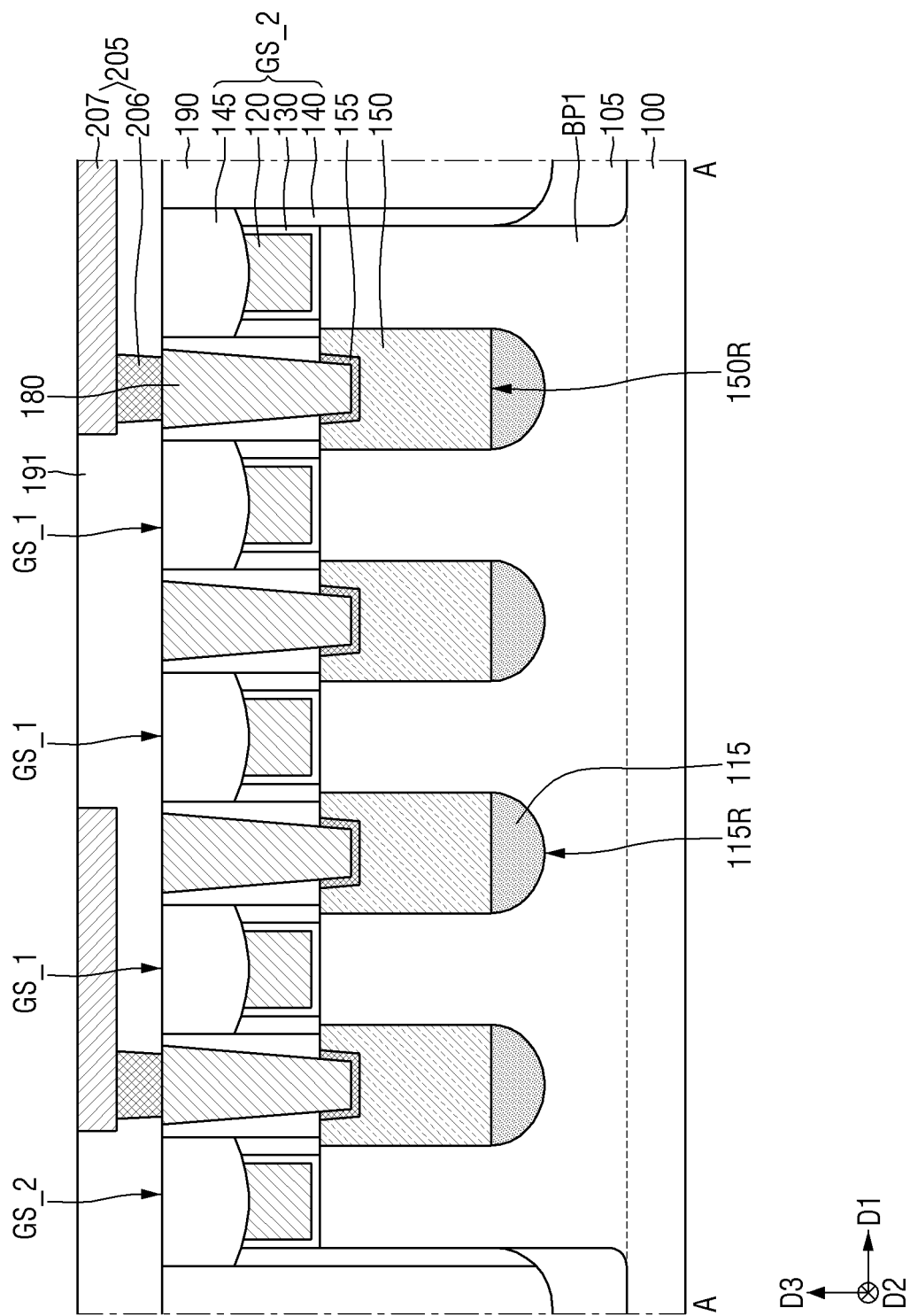


FIG. 37

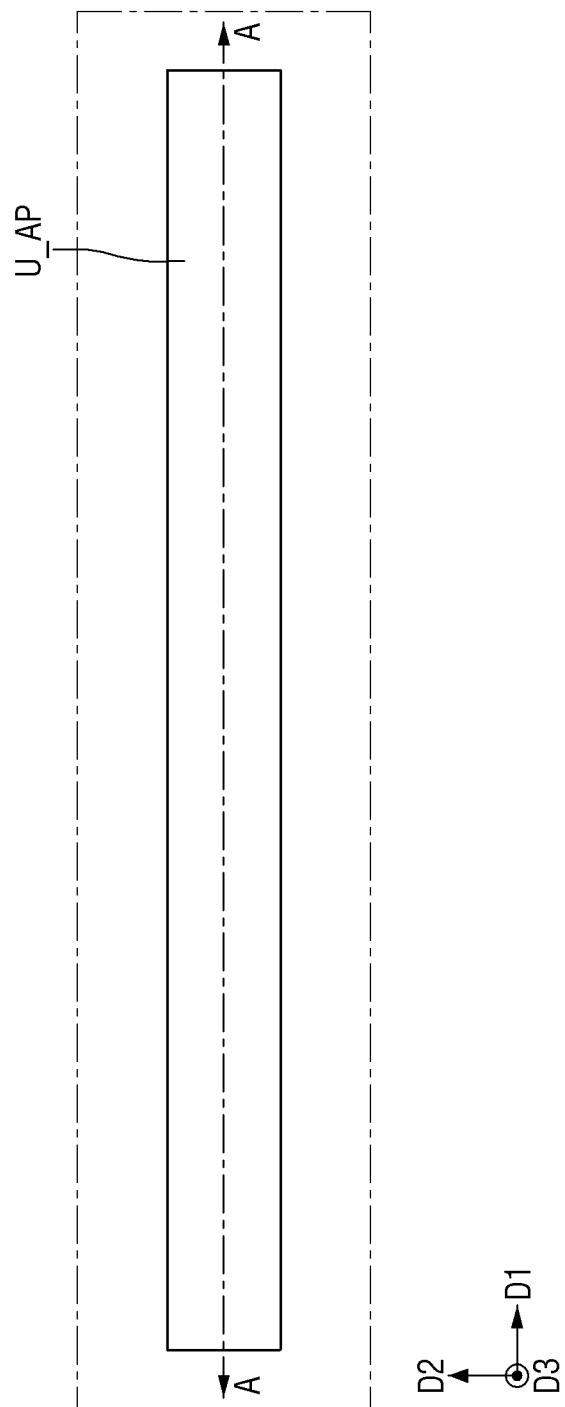


FIG. 38

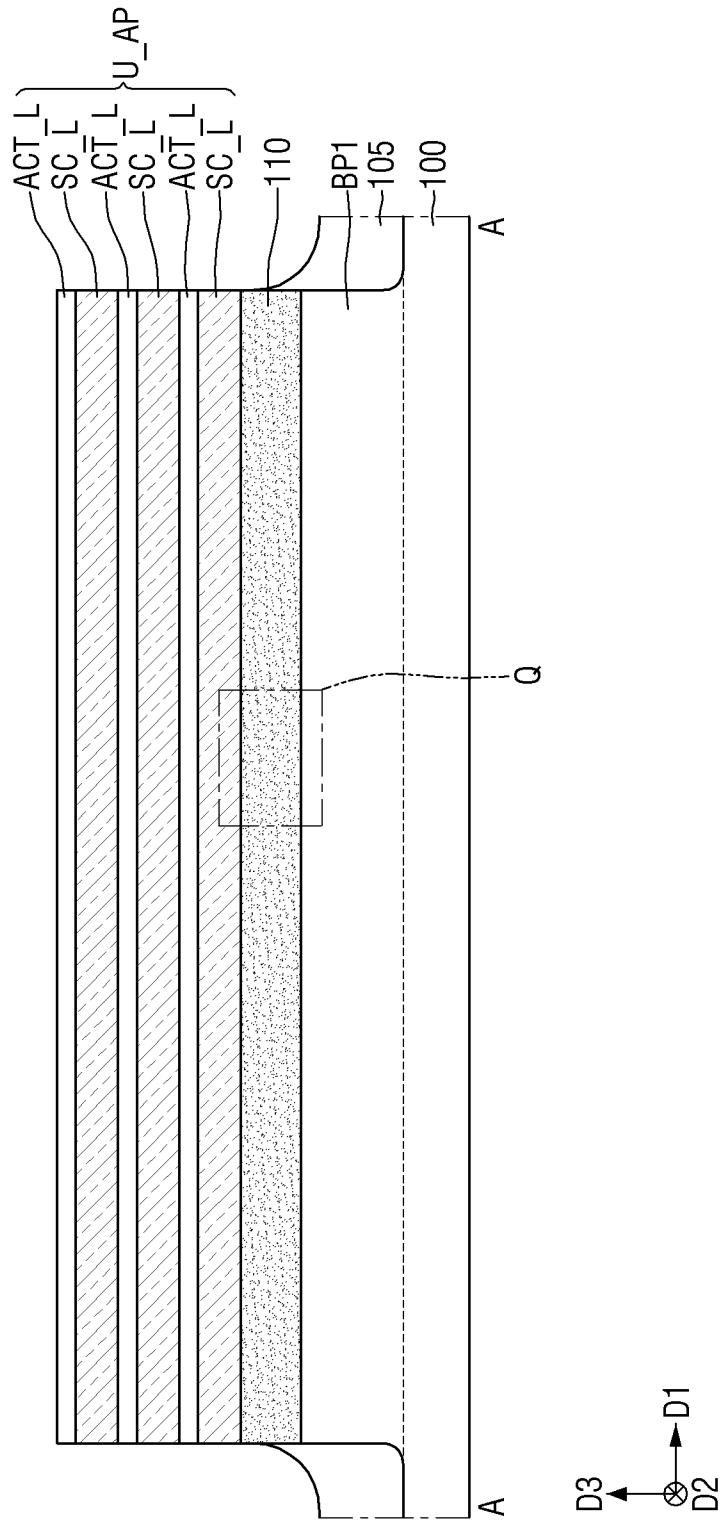


FIG. 39

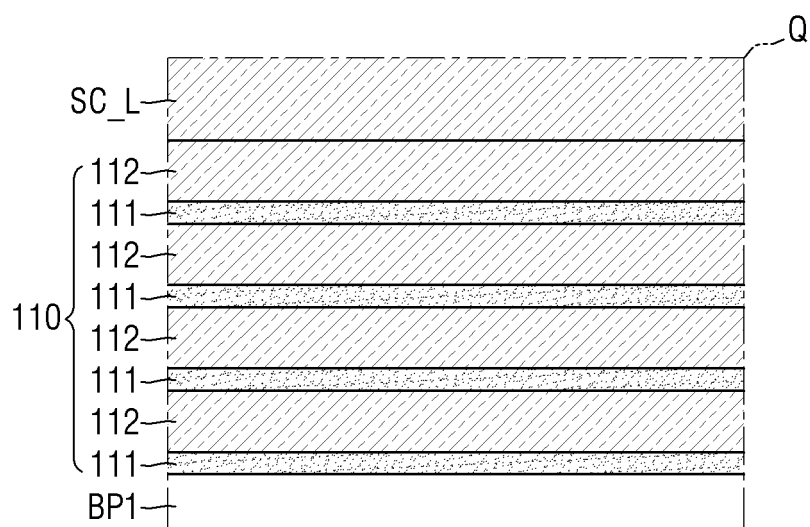


FIG. 40

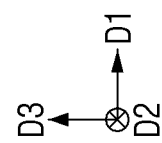
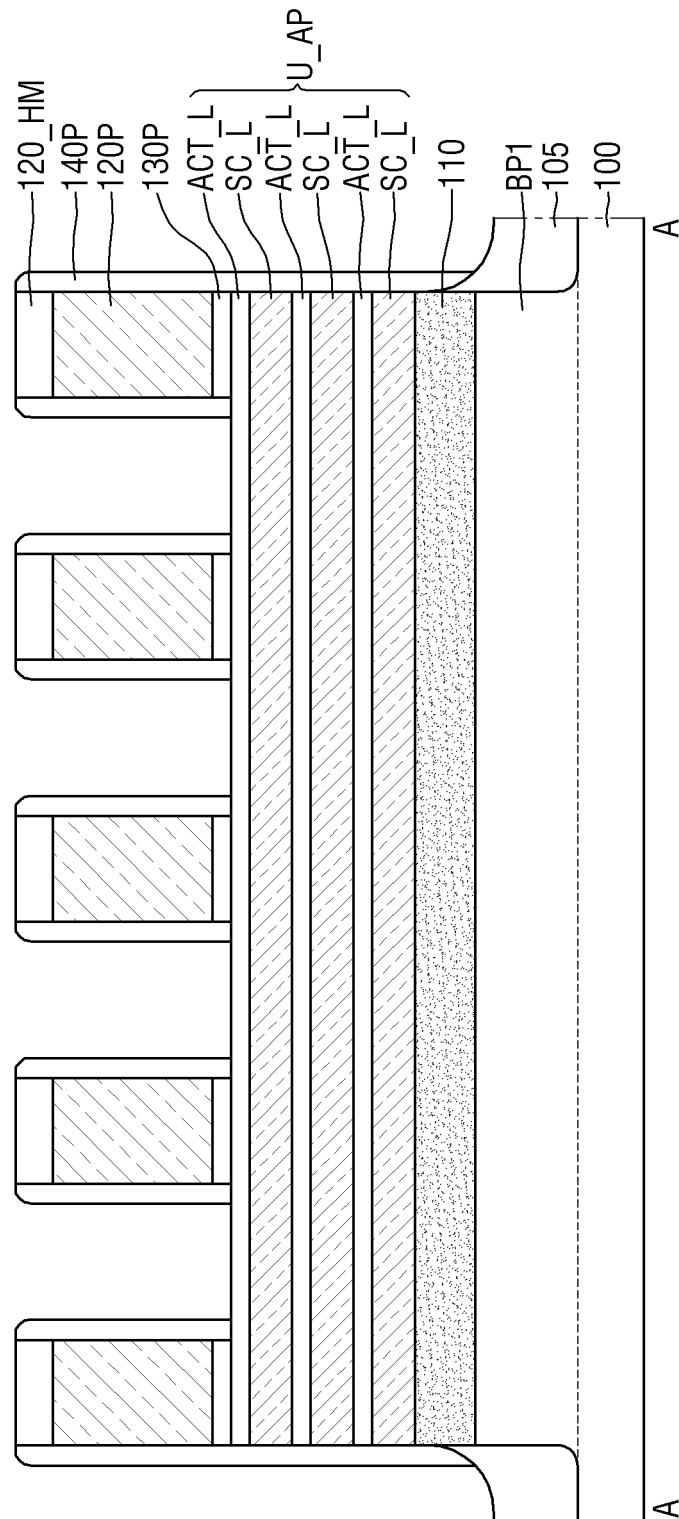


FIG. 41

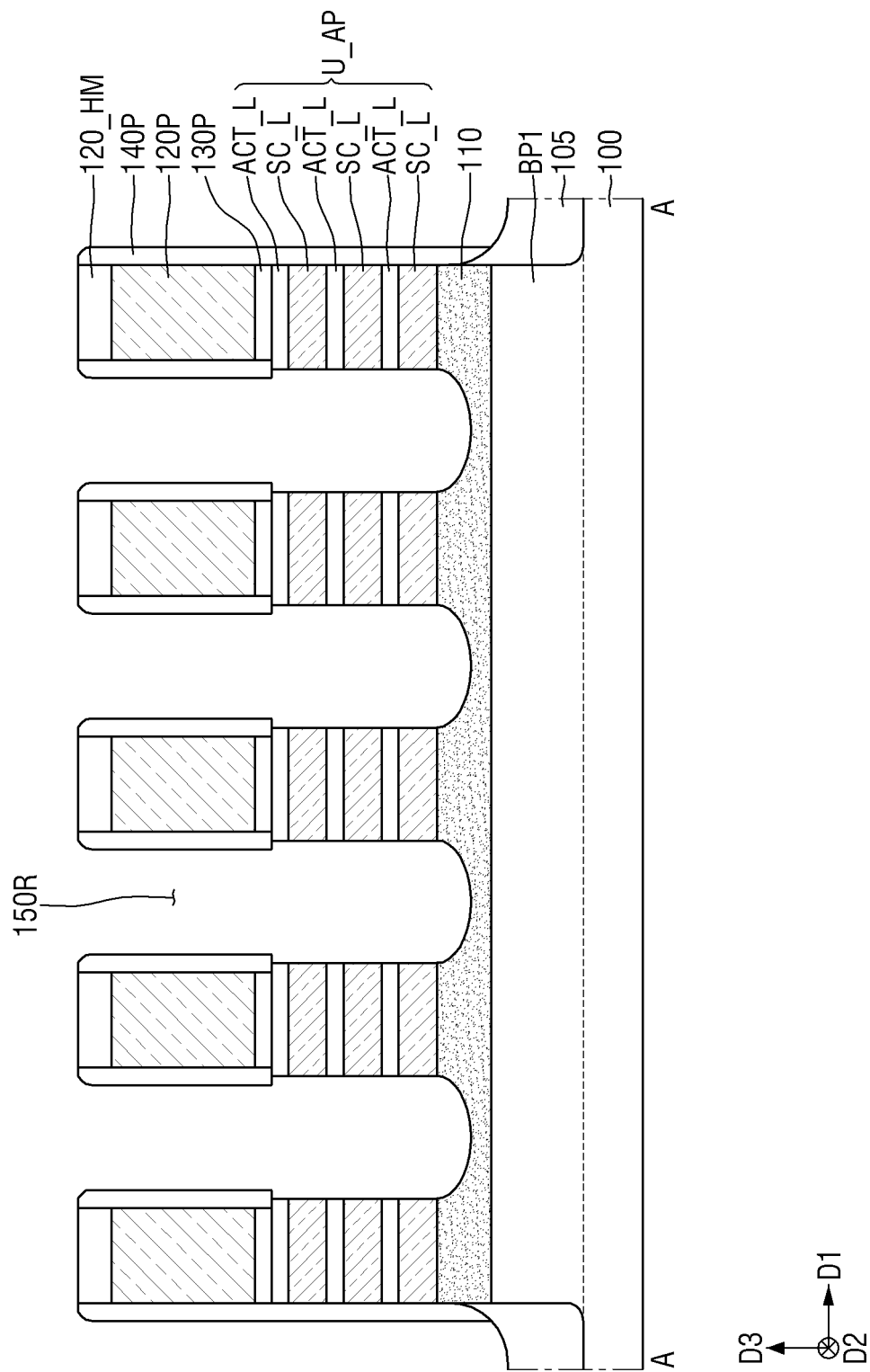


FIG. 42

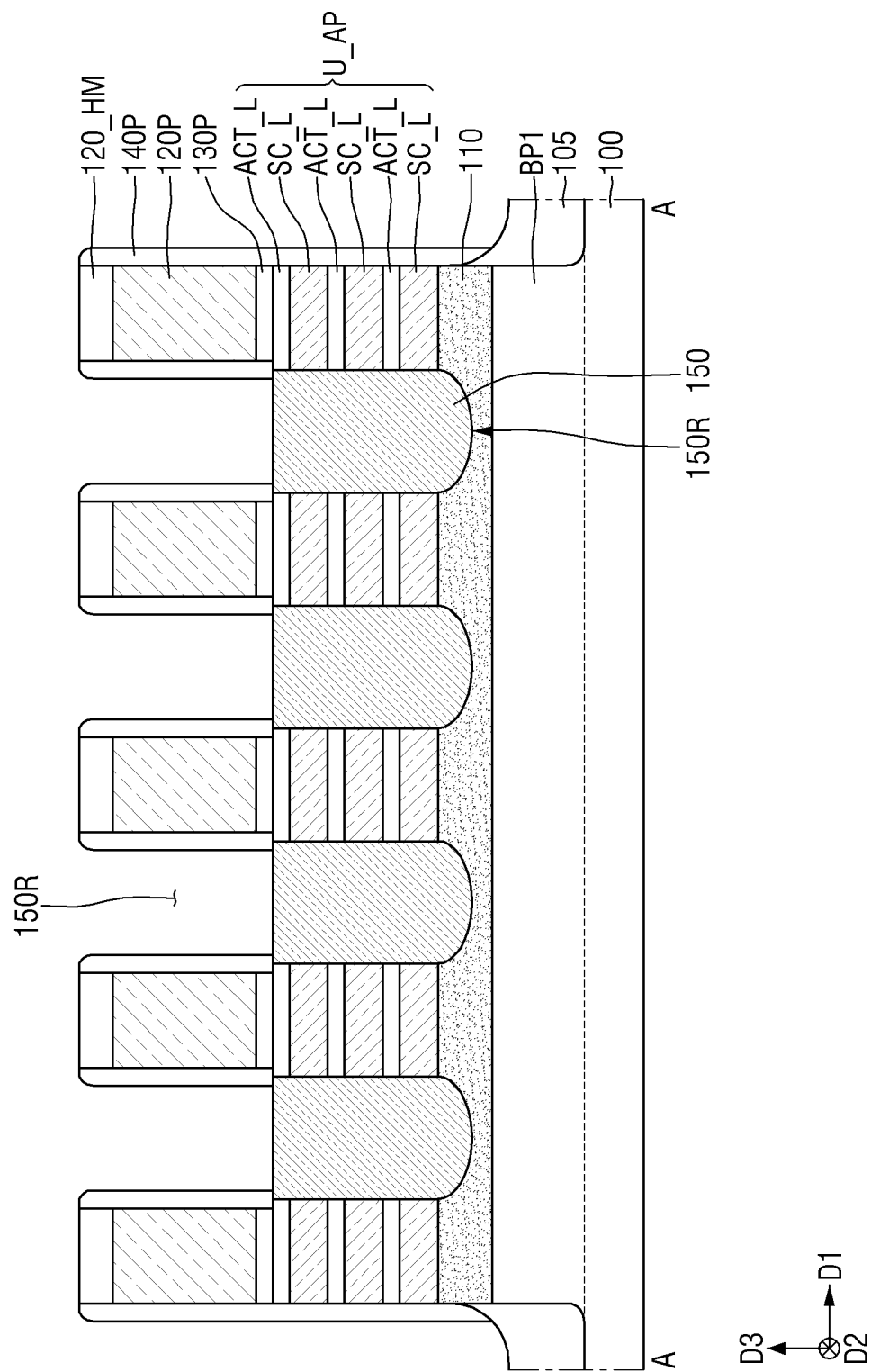
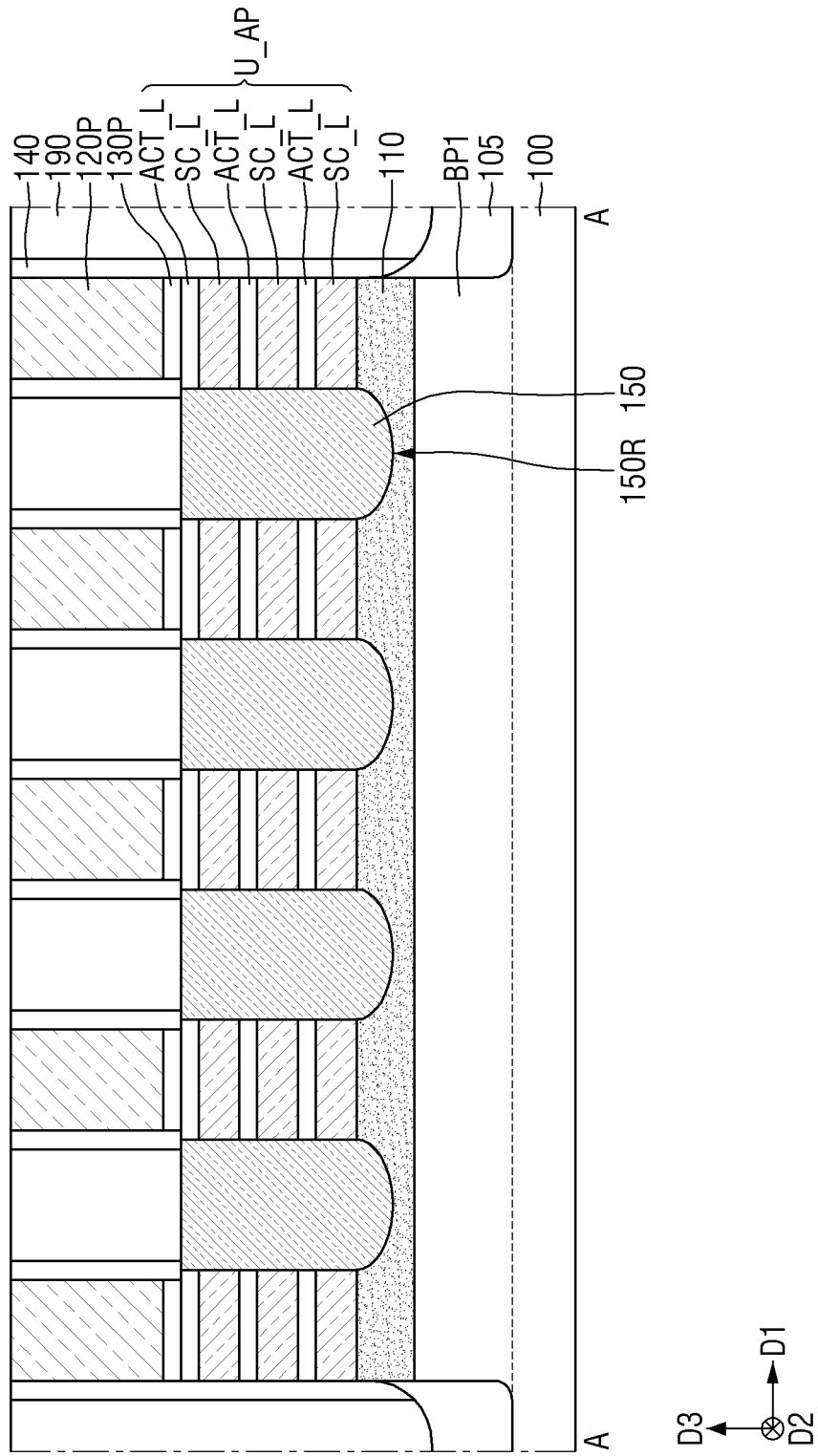


FIG. 43



This cross-sectional view shows a substrate 100 with a base layer 105 and a buffer layer 110. A series of gate structures 120t are formed on the substrate, each consisting of a gate stack 120t and a gate electrode 120t. The gate stacks are separated by insulating regions 150R. The gate electrodes are connected to a common gate line 150. The device is covered by a passivation layer 140 and a protective layer 190. The cross-section is taken along line A-A.

FIG. 45

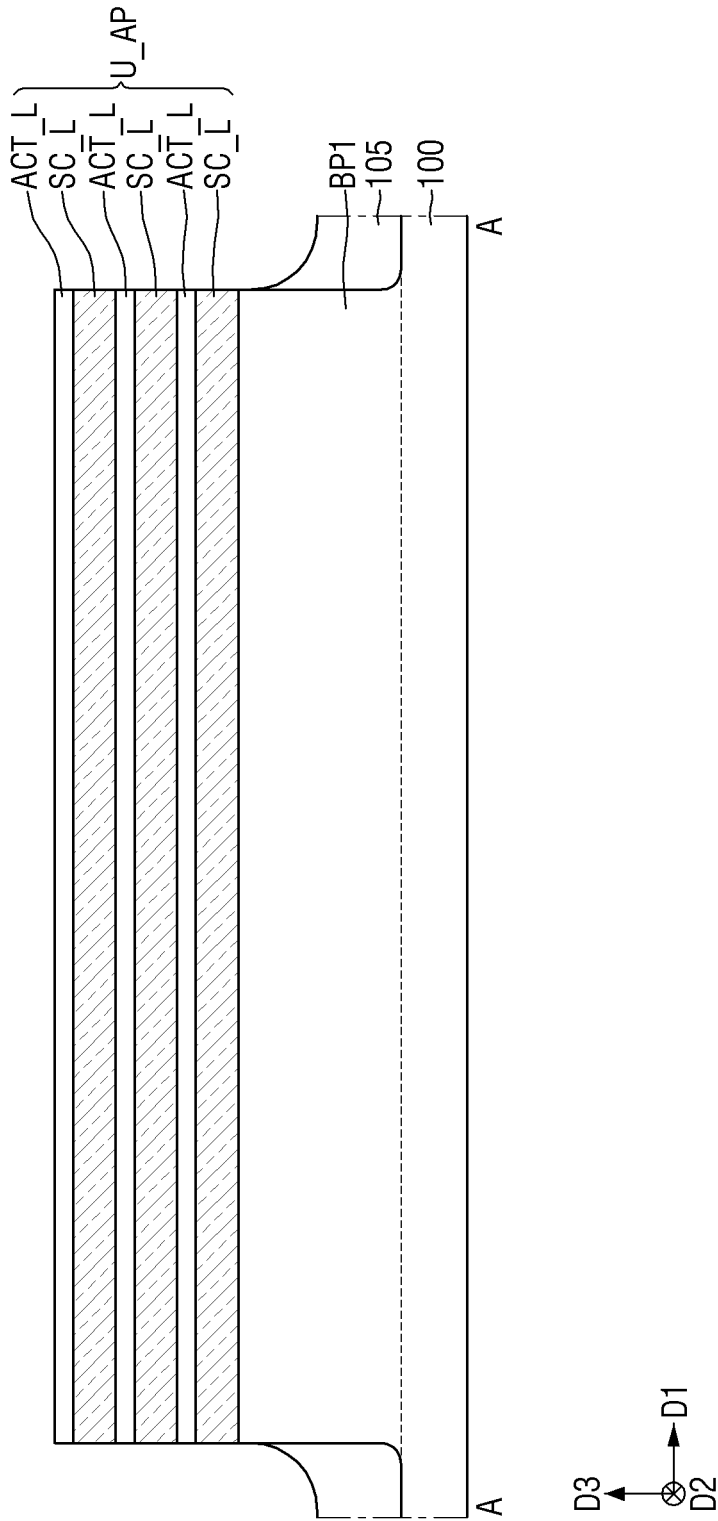


FIG. 46

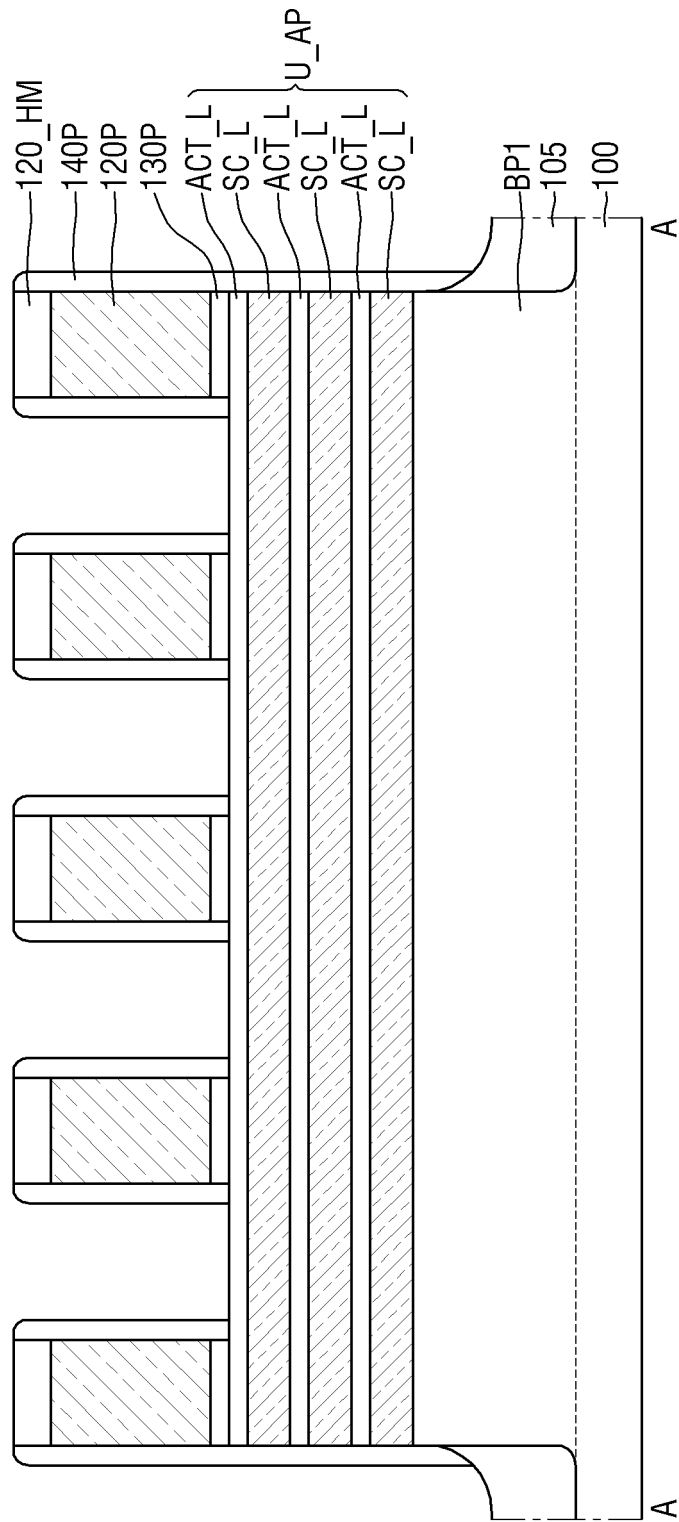


FIG. 47

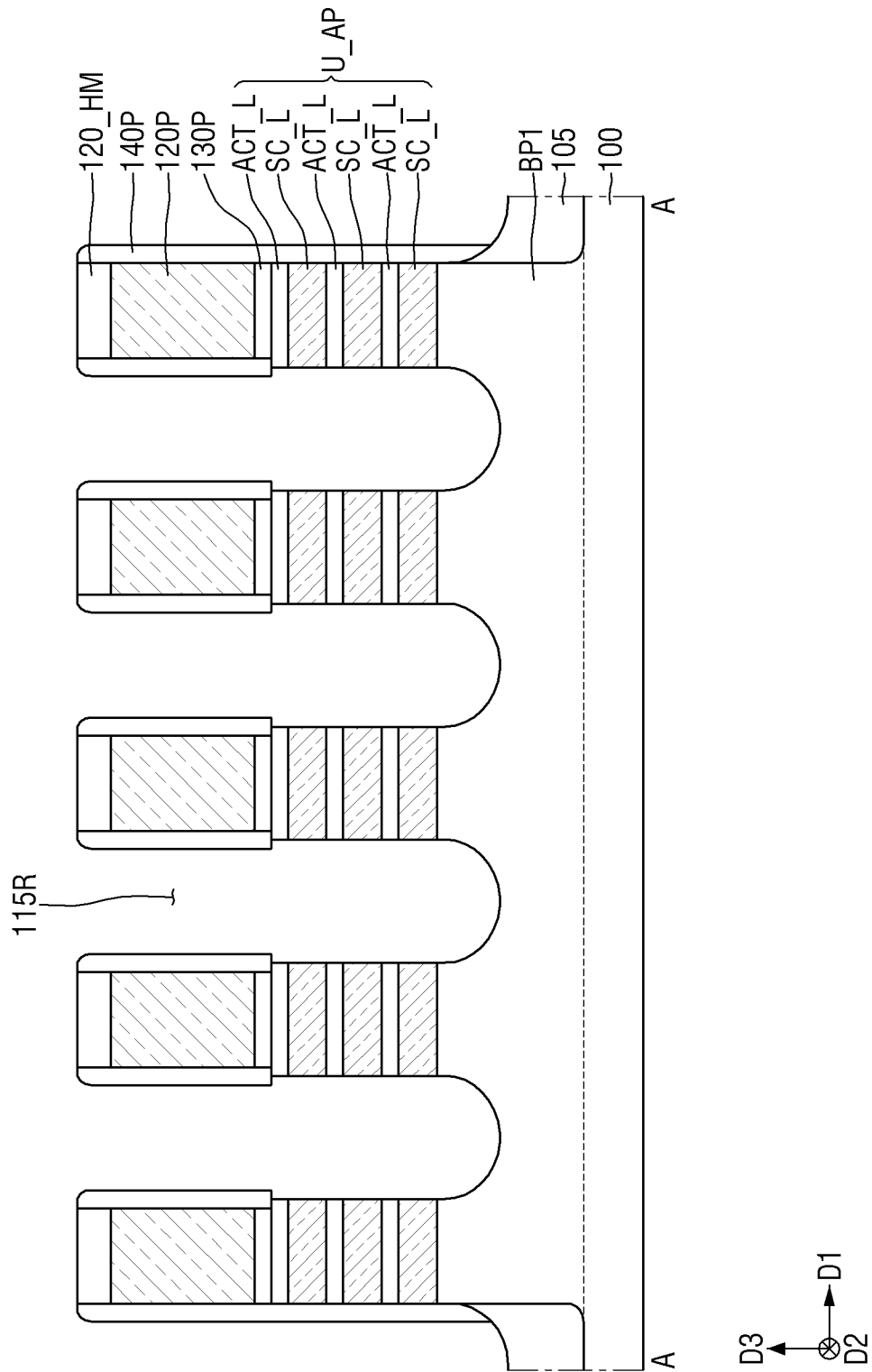


FIG. 48

