CLAIMS

1. A method comprising:

forming a plurality of isolation regions in a semiconductor region of a semiconductor device, said plurality of isolation regions laterally delineating a plurality of fins in said semiconductor region;

forming a place holder gate electrode structure above said semiconductor region, said place holder gate electrode structure covering a central portion of each of said plurality of isolation regions and fins;

forming drain and source regions in each of said plurality of fins in the presence of said place holder gate electrode structure;

removing said placeholder material so as to expose said central portions of said plurality of isolation regions and fins;

forming a recess selectively in said central portions of said plurality of isolation regions so as to adjust an electrically effective height of said central portions of said fins; and

forming a gate dielectric material and an electrode material in said recesses and above said central portions of said fins.

2. The method of claim 1, further comprising forming contact elements laterally adjacent to said place holder gate electrode structure prior to replacing said place holder material so as to connect to said drain and source regions.

3. The method of claim 2, wherein forming said contact elements comprises providing a conductive contact material that has etch stop characteristics with respect to said place holder material and material of said plurality of isolation regions.

4. The method of claim 3, wherein said conductive contact material is provided so as to have an exposed surface that comprises titanium nitride.

5. The method of claim 1, wherein forming said drain and source regions comprises depositing a doped semiconductor material in the presence of said place holder material.

6. The method of claim 5, further comprising forming recesses in said plurality of fins and forming said doped semiconductor material at least in said recesses.

7. The method of claim 6, wherein forming said doped semiconductor material comprises forming a strain inducing semiconductor alloy.

8. The method of claim 1, wherein forming a recess selectively in said central portions of said plurality of isolation regions comprises performing a plasma assisted etch process and removing polymer byproducts of said plasma assisted etch process by using an oxidizing chemistry so as to form an oxide layer on exposed surface areas of said central portions of said plurality of fins.

9. The method of claim 1, further comprising forming a second isolation region so as to laterally delineate a continuous semiconductor region having a lateral size that is greater than a lateral size of each of said plurality of fins, wherein the method further comprises forming a planar transistor in and above said continuous semiconductor region.

10. The method of claim 9, further comprising masking said continuous semiconductor region and said second isolation region prior to forming said recess in each of said plurality of fins.

11. A method of forming a semiconductor device, the method comprising:

forming a gate opening in a place holder gate electrode structure that is formed above a central portion of a plurality of fins formed in a semiconductor region and being laterally separated by isolation regions;

forming a cavity in a central portion of each of said isolation regions through said gate opening so as to adjust an electrically effective height of said plurality of fins; and

forming a gate dielectric material and an electrode material in said cavities and said gate opening.

12. The method of claim 11, further comprising forming a conductive contact material laterally adjacent to said place holder gate electrode structure prior to forming said gate opening.

13. The method of claim 11, wherein forming said conductive contact material comprises providing etch stop characteristics with respect to a place holder material and said isolation regions at least on a surface of said conductive contact material.

14. The method of claim 13, wherein said conductive contact material comprises titanium nitride at least at a surface thereof.

15. The method of claim 11, further comprising forming a drain region and a source region in each of said plurality of fins prior to forming said gate opening.

16. The method of claim 15, wherein forming drain and source regions comprises selectively depositing a doped semiconductor material.

17. The method of claim 16, wherein forming said drain and source regions comprises forming drain and source cavities in each of said plurality of fins and filling said drain and source cavities with an in-situ doped semiconductor material.

18. A semiconductor device comprising:

a semiconductor region comprising a plurality of fins that are separated by isolations regions, each of said isolation regions having a recessed central isolation portion;

a high-k metal gate electrode structure formed above a central portion of said plurality of fins and above said recessed central isolation portions;

a drain region formed in each of said plurality of fins so as to connect to said central portion;

a source region formed in each of said plurality of fins so as to connect to said central portion;

a first self-aligned contact element formed above each of said drain regions and above said isolation regions; and

a second self-aligned contact element formed above each of said source regions and above said isolation regions.

19. The semiconductor device of claim 18, further comprising a second semiconductor region whose lateral size is greater than a lateral size of each of said plurality of fins, wherein said second semiconductor region comprises continuous drain and source regions and self-aligned contact elements connecting to said continuous drain and source regions.

20. The semiconductor device of claim 18, wherein said first and second self-aligned contact elements comprise, at least at a top surface thereof, a titanium and nitride containing contact material.

CLAIMS

1. A method, comprising:

forming a plurality of isolation regions in a semiconductor region of a semiconductor device, said plurality of isolation regions laterally delineating a plurality of fins in said semiconductor region;

forming a placeholder gate electrode structure above said semiconductor region, said placeholder gate electrode structure covering a central portion of each of said plurality of isolation regions and fins;

forming drain and source regions in each of said plurality of fins in the presence of said placeholder gate electrode structure; removing said placeholder material so as to expose said central portions of said plurality of isolation regions and fins;

forming a recess selectively in said central portions of said plurality of isolation regions so as to adjust an electrically effective height of said central portions of said fins; and

forming a gate dielectric material and an electrode material in said recesses and above said central portions of said fins.

2. The method of claim 1, further comprising forming contact elements laterally adjacent to said placeholder gate electrode structure prior to replacing said placeholder material so as to connect to said drain and source regions.

3. The method of claim 2, wherein forming said contact elements comprises providing a conductive contact material that has etch stop characteristics with respect to said placeholder material and material of said plurality of isolation regions.

4. The method of claim 3, wherein said conductive contact material is provided so as to have an exposed surface that comprises titanium nitride.

5. The method of claim 1, wherein forming said drain and source regions comprises depositing a doped semiconductor material in the presence of said placeholder material.

6. The method of claim 5, further comprising forming recesses in said plurality of fins and forming said doped semiconductor material at least in said recesses.

7. The method of claim 6, wherein forming said doped semiconductor material comprises forming a strain-inducing semiconductor alloy.

8. The method of claim 1, wherein forming a recess selectively in said central portions of said plurality of isolation regions comprises performing a plasma assisted etch process and removing polymer by products of said plasma assisted etch process by using an oxidizing chemistry so as to form an oxide layer on exposed surface areas of said central portions of said plurality of fins.

9. The method of claim 1, further comprising forming a second isolation region so as to laterally delineate a continuous semiconductor region having a lateral size that is greater than a lateral size of each of said plurality of fins, wherein the method further comprises forming a planar transistor in and above said continuous semiconductor region.

10. The method of claim 9, further comprising masking said continuous semiconductor region and said second isolation region prior to forming said recess in each of said plurality of fins.

11. A method of forming a semiconductor device, the method comprising:

forming a gate opening in a placeholder gate electrode structure that is formed above a central portion of a plurality of fins formed in a semiconductor region and being laterally separated by isolation regions;

forming a cavity in a central portion of each of said isolation regions through said gate opening so as to adjust an electrically effective height of said plurality of fins; and

forming a gate dielectric material and an electrode material in said cavities and said gate opening.

12. The method of claim 11, further comprising forming a conductive contact material laterally adjacent to said placeholder gate electrode structure prior to forming said gate opening.

13. The method of claim 11, wherein forming said conductive contact material comprises providing etch stop characteristics with respect to a placeholder material and said isolation regions at least on a surface of said conductive contact material.

14. The method of claim 13, wherein said conductive contact material comprises titanium nitride at least at a surface thereof.

15. The method of claim 11, further comprising forming a drain region and a source region in each of said plurality of fins prior to forming said gate opening.

16. The method of claim 15, wherein forming drain and source regions comprises selectively depositing a doped semiconductor material.

17. The method of claim 16, wherein forming said drain and source regions comprises forming drain and source cavities in each of said plurality of fins and filling said drain and source cavities with an in situ doped semiconductor material.

18. A semiconductor formed by a method in accordance with any one of the preceding claims.