What is Claimed is:

1. A memory device comprising:

a memory cell array comprising a plurality of memory cells;

a control logic configured to output a control signal for data reading or data writing to the memory cell array; and

a data streamer configured to perform a streaming operation for reading data from or writing data to the memory cell array in response to a streaming signal,

wherein the data streamer is further configured to receive data size information of first data to be read or written and perform the streaming operation by outputting at least one streaming drive command to the control logic based on the data size information,

wherein the data streamer comprises a state manager configured to determine a type and a number of the at least one streaming drive command based on the data size information in response to the streaming signal received from outside of the memory device and configured to output the at least one streaming drive command to the control logic, the at least one streaming drive command being for reading or writing the first data.

2. The memory device of claim 1, wherein the first data is deterministic data of which a format and a size do not vary with an external command that is external to the memory device.

3. The memory device of claim 1, wherein the first data is at least one among image data, audio data, and video data.

4. The memory device of claim 1, further comprising a data information register configured to store the data size information.

5. The memory device of claim 1, wherein the data streamer comprises:

an address manager configured to determine an address based on the data size information, the address being for reading or writing the first data; and

a timing manager configured to control output timing of the at least one streaming drive command and to count the number of the at least one streaming drive command.

6. The memory device of claim 1, wherein the state manager is further configured to differently determine the number of the at least one streaming drive command according to the data size information.

7. The memory device of claim 1, wherein the at least one streaming drive command comprises at least one signal among a row address strobe signal for driving the plurality of memory cells row by row, a column address strobe signal for driving the plurality of memory cells column by column, and a precharge signal for precharging the plurality of memory cells.

8. The memory device of claim 5, further comprising a status register configured to store available address information of an available address corresponding to a memory cell that does not store valid data among the plurality of memory cells.

9. The memory device of claim 8, wherein the address manager is further configured to, in a write streaming operation, receive the available address information from

the status register and determine a write address for writing of the first data based on the available address information and the data size information.

10. The memory device of claim 5, wherein the address manager is further configured to, in a read streaming operation, receive a start address corresponding to a first one of a plurality of addresses of the memory cell array in which the first data has been stored and determine a read address for reading of the first data based on the start address and the data size information.

11. The memory device of claim 1, further comprising a mode register configured to receive a mode command from outside the memory device and to set an operating mode of the memory device in response to the mode command,

wherein the streaming signal is included in the mode command.

12. The memory device of claim 1, further comprising a command address generator configured to generate a command and an address for a read or write operation on the memory cell array,

wherein the data streamer is further configured to generate a state signal comprising state information about a state for the read or write operation, the state information being generated based on the data size information, and outputs the state signal to the command address generator, and

the command address generator is further configured to generate, based on the state information, at least one signal among a row address strobe signal for driving the plurality of memory cells row by row, a column address strobe signal for driving the plurality of memory

cells column by column, and a precharge signal for precharging the plurality of memory cells, and output the at least one signal to the control logic.

13. The memory device of claim 1, further comprising a multiplexer configured to receive, from outside of the memory device, at least one normal drive command for reading or writing the first data and to selectively output the at least one normal drive command and the at least one streaming drive command to the control logic according to a mode selection signal of the data streamer.

14. A memory system comprising:

a memory controller; and

a memory device,

wherein the memory controller comprises a streaming manager configured to output data size information of first data to the memory device when the first data is deterministic data of which a format and a size do not vary with an external command that is external to the memory controller, the first data being written to or read from the memory device, and

the memory device comprises a data streamer configured to perform a streaming operation by internally generating, by the data streamer, at least one streaming drive command based on the data size information without intervention of the memory controller, the least one streaming drive command being for reading or writing the first data,

wherein the data streamer comprises a state manager configured to determine a type and a number of the at least one streaming drive command based on the data size information in response to a streaming signal and to output the at least one streaming drive command to a control logic.

15. The memory system of claim 14, wherein the streaming manager comprises:

a data information generator configured to generate the data size information based on the first data; and

a streaming enabler configured to output, to the memory device, the streaming signal for performing the streaming operation.

16. The memory system of claim 15, wherein the streaming enabler is further configured to determine whether the first data is the deterministic data and outputs the streaming signal to the memory device when the first data is determined to be the deterministic data.

17. The memory system of claim 15, wherein the streaming manager is further configured to:

output the streaming signal and the data size information to the memory device when the first data is written, and

output the streaming signal, the data size information, and a start address to the memory device when the first data is read, the start address corresponding to a first one of a plurality of addresses at which the first data has been stored.

18. The memory system of claim 14, wherein the memory device further comprises a memory cell array comprising a plurality of memory cells storing data and the control logic configured to output a control signal for controlling the memory cell array,

the memory controller is further configured to output the streaming signal for performing the streaming operation to the data streamer in response to a streaming command from a host, and

the data streamer comprises:

an address manager configured to determine an address based on the data size information, the address being for reading or writing the first data, and

a timing manager configured to control output timing of the at least one streaming drive command and to count the number of the at least one streaming drive command.

19. An image processing apparatus comprising:

an image sensor comprising a plurality of pixels, the image sensor being configured to generate image data based on an optical signal applied to the plurality of pixels;

a memory device; and

a memory controller configured to receive the image data and to output data size information of the image data and a streaming signal to the memory device, and

the memory device comprising:

a memory cell array configured to store the image data,

a control logic configured to output a control signal for data reading or writing to the memory cell array, and

a data streamer configured to receive the data size information, to generate internally, by the data streamer, at least one streaming drive command based on the data size information without intervention of the memory controller, and to output the at least one streaming drive command to the control logic so that the image data is written to the memory cell array,

wherein the data streamer comprises a state manager configured to determine a type and a number of the at least one streaming drive command based on the data size information and to output the at least one streaming drive command to the control logic, the least one streaming drive command being for reading or writing the image data.

20. The image processing apparatus of claim 19, wherein the data streamer comprises:

an address manager configured to determine an address based on the data size information, the address being for reading or writing the image data; and

a timing manager configured to control output timing of the at least one streaming drive command and to count the number of the at least one streaming drive command.