

ABSTRACT OF THE DISCLOSURE

A memory device including an interface circuit for data conversion according to different endian formats includes an interface circuit that performs data conversion with hardware in a data transfer path inside the memory device in accordance with a memory bank, a processing element (PE), and an endian format of a host device. The interface circuit is (i) between a memory physical layer interface (PHY) region and a serializer/deserializer (SERDES) region, (ii) between the SERDES region and the memory bank or the PE, (iii) between the SERDES region and a bank group input/output line coupled to a bank group including a number of memory banks, and (iv) between the PE and bank local input/output lines coupled to the memory bank.

FIG. 7