Claims

1. A method of forming a semiconductor device, the method comprising:

providing an engineered substrate including:

a polycrystalline ceramic core;

a barrier layer encapsulating the polycrystalline ceramic core;

a bonding layer coupled to the barrier layer; and

a substantially single crystalline silicon layer coupled to the bonding layer;

forming a first epitaxial N-type gallium nitride layer coupled to the substantially single crystalline silicon layer, the first epitaxial N-type gallium nitride layer having a first doping concentration;

forming a second epitaxial N-type gallium nitride layer coupled to the first epitaxial N-type gallium nitride layer, the second epitaxial N-type gallium nitride layer having a second doping concentration less than the first doping concentration;

forming a channel region coupled to the second epitaxial N-type gallium nitride layer by forming an epitaxial aluminum gallium nitride barrier layer on the second epitaxial N-type gallium nitride layer, the channel region having a first end and a second end, and a central portion between the first end and the second end;

forming a gate dielectric layer coupled to the epitaxial aluminum gallium nitride barrier layer in the central portion of the channel region;

forming a gate contact coupled to the gate dielectric layer;

forming a source contact at the first end of the channel region;

forming a via through the second epitaxial N-type gallium nitride layer at the second end of the channel region to expose a portion of the first epitaxial N-type gallium nitride layer;

filling the via with a conductive material; and

forming a drain contact at the second end of the channel region, the drain contact electrically coupled to the first epitaxial N-type gallium nitride layer through the conductive material in the via.

2. The method of claim 1 wherein the semiconductor device comprises a high-electron-mobility transistor (HEMT).

3. The method of claim 1 wherein the epitaxial aluminum gallium nitride barrier layer, the second epitaxial N-type gallium nitride layer, and the first epitaxial N-type gallium nitride layer form a voltage clamp diode.

4. The method of claim 1 wherein the second epitaxial N-type gallium nitride layer has a thickness greater than about 5 μm.

5. The method of claim 4 wherein the second epitaxial N-type gallium nitride layer has a thickness greater than about 10 μm.

6. The method of claim 1 further comprising:

forming one or more gate field plates coupled to the gate contact;

forming a source field plate coupled to the source contact;

forming an interlayer dielectric (ILD) layer over the epitaxial aluminum gallium nitride barrier layer and the gate dielectric layer; and

forming a source pad over the ILD layer, the source pad electrically coupled to the source contact and the source field plate.

7. The method of claim 1 wherein the polycrystalline ceramic core comprises polycrystalline aluminum gallium nitride (AlGaN).

8. The method of claim 1 wherein the substantially single crystalline silicon layer has a (111) surface orientation.

9. A lateral high-electron-mobility transistor (HEMT) comprising:

a drain pad;

an epitaxial gallium nitride layer coupled to the drain pad;

a channel region having a first end, a second end, and a central portion between the first end and the second end, the channel region comprising an epitaxial aluminum gallium nitride barrier layer coupled to the epitaxial gallium nitride layer;

a gate dielectric layer coupled to the central portion of the channel region;

a gate contact coupled to the gate dielectric layer;

a source contact disposed at the first end of the channel region;

a via disposed at the second end of the channel region; and

a drain contact coupled to the via, wherein the drain contact is electrically connected to the drain pad through the via;

wherein the epitaxial aluminum gallium nitride barrier layer, the epitaxial gallium nitride layer, and the drain contact form a voltage clamp diode.

10. The lateral HEMT of claim 9 wherein the via passes through the epitaxial gallium nitride layer.

11. The lateral HEMT of claim 9 wherein the epitaxial gallium nitride layer has a thickness that is greater than about 5 μm.