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# USE OF AN INSULATOR SPACER ON THE SIDEWALLS OF A VIA HOLE

## BACKGROUND OF THE INVENTION

### (1) FIELD OF THE INVENTION

The invention relates to processes used to fabricate semiconductor devices, and more specifically to a process used to form an insulator spacer, on the sides of a via hole, to improve the integrity of the via hole.

### (2) DESCRIPTION OF THE PRIOR ART

The semiconductor industry is continually striving to improve the performance of semiconductor devices. This objective has been addressed by the ability of the semiconductor industry to fabricate devices with sub-micron features, or micro-miniaturization. Via holes, in a dielectric layer, are used as conduits to allow physical and electrical connection, between wiring levels, to be realized. The via holes can be designed with diameters in the sub-micron range to allow the performance objective to be realized. However the formation of via holes, with sub-micron diameters, present problems, that if not addressed, can result in either semiconductor device yield or reliability problems.

First, to obtain a sub-micron diameter, via hole, anisotropic dry etching procedures are used. These procedures, using specific etch chemistries, needed for the anisotropic component, as well as used for selectivity between the dielectric material being etched, and the underlying conductor, can produce resistant materials on the sidewall of the etched via. These materials, complex polymers, are difficult to remove, and if not completely removed, or passivated, can adversely influence device yield and reliability. Other deleterious phenomena can occur in the formation of sub-micron diameter via holes, when forming vias in a multi-layered dielectric film. For example if a spin-on glass, (SOG), layer is used as part of a three layer dielectric composite, comprised of plasma enhanced chemically vapor deposited, (PECVD), sandwiching the SOG layer, the exposed sides of the SOG layer, located between PECVD layers, can introduce contaminants to the very narrow via hole in the form of outgassed solvents and moisture. This phenomena is more severe with sub-micron diameter vias, concentrating the outgassed contaminants in an enclosed, small via hole. This phenomena can lead to poisoning or corrosion of the conductive material used to fill the sub micron diameter via hole, again resulting in yield or reliability problems. In addition if a composite dielectric, comprised of several specific materials is used, and if one or more of the layers is more influenced by an isotropic component of the dry etching ambient, severe undercutting can occur in the sub-micron diameter via hole.

The undercut shaped via hole is now more difficult to fill with a conductive material, possibly resulting in yield or reliability problems.

This invention will offer a solution to the above phenomena. A insulator spacer is formed, on the sides of the sub-micron diameter via hole, using a PECVD oxide deposition, followed by a dry etch procedure, creating the insulator spacer. The insulator spacer encapsulates the unremoved, resistant material, on the sides of the etch via, removing the possibility of reaction between the resistant materials and the conductive material placed in the sub-micron diameter via hole. The insulator spacer also fills the crevices, or undercuts, formed in the composite dielectric, occurring during the dry etching of the composite dielectric. The insulator spacer produces a straight walled, sub-micron diameter via hole. Yang, et al, in U.S. Pat. No. 5,393,702, describe a process for preventing outgassing from an exposed SOG layer, by nitriding the exposed SOG via reaction with $NH_3$. This invention prevents outgassing from exposed SOG regions by creating the insulator spacer. In addition this invention, unlike Yang, et al, describe a process for encapsulating sidewall contaminants.

## SUMMARY OF THE INVENTION

It is an object of this invention to create an insulator spacer on the sides of a sub-micron diameter via hole, in

a dielectric layer, to encapsulate contaminant residues, formed on the sides of the etched via hole during the anisotropic dry etching process.

It is another object of this invention to create an insulator spacer on the sides of a sub-micron diameter via hole, in a composite dielectric layer, to prevent outgassing from an exposed SOG layer, used as one of the components of a composite dielectric layer.

It is still another object of this invention to create an insulator spacer on the sides of a sub-micron diameter via hole, in a composite dielectric layer, to fill undercut regions in the composite dielectric layer, producing a straight walled via hole.

It is still yet another object of this invention to create the insulator spacer, on the sides of a sub-micron diameter via hole, by depositing an insulator layer, followed by anisotropic dry etching.

In accordance with the present invention a process is described for forming an insulator spacer on the sides of a sub-micron diameter via hole: allowing encapsulation of unwanted residues on the sides of the sub-micron diameter via hole; preventing outgassing from exposed SOG layers, used as part of the composite dielectric layer that the sub-micron via hole was formed in; and refilling undercuts in the composite dielectric layer that

the sub-micron via hole was etched in. A thick dielectric layer is formed over semiconductor device structures, located on a semiconductor substrate. A contact hole is opened in the thick dielectric layer, exposing a device region in the semiconductor substrate. A metal contact structure is formed in the contact hole, contacting the underlying device region in the semiconductor substrate, and extending over the top surface of the thick dielectric layer. An interlevel dielectric layer, or a composite interlevel dielectric layer, using a SOG layer as one of the layers, is deposited on the metal contact structure, as well as on the top surface of the thick dielectric layer, not covered by the metal contact structure. A sub-micron diameter via hole is next etched in the interlevel dielectric layer, or in the composite interlevel dielectric layer, using anisotropic reactive ion etching, (RIE), exposing the top surface of the metal contact structure. After the RIE procedure: residual material, formed during the anisotropic RIE procedure, may be present on the sides of the sub-micron diameter via hole; exposed SOG sidewall surfaces can be present in the sub-micron diameter via hole, formed in a composite interlevel dielectric layer that includes a SOG layer as one of the components; and undercut regions of the composite interlevel dielectric layer, can be present in the sub-micron diameter via hole. An insulator layer is next deposited using chemical vapor deposition procedures, followed by an anisotropic RIE procedure, creating an insulator spacer on the sides of the

sub-micron diameter via hole, encapsulating any residual material on the sides of the via hole, and/or preventing outgassing from SOG layer, and/or refilling undercut regions in the composite interlevel dielectric layer that the sub-micron diameter via hole was formed in. A metal interconnect structure is next formed, contacting the top surface of the underlying metal contact structure, interfacing the insulator spacer in the sub-micron diameter via hole, and extending over the top surface of the interlevel dielectric layer, or composite interlevel dielectric layer, used to form the sub-micron via hole in.

## BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiment with reference to the attached drawings that include:

Figs. 1 - 4, schematically, in cross-sectional style, describing the formation of an insulator spacer, on the sides of a sub-micron diameter via hole, in a dielectric layer, with residues from the via hole, anisotropic RIE procedure, on the sides of the sub-micron diameter via hole, encapsulated by the insulator spacer.

Figs. 5 - 7, schematically, in cross-sectional style, showing the formation of an insulator spacer, on the sides of a sub-micron diameter hole, in a composite dielectric layer,

comprised of a SOG layer as a component of the composite dielectric layer, and with outgassing from the SOG layer being prevented by the overlying insulator spacer.

Figs. 8 - 10, schematically, in cross-sectional representation, showing an insulator spacer, on the sides of a sub-micron diameter via hole, formed in a composite dielectric layer, and with undercut regions of the composite dielectric layer, filled with by the insulator spacer.

Fig. 11, schematically, in cross-sectional style, showing the formation of a metal interconnect structure, in the sub-micron diameter via hole, interfacing the insulator spacer, on the sides of the sub-micron diameter via hole.

Figs. 12 - 13, schematically, in cross-sectional style, showing the formation of an insulator spacer, on the sides of a sub-micron diameter contact hole opening, in a dielectric layer, with residues on the contact hole sides, encapsulated by the insulator spacer.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method for forming an insulator spacer on the sides of a sub-micron via hole to: encapsulate residue material adhered to the via hole sides; or to prevent outgassing of a SOG layer, used as a component of a composite dielectric layer in which

the sub-micron diameter via hole was formed in; or to fill undercuts that may exist in regions of a composite dielectric layer in which the sub-micron via hole was formed in; will now be described. This invention will be described for a sub-micron diameter via hole, but could be applied to any diameter via hole. In addition this invention is shown as an application for a n-channel, (NFET), metal oxide semiconductor field effect transistor, (MOSFET), device. However this invention can also be applied to p-channel, (PFET), MOSFET devices, as well as for complimentary, (CMOS) devices. In addition other device structures, such as bipolar transistor devices, EEPROM devices, and DRAM devices, can be fabricated using this invention.

Fig. 1, shows a P type, semiconductor substrate, 1, having a <100> crystallographic orientation. A silicon oxide gate insulator layer, 2, is thermally grown to a thickness between about 50 to 200 Angstroms, followed by the deposition of a polysilicon layer, 3, via low pressure chemical vapor deposition, (LPCVD), procedures, to a thickness between about 1500 to 4000 Angstroms. Polysilicon layer, 3, is either deposited using in situ doping procedures, adding phosphine or arsine to a silane ambient, or grown intrinsically and doped using $POCl_3$, or doped via ion implantation of phosphorous or arsenic. A polysilicon layer is next patterned using conventional photolithographic and RIE procedures, using $Cl_2$ as an etchant, to form the polysilicon gate

structure, 3, schematically shown in Fig. 1. A lightly doped source and drain region, 4, is formed via ion implantation of phosphorous, in regions of semiconductor substrate, 1, not covered by polysilicon gate structure, 3. Silicon oxide sidewalls, 5, are next formed on the sides of polysilicon gate structure, 3, via deposition of a silicon oxide layer, via LPCVD or PECVD procedures, using tetraethylorthosilicate, (TEOS), as a source, followed by an anisotropic RIE procedure, using $CHF_3$ as an etchant. Heavily doped source and drain regions, 6, are then created via ion implantation of arsenic or phosphorous into regions of semiconductor substrate, 1, not covered by polysilicon gate structure, 3, and not covered by silicon oxide sidewalls, 5.

A thick insulator layer of silicon oxide, 7, is next deposited using PECVD procedures, to a thickness between about 10000 to 15000 Angstroms, at a temperature between about 350 to 450°C. Thick insulator layer, 7, can also be composed of borosilicate glass, or phosphosilicate glass. Planarization of thick insulator layer, 7, is performed using chemical mechanical polishing, resulting in a smooth top surface topography. Conventional photolithographic and RIE procedures, using $CHF_3$ as an etchant, are used to open a contact hole in thick insulator layer, 7, exposing the top surface of heavily doped source and drain region, 6. After removal of the photoresist masking layer, using plasma oxygen ashing and careful wet cleans, a metal contact

layer, 8, comprised of an adhesive layer of titanium, a barrier layer of titanium nitride, and an interconnecting metal layer of aluminum, containing between about 0.5 to 3 % copper, and between about 0 to 2 % silicon, is deposited using r.f. sputtering procedures, to a thickness between about 4000 to 10000 Angstroms. An anti-reflective coating of titanium nitride, between about 200 to 400 Angstroms, in thickness, is also deposited on the aluminum layer. Conventional photolithographic and RIE procedures, using $Cl_2$ as an etchant, are again employed to form metal contact structure, 8, shown schematically in Fig. 1. Metal contact structure, 8, can also be comprised of tungsten. After removal of the masking photoresist layer, via plasma oxygen ashing and careful wet cleans, an interlevel dielectric layer, 9, comprised of silicon oxide, is deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 10000 to 15000 Angstroms. A photoresist shape, 10, is formed on interlevel dielectric layer, 9, with a sub-micron opening, 11a, having a diameter between about 0.4 to 0.8 uM.

Fig. 2, schematically shows the result of an anisotropic RIE procedure, using $CHF_3$ as an etchant, used to transfer the sub-micron opening, 11a, in photoresist layer, 10, to interlevel dielectric layer, 9, creating sub-micron diameter via hole, 11b. Sub-micron diameter via hole, 11b, with straight walls, again exhibits a diameter between about 0.4 to 0.8 uM. The RIE

procedure, in addition to removing interlevel dielectric layer, 9, also forms unwanted polymer residue material, 12, on the sides of sub-micron diameter via hole, 11b. The polymer residue material is is comprised of carbon, silicon, titanium, aluminum, photoresist fragments, and plasma gases. Removal of photoresist shape, 10, using plasma oxygen ashing and careful wet cleans does not remove the polymer residue material, and if the polymer residue material would remain on the sides of sub-micron diameter via hole, 11b, reaction between the polymer residue material and a metal interconnect layer, used to fill sub-micron diameter via hole, 11b, could occur, adversely influencing the yield and reliability of the metal interconnect layer.

Figs. 3 - 4, schematically describe the formation of an insulator spacer, used to encapsulate the polymer residue material, 12, removing the possibility of reaction between polymer residue material and subsequent metal layers. After removal of photoresist shape, 10, using plasma oxygen ashing and careful wet cleans, a insulator layer, 13, of silicon oxide, is deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms, using TEOS as a source. The conformality of insulator layer, 13, allows for complete encapsulation of polymer residue material, 12, on the sides of sub-micron diameter via hole, 11b. Insulator layer, 13, can also be a silicon nitride layer. Fig. 4, schematically shows

the result of an anisotropic RIE procedure, using $CHF_3$ as an etchant, used to remove insulator layer, 13, from all regions except from the straight walled, sub-micron diameter via hole, 11b, creating insulator spacers, 13, on the sides of sub-micron diameter via hole, 11b. Argon sputter etching can also be used to form insulator spacers, 13. Insulator spacers, 13, completely encapsulates polymer residue material, 12, thus allowing subsequent metal layers to interface insulator spacers, 13, preventing direct contact between subsequent metal layers and polymer residue material, 12.

A second use of the insulator spacers, on the sides of a sub-micron diameter via hole, is described using Figs. 5 - 7. In this case a composite interlevel dielectric layer is used, comprised of: an underlying layer of silicon oxide, 14, obtained via PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 3000 to 6000 Angstroms; a SOG layer, 15a, applied and cured at a temperature between about 400 to 425°C, to a thickness between about 4000 to 5500 Angstroms, and etched back to result in a SOG layer, 15a, with a thickness between about 1500 to 3000 Angstroms; and an overlying layer of silicon oxide, 16, again obtained via PECVD procedures, at a temperature between about 375 to 425°C, to a thickness between about 6000 to 8000 Angstroms. A photoresist shape, 17, with a sub-micron diameter opening, 18a, is used and shown schematically in Fig. 5.

A RIE procedure, using $CHF_3$ as an etchant, is used to transfer sub-micron diameter opening, 18a, in photoresist shape, 17, to the composite interlevel dielectric layer, creating a straight walled, sub-micron diameter via hole, 18b, in the composite interlevel dielectric layer, exposing the top surface of metal contact structure, 8. This is schematically shown in Fig. 6. For this iteration sub-micron diameter via hole, 18b, exhibits the exposed SOG surfaces, 15b, of SOG layer, 15a. SOG layers contain significant levels of moisture, and levels of unevaporated solvents, that can outgas during subsequent processing steps, such as metal depositions, resulting in oxidation or reaction with the depositing metal layer, resulting in metal resistivity increases, or corrosion of the metal layer. This effect is more pronounced in small spaces, such as the sub-micron diameter via hole, where the amount of outgassing from exposed SOG surfaces, 15b, is concentrated. Therefore a procedure to prevent outgassing from exposed SOG surfaces, 15b, using the insulator spacer invention is performed, and shown in Fig. 7. Again an insulator layer, 19, of silicon oxide is deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms, using TEOS as a source. Insulator layer, 19, can also be a silicon nitride layer. An anisotropic RIE procedure, using $CHF_3$ as an etchant is used to create insulator spacers, 19, on the sides of the straight walled, sub-micron diameter via hole, 18, completely covering the exposed SOG surfaces, 15b, thus preventing

SOG outgassing during subsequent metal depositions. Argon sputter etching can also be used to create insulator spacers, 19.

A third iteration of this invention is schematically described using Figs. 8 - 10. In this case a composite interlevel dielectric layer, in Fig. 8, is used and comprised of: an underlying insulator layer, 20, for example silicon oxide, not vulnerable to isotropic components of a subsequent RIE procedure; insulator layer, 21a, for example a SOG layer with subsequent heat cycles, which is susceptible to isotropic components of a subsequent RIE procedure; and overlying insulator layer, 22, such as silicon oxide, which again is not prone to isotropic components of a subsequent RIE procedure. A photoresist shape, 23, with a sub-micron diameter opening, 24a, overlays the composite interlevel dielectric layer.

An anisotropic RIE procedure, using $CHF_3$ as an etchant, is used to create sub-micron diameter via hole, 24b, in the composite interlevel dielectric layer. However insulator layer, 21a, prone to an isotropic component of the RIE procedure, results in undercut region, 21b, shown schematically in Fig. 9. The undercut region will be further deformed during subsequent heat treatments, such as metal depositions. This undercut region can present problems when attempting to fill sub-micron diameter via hole, 21b, with a metal layer. If the subsequent metal layer does not conform to the undercut region, 21b, in sub-micron diameter via

hole, 24b, voids can be present between the subsequent metal layer and the undercut via hole, presenting regions in which unwanted and corrosive chemicals, used for subsequent processing steps, can be trapped. A solution to the undercut via hole is again the use of the insulator spacer. After removal of photoresist shape, 23, via plasma oxygen ashing and careful wet cleans, an insulator layer, of silicon oxide, 25, is deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 200 to 500 Angstroms. Insulator layer, 25, can again also be a silicon nitride layer. The excellent conformality of the PECVD silicon oxide layer, 25, allows deposition to occur on the sides of undercut region, 21b, as well as on the exposed bottom surface of insulator layer, 22, and on the exposed top surface of insulator layer, 20, thus completely filling undercut region, 21b. An anisotropic RIE procedure, using $CHF_3$ as an etchant, is again used to create insulator spacers, 25, schematically shown in Fig. 10. Argon sputter etching, again can be used to form insulator spacers, 25. Insulator spacers 25, filling undercut region, 21b, now exhibit a straight walled feature.

Fig. 11, schematically shows the creation of a metal interconnect structure, 26, contacting the top surface of the metal contact structure, 8, in sub-micron diameter via hole, 24b. Sub-micron diameter via hole, 24b, now exhibits a straight walled feature, resulting from filling of undercut region, 21b, with

insulator spacers, 25. This allows for a metal deposition of a adhesive layer of titanium, a barrier layer of titanium nitride, and an aluminum, with between about 0.5 to 3 % copper, to be performed using r.f. sputtering procedures, to a thickness between about 4000 to 10000 Angstroms. Conventional photolithographic and RIE procedures, using $Cl_2$ as an etchant, are employed to form metal interconnect structure, 26. The ability to create the straight walled sub-micron diameter via hole, 24b, allowed a voidless metal interconnect structure to be created. Photoresist removal is once again achieved via plasma oxygen ashing and careful wet cleans.

This invention can also be applied to contact hole processing, as shown schematically in Figs. 12 - 13. Contact hole, 30, formed via RIE using $CHF_3$ as an etchant, can result in the deposition of particles, 31, comprised of carbon, silicon and photoresist fragments, on the sides of contact hole, 30, unremovable during subsequent photoresist removal procedures. Again the deposition of an insulator layer, followed by either anisotropic RIE, or argon sputter etching, results in insulator spacers, 32, encapsulating particles, 31, on the sides of contact hole, 30.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

CLAIMS

1. A method for fabricating an insulator spacer, on the sides of a sub-micron diameter via hole, formed in an interlevel dielectric layer, wherein said insulator spacer encapsulates polymer residue material, located on the sides of said sub-micron diameter via hole, comprising the steps of:

depositing said interlevel dielectric layer on an underlying metal contact structure, and on an underlying thick insulator layer;

opening said sub-micron diameter via hole, in said dielectric layer, using photolithography and anisotropic dry etching procedures, exposing top surface of said metal contact structure, and forming polymer residue material, from anisotropic dry etching ambient, on the sides of said sub-micron diameter via hole;

depositing an insulator layer on top surface of said interlevel dielectric layer, and in said sub-micron diameter via hole, encapsulating said polymer residue material on sides of said sub-micron diameter via hole;

anisotropic etching to create said insulator spacer, on sides of said sub-micron diameter via hole, encapsulating said polymer residue material on the sides of said sub-micron diameter via hole;

depositing a metal interconnection layer; and

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etching of said metal interconnection layer using photolithography and dry etching techniques, to form an interconnect metal structure, contacting top surface of said metal contact structure, at the bottom of said sub-micron diameter via hole, and interfacing with said insulator spacer, on sides of said sub-micron diameter via hole, while overlying a region of the top surface of said interlevel dielectric layer.

2. The method of claim 1, wherein said interlevel dielectric layer is silicon oxide, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 10000 to 15000 Angstroms.

3. The method of claim 1, wherein said sub-micron diameter via hole is formed in said interlevel dielectric layer via anisotropic RIE procedures, using $CHF_3$ as an etchant.

4. The method of claim 1, wherein the diameter of said sub-micron diameter via hole is between about 0.4 to 0.8 uM.

5. The method of claim 1, wherein said polymer residue material is comprised of carbon, silicon, titanium, photoresist fragments, aluminum, and plasma gases.

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6. The method of claim 1, wherein said insulator layer is silicon oxide, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms.

7. The method of claim 1, wherein said insulator layer is silicon nitride, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms.

8. The method of claim 1, wherein said insulator spacer is formed on the sides of said sub-micron diameter via hole, by etching of said insulator layer, using anisotropic RIE procedures, using $CHF_3$ as an etchant, or formed via use of argon sputter etching.

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9. A method for fabricating an insulator spacer on the sides of a sub-micron diameter via hole, formed in a composite interlevel dielectric layer, with one of the layers of said composite interlevel dielectric layer being a SOG layer, wherein said insulator spacer covers exposed sides of said SOG layer, in said sub-micron diameter via hole, comprising the steps of:

depositing a composite interlevel dielectric layer comprised of an underlying PECVD insulator layer, a SOG layer, and an overlying PECVD insulator layer, on an underlying metal contact structure;

opening said sub-micron diameter via hole, in said composite interlevel dielectric layer, using photolithography and anisotropic dry etching procedures, exposing top surface of said metal contact structure, at the bottom of said sub-micron diameter via hole, and exposing the sides of said SOG layer, in said sub-micron diameter via hole;

depositing an insulator layer on the top surface of said composite interlevel dielectric layer, and in said sub-micron diameter via hole, covering exposed sides of said SOG layer, in said sub-micron diameter via hole;

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anisotropic dry etching to create said insulator spacer on sides of said sub-micron diameter via hole, in said composite interlevel dielectric layer, with said insulator spacers covering exposed sides of said SOG layer, in said sub-micron diameter via hole;

depositing a metal interconnection layer; and

etching of said metal interconnection layer, using photolithography and dry etching techniques, to create an interconnect metal structure, contacting top surface of said metal contact structure, at the bottom of said sub-micron diameter via hole, and interfacing with said insulator spacer, on the sides of said sub-micron diameter via hole, while overlying a region of the top surface of said composite interlevel dielectric layer.

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10. The method of claim 9, wherein said composite interlevel dielectric layer is comprised of: an underlying silicon oxide layer, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 3000 to 6000 Angstroms; a layer of SOG, applied and cured at a temperature between about 400 to 425°C, to a thickness between about 4000 to 5500 Angstroms, and etched back to a thickness between about 1500 to 3000 Angstroms; and an overlying silicon oxide layer, deposited using PECVD procedures, at a temperature between about 375 to 425°C, to a thickness between about 6000 to 8000 Angstroms.

11. The method of claim 9, wherein said sub-micron diameter via hole is formed in said composite interlevel dielectric layer using anisotropic RIE procedures, using $CHF_3$ as an etchant.

12. The method of claim 9, wherein the diameter of said sub-micron diameter via hole is between about 0.4 to 0.8 uM.

13. The method of claim 9, wherein said insulator layer is silicon oxide, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms.

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14. The method of claim 9, wherein said insulator layer is silicon nitride, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 100 to 400 Angstroms.

15. The method of claim 9, wherein said insulator spacer, is formed on the sides of said sub-micron diameter via hole, by etching of said insulator layer, via anisotropic RIE procedures, using $CHF_3$ used as an etchant, or formed using argon sputter etching procedures.

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16. A method for fabricating a straight walled insulator spacer, on the sides of a sub-micron diameter via hole, formed in an composite interlevel dielectric layer, wherein an insulator layer fills an undercut region, created in one of the layers of said composite interlevel dielectric layer during the anisotropic RIE procedure used to create sub-micron diameter via hole, comprising the steps of:

depositing said composite interlevel dielectric layer, comprised of an underlying insulator layer, a middle insulator layer, and an overlying insulator layer, on an underlying metal contact structure;

opening said sub-micron diameter via hole in said composite interlevel dielectric layer, using photolithography and anisotropic RIE procedures, exposing the top surface of said metal contact structure, with anisotropic RIE of said middle insulator layer exhibiting a lateral etch component, resulting in said undercut region of said middle insulator layer, wherein said opening in said middle insulator layer is larger in diameter then opening in said overlying insulator layer, and larger then opening in said underlying insulator layer;

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depositing said insulator layer on top surface of said composite interlevel dielectric layer, and in said sub-micron diameter via hole, filling said undercut region, in said middle insulator layer;

anisotropic RIE to create said straight walled insulator spacer on sides of said sub-micron diameter via hole, with said insulator layer filling said undercut region, in said middle insulator layer;

depositing a metal interconnection layer; and

etching of said metal interconnection layer, using photolithography and dry etching techniques, to form an interconnect metal structure, contacting top surface of said metal contact structure, at the bottom of said sub-micron diameter via hole, and interfacing said straight walled insulator spacer, on the sides of said sub-micron diameter via hole.

17. The method of claim 16, wherein said sub-micron diameter via hole is opened in said composite interlevel dielectric layer using anisotropic RIE procedures, using $CHF_3$ as an etchant.

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18. The method of claim 16, wherein the diameter of said sub-micron diameter via hole is between about 0.4 to 0.8 uM, with said undercut region of said middle insulator layer, of said composite interlevel dielectric layer, having a larger diameter opening then the opening in said sub-micron diameter via hole.

19. The method of claim 16, wherein said insulator layer is silicon oxide, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 200 to 500 Angstroms.

20. The method of claim 16, wherein said insulator layer is silicon nitride, deposited using PECVD procedures, at a temperature between about 350 to 400°C, to a thickness between about 200 to 500 Angstroms.

21. The method of claim 16, wherein said straight walled insulator spacer is formed on the sides of said sub-micron diameter via hole, by etching of said insulator layer via anisotropic RIE procedures, using $CHF_3$ as an etchant.

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