ABSTRACT OF THE DISCLOSURE

METHOD FOR FORMING A LOW IMPURITY DIFFUSION POLYSILICON LAYER

A method for forming within an integrated circuit a low impurity diffusion polysilicon layer. Formed upon a semiconductor substrate is an amorphous silicon layer. Formed also upon the semiconductor substrate and contacting the amorphous silicon layer is a polysilicon layer. The amorphous silicon layer and the polysilicon layer are then simultaneously annealed to form a low impurity diffusion polysilicon layer. The low impurity diffusion polysilicon layer is a polysilicon multi-layer with grain boundary mis-matched polycrystalline properties. Optionally, a metal silicide layer may be formed upon the amorphous silicon layer and the polysilicon layer either prior to or subsequent to annealing the amorphous silicon layer and the polysilicon layer. The metal silicide layer and low impurity diffusion polysilicon layer may then be patterned to form a polycide gate electrode.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)