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Method for the production of a contact hole to a doped region.

In the production of integrated circuits, the completion of the individual components, mainly MOS transistors, is followed by the formation of at least one interconnection plane, which interconnects the components.

In conventional technologies, a relatively thick insulating layer, generally made of silicon oxide with additives, is deposited for this purpose. With the aid of a photoresist mask, contact holes are etched anisotropically, that is to say with a vertical preferred direction, through this insulating layer down to those regions of the components with which contact is to be made. Contact is to be made, inter alia, with gates or doped regions of the transistors. A metallization layer, for example an AlSiCu alloy is deposited. The metallization layer fills the contact holes and forms a continuous layer at the surface of the insulating layer. This continuous layer is structured in order to complete the interconnection plane.

In this procedure, the contact holes must be positioned in such a way that a safety clearance is preserved in each case between the location of the contact hole and adjacent conductive regions in or on the surface of the substrate. Particularly when contact is made with doped regions of an MOS transistor, a safety clearance from adjacent gate electrodes must be preserved in order to avoid short circuits. This clearance must be large enough to reliably absorb unavoidable process and alignment tolerances. This safety clearance causes space to be lost, and this loss has a particularly disturbing effect in the case of miniaturized integrated circuits having an extreme component density, for example DRAMs.

Methods which avoid this disadvantage are disclosed in the literature.

K. H. Küsters et al., Sympos. on VLSI Technology, 1987, Tech. Digest p. 93 ff. discloses shrouding the gate electrodes, prior to the deposition of the thick insulating layer, with an insulating covering layer and insulating side coverings, so-called spacers. A thin auxiliary layer made, for example, of silicon nitride is subsequently deposited. After this, the thick insulating layer is deposited and the contact holes are opened therein. The auxiliary layer acts as an etching resist in this case. In the opened contact holes, the auxiliary layer is subsequently etched away selectively with respect to the substrate and to the insulation enveloping the gate electrodes. In this method, the contact holes can be placed such that they overlap the gate electrodes. This method necessitates a high etching selectivity of silicon nitride with respect to the insulation enveloping the gate electrodes, generally silicon oxide.

K. H. Küsters et al., ESSDERC 1988, Journal de Physique, p. 503 ff. discloses a further method, which can be used when the etching selectivity of silicon nitride with respect to oxide is insufficient. In this method, a thin layer made of polysilicon is additionally deposited over the auxiliary layer made of silicon nitride. After the contact hole etching through the thick insulating layer, in which the thin polysilicon layer acts as an etching resist, first of all the polysilicon is etched selectively with respect to the silicon nitride and then the silicon nitride is etched selectively with respect to the substrate.

Outside the contact regions, the polysilicon layer remaining under the insulating layer is later oxidized by means of suitable tempering in an O_2 atmosphere. This process step is very problematic.

In both of the known methods, use is made of auxiliary layers which have to be removed again completely in the contact hole region.

In the two known methods, it is fundamentally impossible simultaneously to open contact holes to doped regions in the substrate, source/drain regions and to

gate electrodes made of polysilicon. The contact holes to the gate electrodes must be opened after the silicon nitride etching.

The invention is based on the problem of specifying a further method for the production of a contact hole to a doped region which avoids the removal of auxiliary layers in the contact region and is particularly suitable for simultaneously opening contact holes to source/drain regions and gate electrodes.

The problem is solved according to the invention by means of a method according to Claim 1. Further refinements of the invention emerge from the remaining claims.

In the method according to the invention, use is made of the fact that undoped silicon can be removed selectively with respect to doped silicon. The undoped silicon layer, which is amorphous, for example, is selectively doped in the region of the later contact, for example by means of ion implantation using a mask. The undoped part [sic] of the silicon layer are subsequently removed selectively with respect to the doped zone. An insulation layer is produced over the whole area, in which layer the contact hole is opened by means of anisotropic etching selectively with respect to the doped zone of the silicon layer. The doped zone of the silicon layer acts as an etching resist in this case. The silicon layer introduced as an auxiliary layer no longer needs to be removed in the region of the contact hole.

It is particularly advantageous to produce the silicon layer in such a way that it consists of polysilicon at least in the doped zone, since silicon oxide, which as a rule the insulation layer essentially comprises, can be etched with a high selectivity with respect to polysilicon.

The problematic later oxidation of the silicon layer required in the prior art is omitted, since the undoped parts of the silicon layer are removed outside the contact hole.

Setting a high doping in the doped zone of the

silicon layer results in the presence of a readily conductive, extended contact area at the surface of the doped region with which contact is to be made. It is thereby possible to achieve low contact resistances for the contacts which are formed by a metallization layer filling the contact hole.

The method enables simultaneous opening of contact holes to gate electrodes made of polysilicon. If the insulating covering layer of the gate electrodes and the insulation layer essentially consists of silicon oxide, then during the contact hole etching, the polysilicon of the gate electrode acts as an etching resist in the region of the gate electrode and the doped zone of the silicon layer acts as an etching resist in the region of the doped region.

The invention is explained in more detail below using an exemplary embodiment with reference to the figures.

Figure 1 shows a substrate in which MOS transistors are produced and on the surface of which a silicon layer is produced.

Figure 2 shows the selective doping of the silicon layer.

Figure 3 shows the doped zone of the silicon layer which overlaps the contact hole region 4.

Figure 4 shows the contact hole in the insulation layer.

Doped regions 2 are arranged in a substrate 1 made, for example, of monocrystalline silicon. The doped regions 2 are, for example, source or drain regions of MOS transistors. They are p-doped, for example.

Gate electrodes 3 made of doped polysilicon are arranged on the surface of the substrate 1, between two doped regions 2 which act as the source region and the drain region. The gate electrodes 3 are provided with an insulating covering layer 4 made, for example, of SiO_2. Arranged on the sides of the gate electrodes 3 and of the insulating covering layer 4 are spacers 5, which likewise consist, for example, of SiO_2.

A silicon layer 6 is produced over the whole

area, which layer covers the exposed surfaces of the doped regions 2 and the surfaces of the insulating covering layers 4 and of the spacers 5. The silicon layer 6 is deposited in an amorphous or polycrystalline form. The silicon layer 6 is undoped (see Figure 1).

A photoresist mask 7 is produced which leaves uncovered a zone of the silicon layer 6 which reliably overlaps the extent of the later contact hole. Using the photoresist mask 7 as an implantation mask, a doped zone 61 of the silicon layer is produced by implantation with boron, for example, indicated by the arrows 8. The implantation takes place, for example, at an ion energy of 10 keV and a particle density of 10^{15} cm^{-2} (see Figure 2).

Following removal of the photoresist mask 7, the undoped part of the silicon layer 6 is removed selectively with respect to the doped zone 61 by means of selective wet-chemical etching using potassium hydroxide solution (see Figure 3).

After an insulation layer 9, which essentially consists of SiO_2, for example, has been applied over the whole area, a contact hole 10 is opened, using a further photoresist mask (not illustrated) as an etching mask, by means of reactive ion etching using CF_6, for example. During the contact hole etching, the doped zone 61 of the silicon layer acts as an etching resist (see Figure 4).

If the intention is to open contact holes to the gate electrodes in the same process, it must be ensured that the doped zone of the silicon layer does not overlap the region for the contact hole to the gate electrode. The contact hole to the gate electrode is opened through the insulation layer and the insulating covering layer.

Patent Claims

1. Method for the production of a contact hole to a doped region,
- in which the doped region (2) is produced in the substrate (1) in such a way that it is bounded by insulation regions (5) at least on the surface of the substrate (1),
- in which an undoped silicon layer (6) is deposited over the whole area,
- in which a doped zone (61), which reliably overlaps the region for the contact hole (10), is selectively produced in the silicon layer (6),
- in which undoped parts of the silicon layer (6) are removed selectively with respect to the doped zone (61),
- in which an insulation layer (9) is produced over the whole area,
- in which the contact hole (10) is opened in the insulation layer (9) by means of anisotropic etching selectively with respect to the doped zone (61) of the silicon layer (6).

2. Method according to Claim 1, in which the substrate (1) consists of monocrystalline silicon.

3. Method according to Claim 1 or 2, in which the silicon layer (6) is produced from amorphous silicon.

4. Method according to one of Claims 1 to 3, in which the undoped parts of the silicon layer (6) are removed by wet-chemical etching.

5. Method according to one of Claims 1 to 4, in which the doped zone (61) in the silicon layer (6) is produced by implantation using a mask (7).

6. Method according to one of Claims 1 to 5, in which the doped zone (61) of the silicon layer (6) is p-doped, and in which the undoped parts of the silicon layer (6) are removed by means of wet-chemical etching using potassium hydroxide solution.

7. Method according to Claim 6, in which a boron concentration of between 10^{18} cm^{-3} and 10^{20} cm^{-3} is set in

the doped zone (61) of the silicon layer (6).

8. Method according to one of Claims 1 to 7,

- in which the doped region (2) in the substrate (1) is a source/drain region of an MOS transistor,
- in which the insulation regions include insulating side coverings (5) and insulating covering layers (4) of the gate electrode (3) of the MOS transistor.

9. Method according to Claim 8,

- in which the doped region (2) in the substrate (1) is p-doped,
- in which the doped zone (61) of the silicon layer (6) is p-doped,
- in which the gate electrode (3) is formed from polysilicon,
- in which the insulating side coverings (5) and the insulating covering layers (4) are formed from silicon oxide.

10. Method according to Claim 9,

- in which the insulation layer (9), in which the contact hole (10) is opened, comprises SiO_2,
- in which a further contact hole to the gate electrode (3) is opened at the same time that the contact hole (10) to the doped region (2) is opened.