

TITLE OF INVENTION**PRECISION STAGE CLOCK SYNCHRONIZATION SYSTEM****CROSS REFERENCE TO RELATED APPLICATION**

- 5 This patent application claims the benefit of priority of Singapore Patent Application No. 10202403270Y, filed 22 October 2024. The above application is incorporated by reference herein.

BACKGROUND OF THE INVENTION**A. Field of The Invention**

- 10 The present invention relates generally to precision positioning stages and motion control systems. More particularly, the invention relates to systems and methods for synchronizing multiple clock domains within a precision stage controller to eliminate signal aliasing and improve positioning accuracy, precision, and settling time.

B. Description of Prior Art

- 15 Precision positioning stages are critical components in various applications including semiconductor manufacturing, microscopy, metrology, and precision assembly. These stages require sub-nanometer positioning accuracy and fast settling times to meet increasingly stringent performance requirements.

- 20 Conventional precision stage control systems typically integrate off-the-shelf control and sensing components or subsystems that operate within different, asynchronous clock domains. This modular approach, while convenient from a design and manufacturing perspective, introduces significant technical challenges.

- 25 When control signals, such as motor pulse-width modulation (PWM) signals, operate asynchronously relative to position feedback signals from encoders or other position sensors, aliasing of sensor and control signals can occur within the feedback loops that control the stage. This aliasing phenomenon manifests as position disturbances that corrupt the position feedback signal, potentially destabilizing the feedback loop or introducing error artifacts that increase tracking error and prolong settling time.

For ultra-precision stages designed to achieve sub-nanometer performance, such degradation in precision and accuracy is unacceptable. The asynchronous nature of multiple clock domains creates a fundamental barrier to achieving the highest levels of positioning performance.

5 What is needed is a precision stage control system that eliminates aliasing through systematic synchronization of all clock domains within the control system, thereby enabling superior positioning precision, accuracy, and settling time.

BRIEF SUMMARY OF THE INVENTION

10 The present invention addresses the aforementioned need by providing a precision stage clock synchronization system, wherein the frequency of each clock in the system is an integer multiple of the slowest clock in the system, thereby eliminating aliasing of sensor and control signals within feedback loops.

A main object of the present invention is to provide a precision stage control system comprising:

15 having a servo update frequency (f_{SERVO}), wherein the servo update frequency is the lowest frequency within the control system;

motor drive circuitry operating at a motor pulse-width modulation frequency ($f_{\text{M_PWM}}$) that is an integer multiple of the servo update frequency;

20 power supply circuitry operating at a power supply pulse-width modulation frequency ($f_{\text{S_PWM}}$) that is an integer multiple of the servo update frequency; and encoder and inertial sensing (together sensor) sampling circuitry operating at an encoder sampling frequency ($f_{\text{E_S}}$) that is an integer multiple of the servo update frequency; whereby aliasing of sensor and control signals within feedback loops is eliminated.

25 In accordance with one aspect of the invention, a precision stage control system comprises a master clock generator that generates a servo update clock signal having a servo update frequency (f_{SERVO}), wherein the servo update frequency is the lowest frequency within the control system. The system further comprises multiple subsystems including motor drive circuitry, power supply circuitry, sensor sampling circuitry, feed-forward injection circuitry, state estimator circuitry, and encoder illumination circuitry, wherein each subsystem operates at a
30 frequency that is an integer multiple of the servo update frequency.

In accordance with another aspect of the invention, the master clock generator is implemented within an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) integrated within a main controller board, and clock signals are distributed without phase-shift or distortion to control components and subsystems.

5 In accordance with yet another aspect of the invention, clock distribution in distributed systems is achieved using point-to-point, high-frequency communication channels implementing low-voltage differential signaling (LVDS) or other suitable differential signaling protocols, including those employed in multi-gigabit transfer protocols that incorporate Multi-Gigabit Transceivers (MGT). Examples include network protocols like Gigabit Ethernet, PCI-e, and also point-to-
10 point Serial/Deserializer (SerDes)-based interfaces that extend parallel data from one circuit assembly to a remote circuit assembly, thereby promoting memory-to-memory transfers between embedded processors.

In accordance with a further aspect of the invention, precision time protocol (PTP), Ethernet synchronization (Synch E), and time-sensitive networking (TSN) employing digital phase-lock
15 loops (DPLL) are used to synchronize networked components including AC/DC power supplies, motor power supplies, and encoder feedback sensors with the centralized master clock.

In accordance with another aspect of the invention, the servo update frequency is adjustable during normal operation such that its period at any time is an integer multiple (N_{SUO}) of the
20 period when operated at its highest reference frequency (f_{SERVO}), thereby scaling the integer frequency relationships by the scale factor N_{SUO} to increase stage actuator control precision by a factor of N_{SUO} .

These and other features, aspects and advantages of the present invention will become better understood with reference to the following drawings, description and claims.

25

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

A fuller understanding of the nature and objects of the present invention will become apparent upon consideration of the following detailed description, taken in connection with the accompanying drawing, wherein:

30 Figure 1 is a block diagram illustrating the precision stage clock synchronization system showing the hierarchical relationship between the servo update frequency and the various subsystem frequencies, each being an integer multiple of the servo update frequency.

DETAILED DESCRIPTION OF THE INVENTION

5 The following detailed description is of the best currently contemplated modes of carrying out exemplary embodiments of the invention. The description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention, since the scope of the invention is best defined by the appended claims.

Referring to FIG. 1, broadly, which shows a block diagram illustrating the precision stage clock synchronization system showing the hierarchical relationship between the servo update
10 frequency and the various subsystem frequencies, each being an integer multiple of the servo update frequency.

Referring to Figure 1, a precision stage clock synchronization (PSCS) system 100 is illustrated. The PSCS system 100 synchronizes multiple clock domains within a controller of a precision stage to eliminate aliasing of sensor and control signals within feedback loops that
15 control the stage.

In accordance with a preferred embodiment of the present invention the frequency of each clock in the system is established as an integer multiple of the slowest clock in the system. This relationship ensures that all signal transitions and sampling events throughout the control system occur at predictable, phase-coherent instants, thereby eliminating the random phase
20 relationships that characterize asynchronous systems and give rise to aliasing artifacts.

In the PSCS system 100, the servo update frequency (f_{servo}) serves as the fundamental timing reference and represents the lowest frequency within the control system. The servo update frequency determines the rate at which the position feedback loop is closed and new control commands are computed and issued to the stage actuators.

25 All other frequencies within the system are derived as integer multiples of the servo update frequency (f_{servo}), establishing a coherent timing hierarchy that pervades the entire control system.

The following subsystem frequencies are each established as integer multiples of the servo update frequency (f_{servo}):

- (i) Motor Pulse-Width Modulation Frequency (f_{M_PWM}): The motor PWM frequency controls the switching rate of power transistors in the motor drive electronics. By establishing $f_{M_PWM} = N_{M_PWM} \times f_{SERVO}$, where N_{M_PWM} is an integer, the PWM switching transitions occur at predictable phases relative to position sampling events, eliminating aliasing of PWM-induced position disturbances into the feedback signal.
- (ii) Motor Power Supply Boost-Buck PWM Frequency (f_{S_PWM}): The power supply PWM frequency controls DC-DC, and in the case of power factor correction AC-DC, converter switching in the motor power supply. Establishing $f_{S_PWM} = N_{S_PWM} \times f_{SERVO}$ ensures that power supply ripple and switching noise occur at frequencies that maintain coherent phase relationships with the servo update, preventing aliasing of the resulting force or torque disturbances into the control loop.
- (iii) Sensor Sampling Frequencies (f_{E_S}): This sampling frequency determines how often position measurements are acquired from optical or magnetic encoders and inertial sensors. Setting $f_{E_S} = N_{E_S} \times f_{SERVO}$ ensures that position samples are acquired at instants that are phase-coherent with the servo computation cycle. Here, we consider f_{E_S} as a vector of frequencies since sensor information from different sensors may integrate with feedforward and feedback loops, and multi-modal information-theoretic filters (e.g. Kalman Filters) at different rates.
- (iv) Feed-Forward Injection Frequency (f_{FF}): Feed-forward control signals are injected at frequency $f_{FF} = N_{FF} \times f_{SERVO}$ to provide predictive compensation for known disturbances or commanded trajectory profiles.
- (v) State Estimator Frequency (f_{SE_S}): State estimation algorithms, such as Kalman filters or observers, operate at frequency $f_{SE_S} = N_{SE_S} \times f_{SERVO}$ to generate estimates of unmeasured state variables while maintaining synchronization with the primary control loop.
- (vi) Encoder LED/Laser Modulation Frequency (f_{L_M}): Optical encoders employ modulated illumination sources (LEDs or lasers) to improve signal-to-noise ratio and reduce DC drift. The modulation frequency is set to $f_{L_M} = N_{L_M} \times f_{SERVO}$ to maintain phase coherence with position sampling.
- (vii) Oversampling Clock Frequencies: Modern analog-to-digital converters often employ delta-sigma modulation or other oversampling techniques. The oversampling clocks for various measurement channels are synchronized as

follows: Motor power supply current measurement: $f_{OS_MP} = N_{OS_MP} \times f_{SERVO}$;- Motor power supply voltage measurement: $f_{OS_PS} = N_{OS_PS} \times f_{SERVO}$;- Motor current measurement: $f_{OS_MI} = N_{OS_MI} \times f_{SERVO}$;- Photodiode analog-to-digital conversion: $f_{OS_PD} = N_{OS_PD} \times f_{SERVO}$. Converters employing these synchronized, oversampling clocks can be configured to intrinsically “average” over an integral number of the PWM or other disturbance-generating frequencies thereby eliminating the error introduced by the disturbance.

In each case, N_{xx} represents an integer multiplier that establishes the frequency relationship. The specific values of these integers are selected based on the bandwidth requirements of each subsystem, noise considerations, and implementation constraints.

First Preferred Embodiment: Centralized ASIC/FPGA Clock Generation

In a first preferred embodiment, the PSCS system 100 achieves synchronization by centralizing clock generation within an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) integrated within a main controller board.

The ASIC or FPGA contains a master clock generator that produces the servo update frequency f_{SERVO} and all derived frequencies through integer division or multiplication of a common reference oscillator. Clock synthesis circuits within the ASIC/FPGA, such as phase-locked loops (PLLs), delay-locked loops (DLLs), or direct digital synthesis (DDS) circuits, generate the required clock signals with precise frequency and phase relationships.

The clock signals are then distributed from the ASIC/FPGA to the various control components and subsystems, including power supplies, motor power electronics, and encoder feedback sensors. Distribution is accomplished using buffered clock distribution networks designed to minimize phase-shift, skew, and distortion of the clock signals.

In distributed systems where control components are physically separated across multiple circuit boards or enclosures, clock distribution is achieved using point-to-point, high-frequency communication channels. These MGT-based channels preferably implement low-voltage differential signaling (LVDS), which provides excellent noise immunity, low electromagnetic interference (EMI), and the ability to transmit high-frequency signals over moderate distances with minimal distortion.

Alternative differential signaling standards that may be employed include current-mode logic (CML), positive emitter-coupled logic (PECL), or proprietary differential signalling schemes optimized for specific applications.

5 **Second Preferred Embodiment: Network-Based Clock Synchronization**

In a second preferred embodiment particularly suited to systems with geographically distributed components, clock synchronization is achieved using network-based timing protocols.

The precision time protocol (PTP), as defined in IEEE 1588, provides sub-microsecond synchronization accuracy over packet-based networks. In this embodiment, a PTP grandmaster clock is implemented within or connected to the main controller, and PTP slave clocks are implemented within remote components such as distributed power supplies and encoder heads.

Ethernet synchronization (Synch E), as defined in ITU-T recommendations, provides frequency synchronization by recovering timing information from the physical layer of Ethernet communications. Digital phase-lock loops (DPLL) at each node lock to the recovered timing signal, establishing frequency coherence across the network.

Time-sensitive networking (TSN), comprising a suite of IEEE 802.1 standards, provides deterministic, low-latency communication with guaranteed bandwidth and bounded jitter. TSN ensures that timing information and control commands are delivered with predictable latency, supporting the tight synchronization required for precision control.

In this embodiment, the precision stage clock synchronization (PSCS) timing hierarchy is projected onto these network protocols. The networked components, including AC/DC power supplies, motor power supplies, and encoder feedback sensors, receive timing information via the network and generate their local operating frequencies as integer multiples of the network-synchronized master frequency.

This approach provides exceptional flexibility for systems requiring distributed intelligence, modular reconfiguration, or integration with enterprise manufacturing execution systems while maintaining the tight clock synchronization required for eliminating aliasing.

Third Preferred Embodiment: Adaptive Servo Update Frequency

In a third preferred embodiment, the servo update frequency f_{SERVO} is adjustable during normal operation to optimize control performance under varying conditions.

In this embodiment, a reference servo update frequency f_{SERVO} represents the highest servo update rate at which the system is designed to operate. During operation, the actual servo update frequency f_{SERVO} may be reduced by an integer factor N_{SU0} such that:

$$f_{\text{SERVO}} = f_{\text{SERVO}} / N_{\text{SU0}}$$

where N_{SU0} is an integer scaling factor.

Correspondingly, the period of the servo update clock becomes:

10

$$T_{\text{SERVO}} = N_{\text{SU0}} \times T_{\text{SERVO}}$$

where T_{SERVO} is the period at the reference frequency.

When the servo update frequency is reduced by the factor N_{SU0} , all other system frequencies are similarly scaled, maintaining their integer multiple relationships relative to f_{SERVO} . This preserves the aliasing-free operation while allowing the servo update rate to be adapted to the instantaneous requirements of the positioning task.

The benefit of this adaptive approach is that the stage actuator control precision is effectively increased by the factor N_{SU0} . When the servo operates at a lower rate, the control algorithm has more computational time available, allowing the use of higher-resolution calculations, more sophisticated control algorithms, or more extensive filtering of sensor signals. Here, integrating converters like delta-sigma and voltage-to-frequency can be configured to increase precision as the sampling rate decreases thereby directly increasing the positioning precision needed for ultra-precision applications.

For example, when $N_{\text{SU0}} = 4$, the servo update rate is reduced by a factor of four, but the computational resolution available for each servo update is quadrupled. This is particularly advantageous during fine positioning or settling phases where the motion is slow and the primary objective is to minimize positioning error rather than to achieve high bandwidth.

The adaptive servo update frequency may be controlled automatically based on measured stage velocity, acceleration, positioning error, or disturbance spectrum, or may be similarly commanded explicitly by higher-level control or sequencing software.

In accordance with the present invention, the advantages of the invention are as follows:

- 5 (i) Elimination of Aliasing: By ensuring all frequencies are integer multiples of the servo update frequency, the system eliminates the random phase relationships that cause aliasing of control signals into feedback signals. Such aliasing can destabilize the control system dynamics.
- 10 (ii) Improved Positioning Precision: The elimination of aliasing artifacts directly translates to reduced positioning error, enabling achievement of sub-nanometer positioning precision.
- 15 (iii) Enhanced Accuracy: Systematic error sources related to aliasing are eliminated, improving absolute positioning accuracy.
- 20 (iv) Reduced Settling Time: The absence of aliasing-induced disturbances allows feedback loops to be tuned more aggressively, reducing settling time without risking instability.
- 25 (v) Simplified Analysis and Tuning: The deterministic, phase-coherent nature of the synchronized system makes control system analysis and tuning more straightforward compared to asynchronous systems where statistical analysis of aliasing effects is required.
- 30 (vi) Scalability: The network-based synchronization embodiment provides excellent scalability for complex, multi-axis systems or systems requiring distributed control components.
- 35 (vii) Adaptability: The adaptive servo update frequency embodiment provides optimization of the precision-bandwidth trade off based on instantaneous positioning requirements.

While the invention has been described with reference to specific preferred embodiments, those skilled in the art will recognize that various modifications and alternative implementations are possible without departing from the scope of the invention. For example, while specific signalling standards such as LVDS have been mentioned for clock distribution, any suitable signalling method that preserves clock integrity may be employed. Similarly, while

specific network synchronization protocols (PTP, Synch E, TSN) have been described, other network timing protocols may be used. The specific integer multipliers N used to derive subsystem frequencies from the servo update frequency may be selected based on the requirements of specific applications, and different values may be optimal for different types of stages, actuators, or sensors. The master clock generation function, while described as implemented in an ASIC or FPGA, could alternatively be implemented using discrete clock synthesis ICs, microcontrollers with integrated clock generation capabilities, or other suitable circuitry.

CLAIMS

1. A precision stage control system comprising:

a master clock generator configured to generate a servo update clock signal having a servo update frequency (f_{SERVO}), wherein the servo update frequency is the lowest frequency within

5 the control system;

motor drive circuitry operating at a motor pulse-width modulation frequency ($f_{\text{M_PWM}}$) that is an integer multiple of the servo update frequency;

power supply circuitry operating at a power supply pulse-width modulation frequency ($f_{\text{S_PWM}}$) that is an integer multiple of the servo update frequency; and

10 sensor sampling circuitry operating at an encoder sampling frequency ($f_{\text{E_S}}$) that is an integer multiple of the servo update frequency; whereby aliasing of sensor and control signals within feedback loops is eliminated.
2. The precision stage control system of claim 1, further comprising:

feed-forward injection circuitry operating at a feed-forward injection frequency (f_{FF}) that is an

15 integer multiple of the servo update frequency;

state estimator circuitry operating at a state estimator frequency ($f_{\text{SE_S}}$) that is an integer multiple of the servo update frequency; and

encoder illumination circuitry operating at an encoder illumination modulation frequency ($f_{\text{L_M}}$) that is an integer multiple of the servo update frequency.
- 20 3. The precision stage control system of claim 1, wherein the master clock generator comprises an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) integrated within a main controller board.
4. The precision stage control system of claim 3, wherein clock signals are distributed from the master clock generator to control components and subsystems without phase-shift
- 25 or distortion.
5. The precision stage control system of claim 1, wherein clock distribution to distributed system components is achieved using point-to-point, high-frequency communication channels implementing low-voltage differential signaling (LVDS).

6. The precision stage control system of claim 1, further comprising analog-to-digital conversion circuitry for measuring at least one of motor power supply current, motor power supply voltage, motor current, and photodiode signals, wherein the analog-to-digital conversion circuitry operates with an oversampling clock frequency (f_{OS}) that is an integer multiple of the servo update frequency.
7. The precision stage control system of claim 1, wherein clock synchronization is achieved using precision time protocol (PTP) and digital phase-lock loops (DPLL) to synchronize networked components with the master clock generator.
8. The precision stage control system of claim 7, wherein the networked components include AC/DC power supplies, motor power supplies, encoder feedback sensors, and inertial sensors.
9. The precision stage control system of claim 1, wherein clock synchronization is achieved using Ethernet synchronization (Synch E), time-sensitive networking (TSN), and MGT-based Ser-Desprotocols.
10. The precision stage control system of claim 1, wherein the servo update frequency is adjustable during operation such that a period of the servo update clock signal at any time is an integer multiple (N_{SU0}) of a period when operated at a highest reference frequency (f_{SERVO}), thereby scaling integer frequency relationships by a scale factor N_{SU0} .
11. The precision stage control system of claim 10, wherein adjusting the servo update frequency increases stage actuator control precision by a factor of N_{SU0} .
12. The precision stage control system of claim 10, wherein the servo update frequency is adjusted automatically based on at least one of measured stage velocity, acceleration, positioning error, and the stage disturbance spectrum.
13. A method for controlling a precision stage, comprising:
 - generating a servo update clock signal having a servo update frequency (f_{SERVO}), wherein the servo update frequency is the lowest frequency used in control of the precision stage;
 - deriving a plurality of subsystem clock signals, each having a frequency that is an integer multiple of the servo update frequency;
 - operating motor drive circuitry using a first subsystem clock signal;
 - operating power supply circuitry using a second subsystem clock signal; and

operating encoder sampling circuitry using a third subsystem clock signal; whereby aliasing of sensor and control signals within feedback loops is eliminated.

14. The method of claim 13, further comprising distributing the subsystem clock signals using low-voltage differential signaling (LVDS) to maintain signal integrity.

- 5 15. The method of claim 13, further comprising synchronizing networked components using precision time protocol (PTP) such that the networked components operate at frequencies that are integer multiples of the servo update frequency.