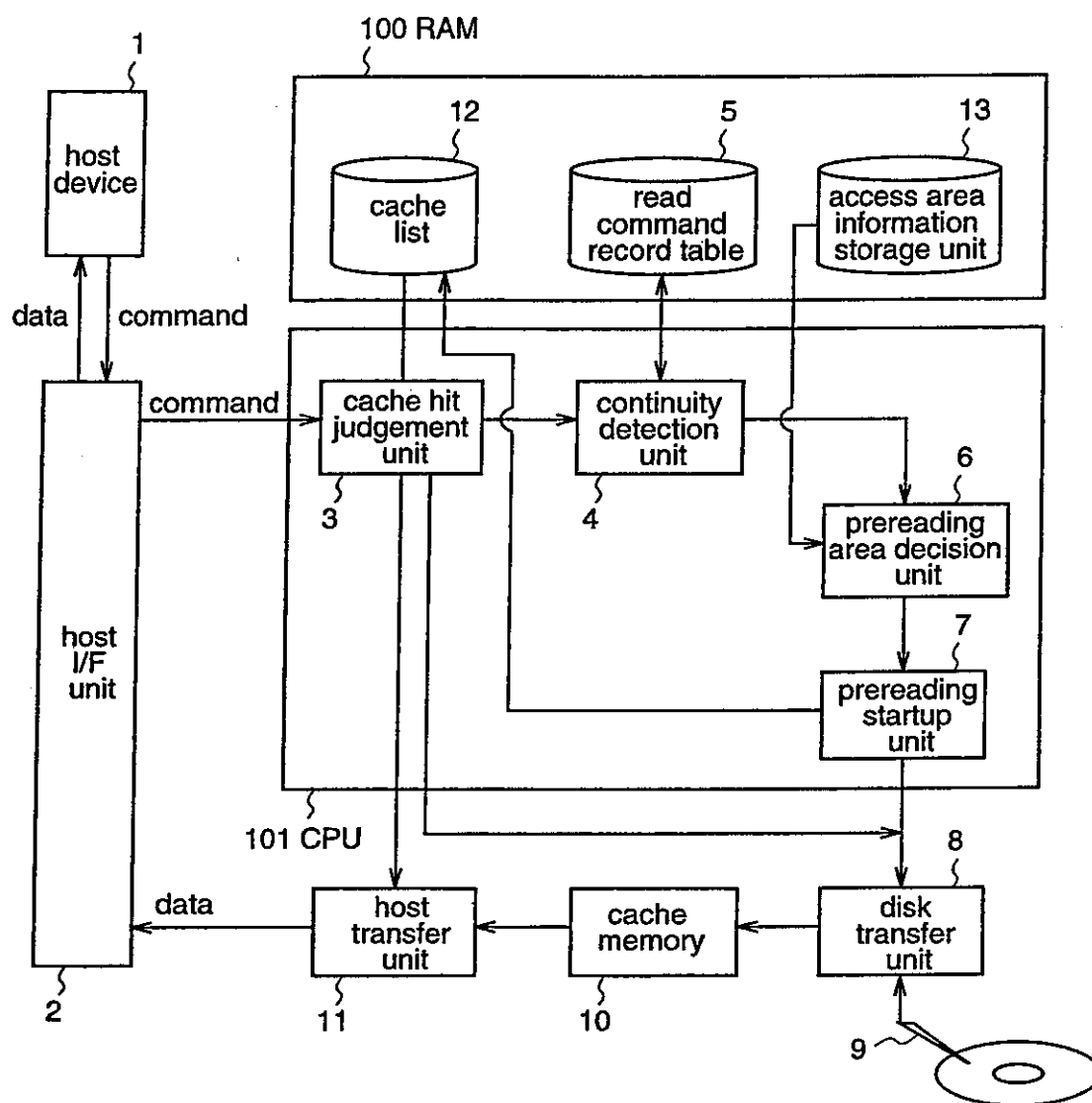
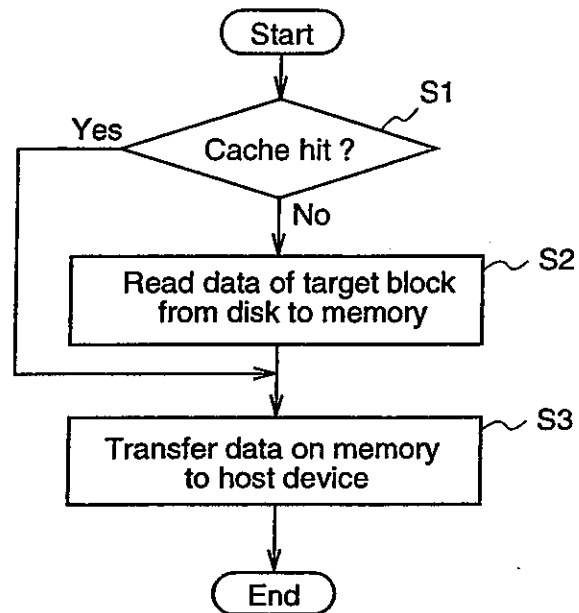


Fig.1



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Fig.2



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Fig.3

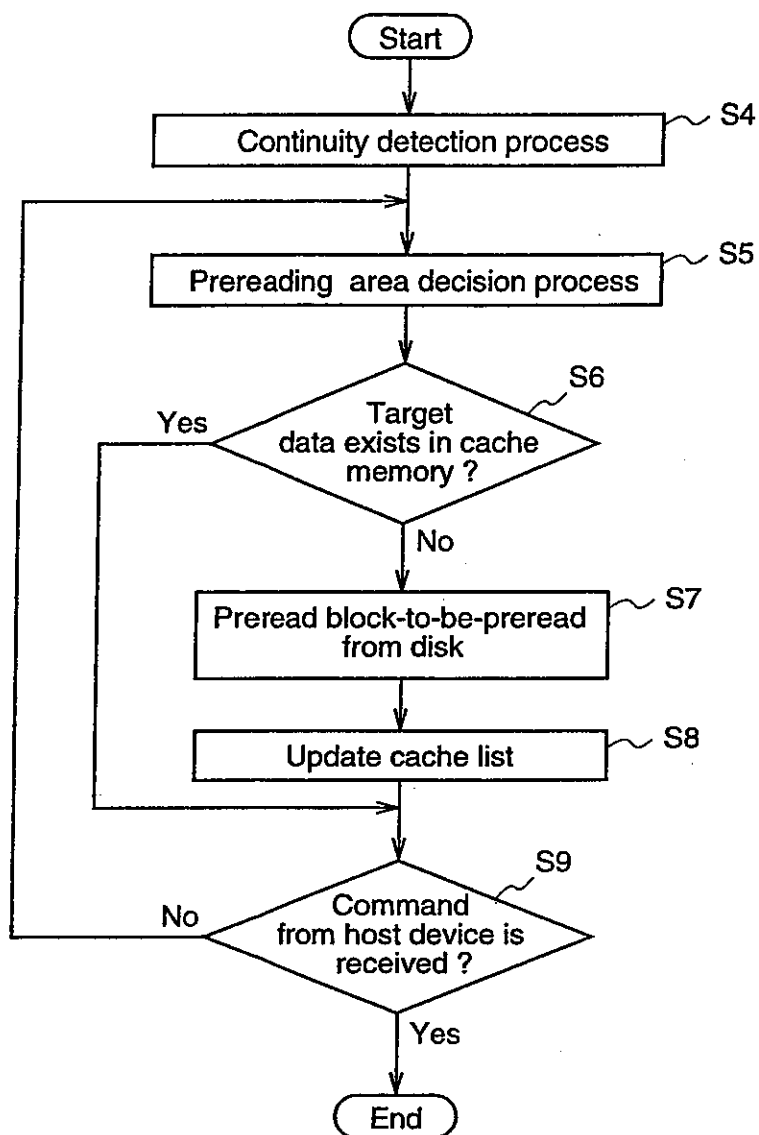


Fig.4

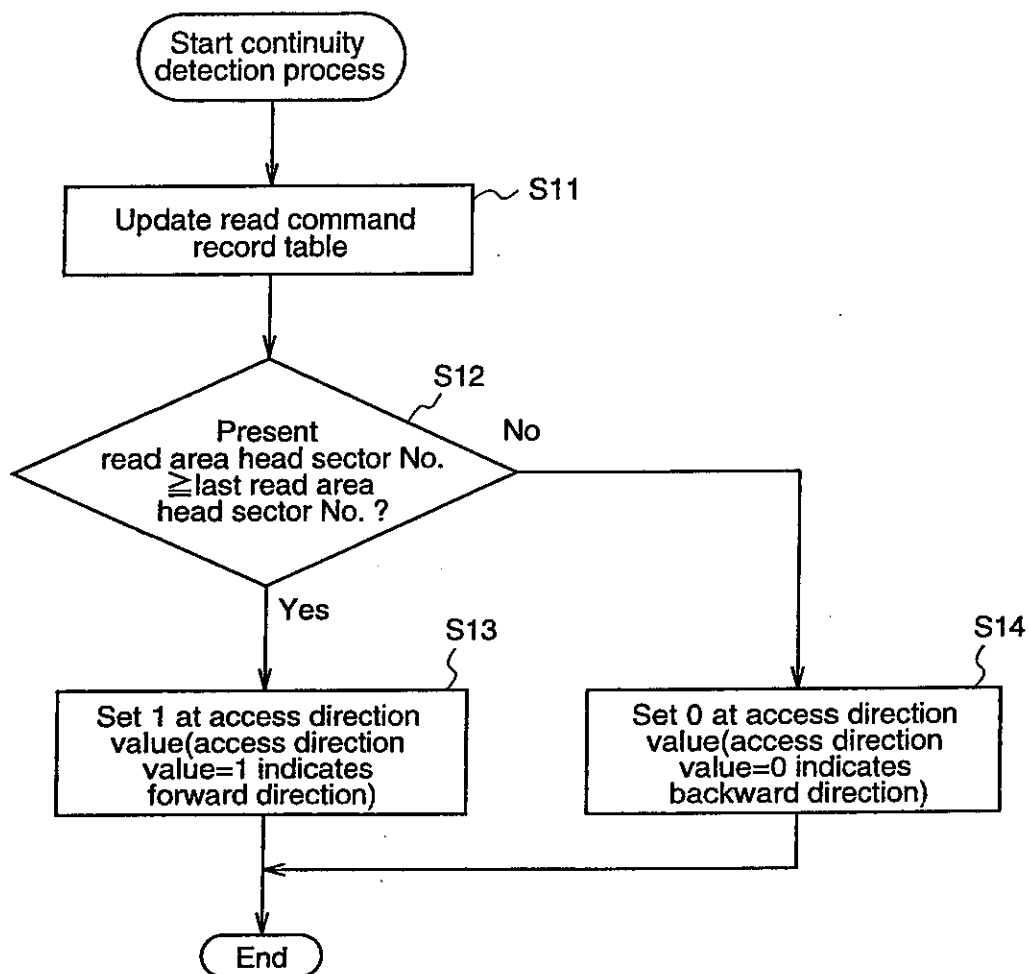


Fig.5

present read area head sector No.
 present read area size
 last read area head sector No.
 last read area size
 last-but-one read area head sector No.
 last-but-one read area size
 present access direction value
 last access direction value

G
H
A
B
C
D
I
E

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Fig.6

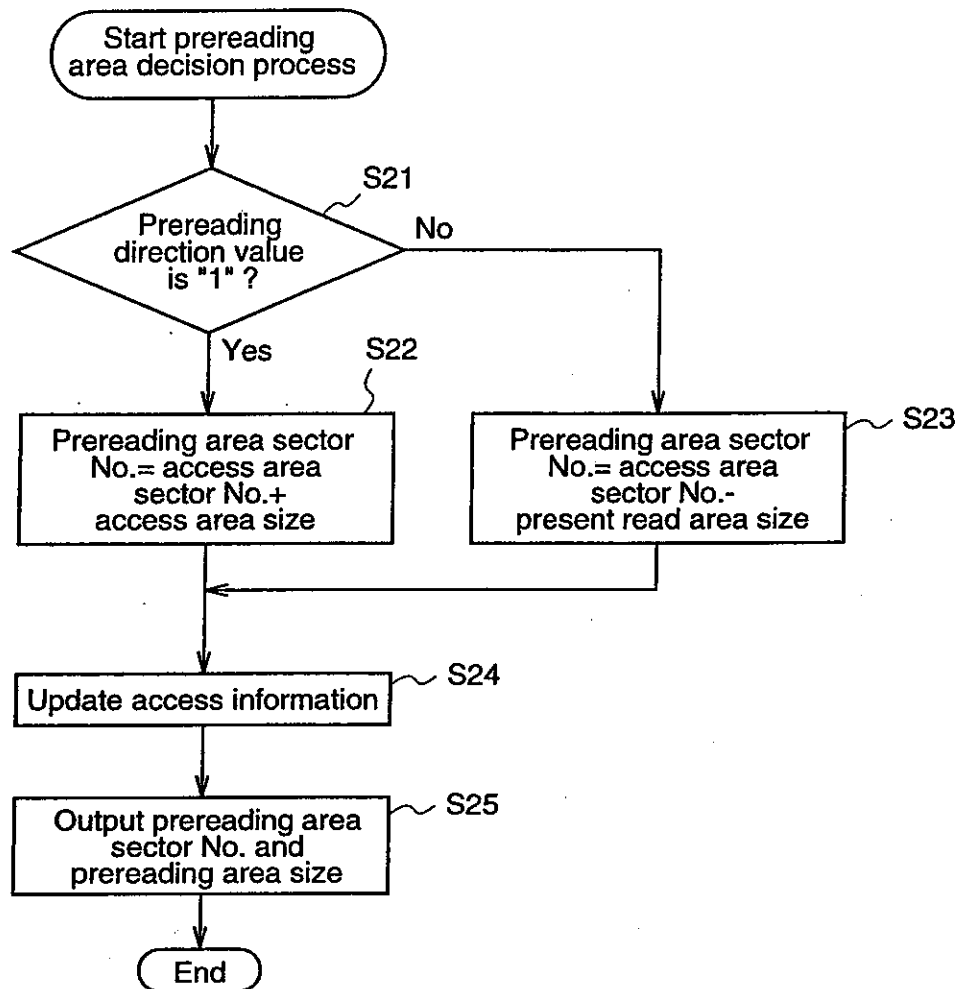
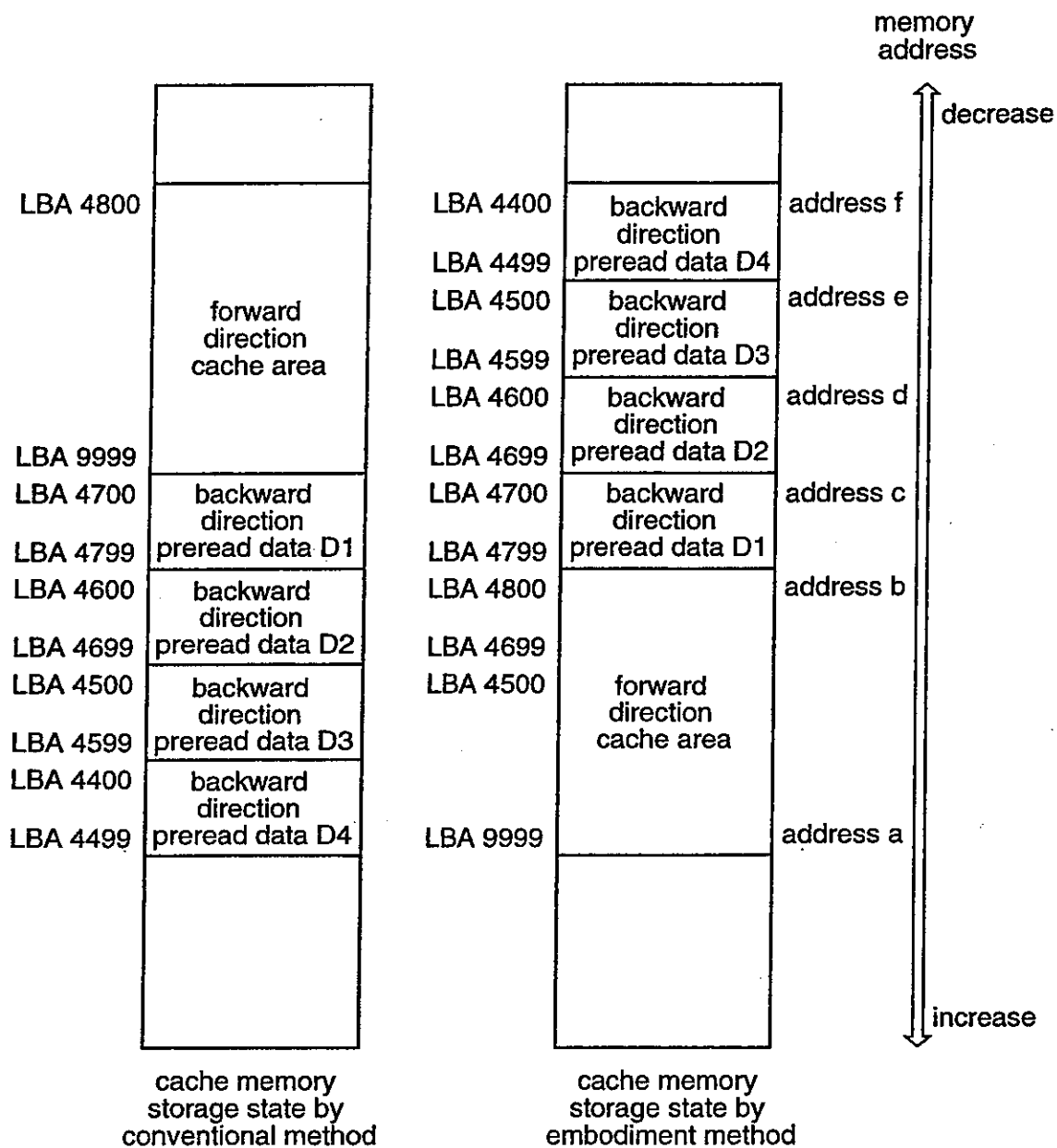


Fig.7

access area head sector No.
access area size

Q
R

Fig.8



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Fig.9

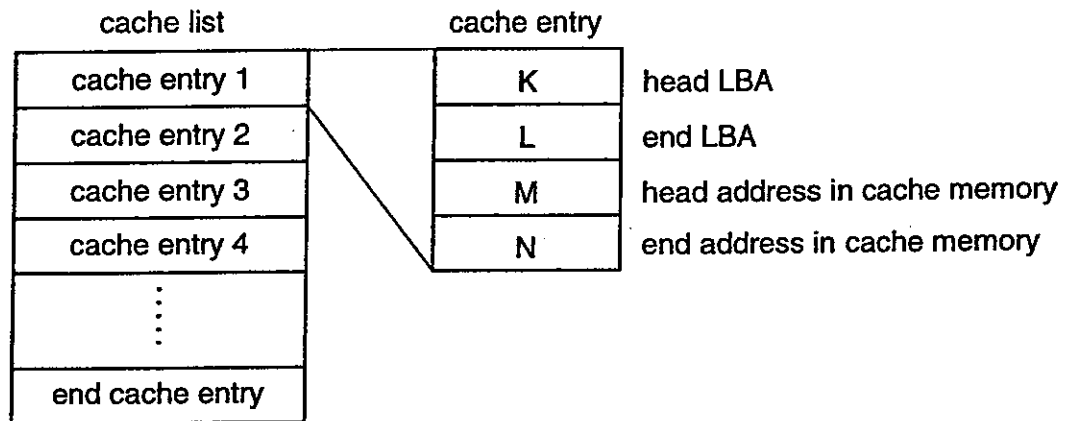
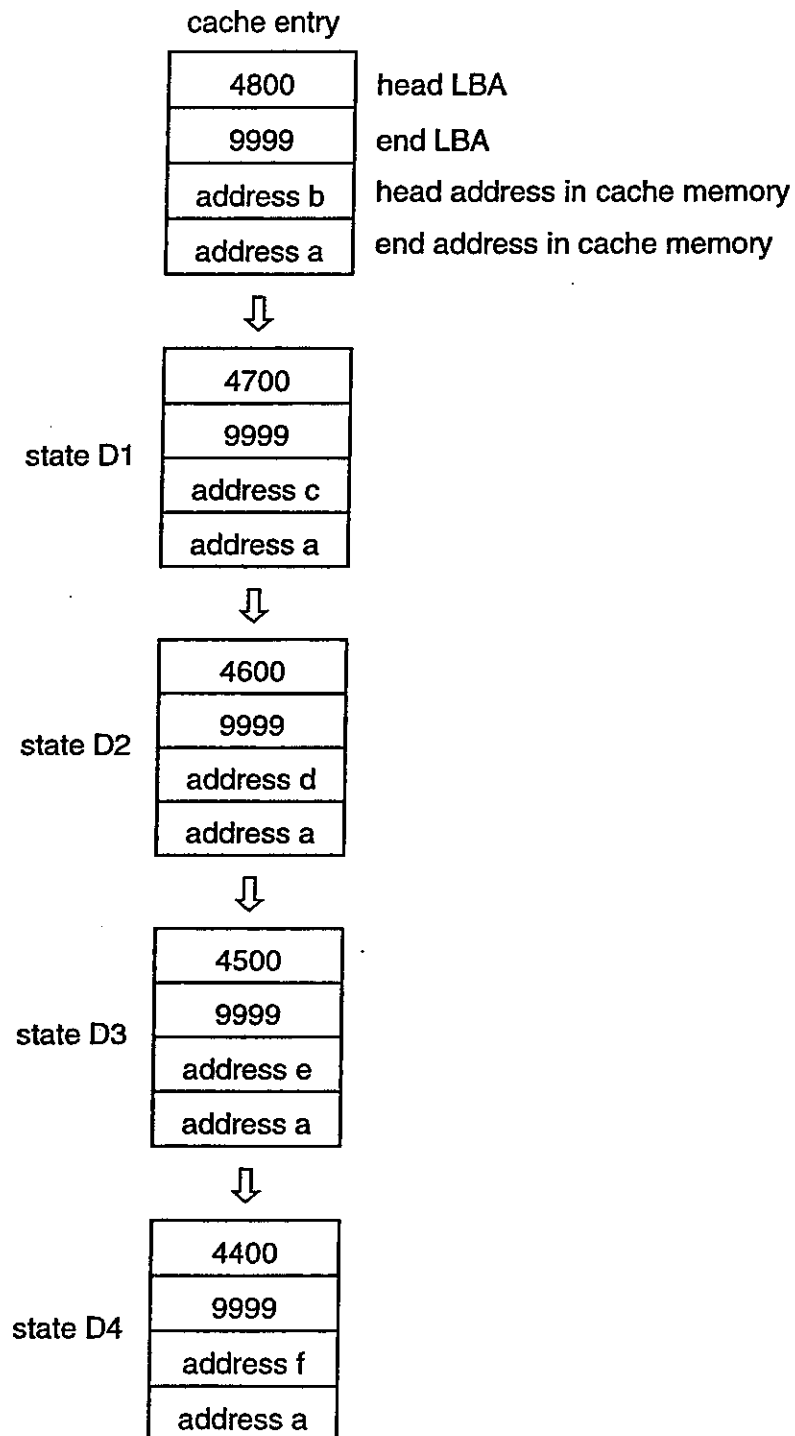


Fig.10



The diagram illustrates the architecture of a disk cache system, showing the flow of data and control signals between various components.

Host Device (1): Interacts with the Host I/F unit (2) via a **data** bus and a **command** bus.

Host I/F unit (2): Receives commands from the host device and manages data transfer between the host and the cache system.

Cache System (102 RAM and 103 CPU):

- 102 RAM:** Contains three tables:
 - cache list (12):** Stores information about cached data.
 - read command record table (5):** Records read commands.
 - access area information storage unit (13):** Stores information about the access area.
 - prereading rule table (15):** Stores rules for prereading.
- 103 CPU:** Contains several processing units:
 - cache hit judgement unit (3):** Checks if data is in the cache.
 - continuity detection unit (16):** Detects continuous access patterns.
 - prereading rule decision unit (14):** Decides on prereading rules.
 - prereading area decision unit (17):** Decides on the prereading area.
 - prereading startup unit (7):** Initiates prereading.

Data Flow:

- When a **command** is received from the host device (1), the **cache hit judgement unit (3)** checks the **cache list (12)**.
- If a hit occurs, data is transferred from the **cache memory (10)** to the **host transfer unit (11)** and then to the **host I/F unit (2)**.
- If a miss occurs, the **continuity detection unit (16)** and **prereading rule decision unit (14)** are involved in deciding on prereading.
- The **prereading area decision unit (17)** determines the area to be preread, and the **prereading startup unit (7)** initiates the process.
- Data is then transferred from the **disk transfer unit (8)** to the **cache memory (10)** and then to the **host transfer unit (11)**.

External Components:

- disk transfer unit (8):** Manages data transfer between the cache memory and the disk.
- disk (9):** The storage medium being accessed.

Fig.12

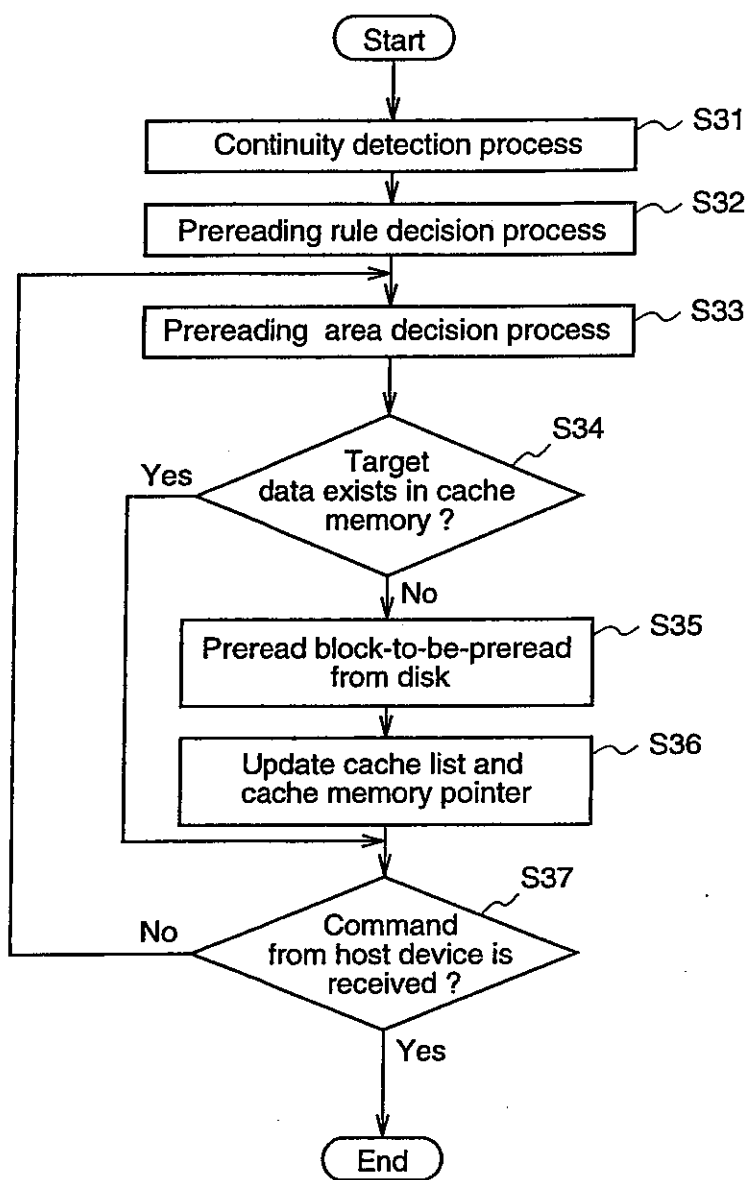


Fig.13

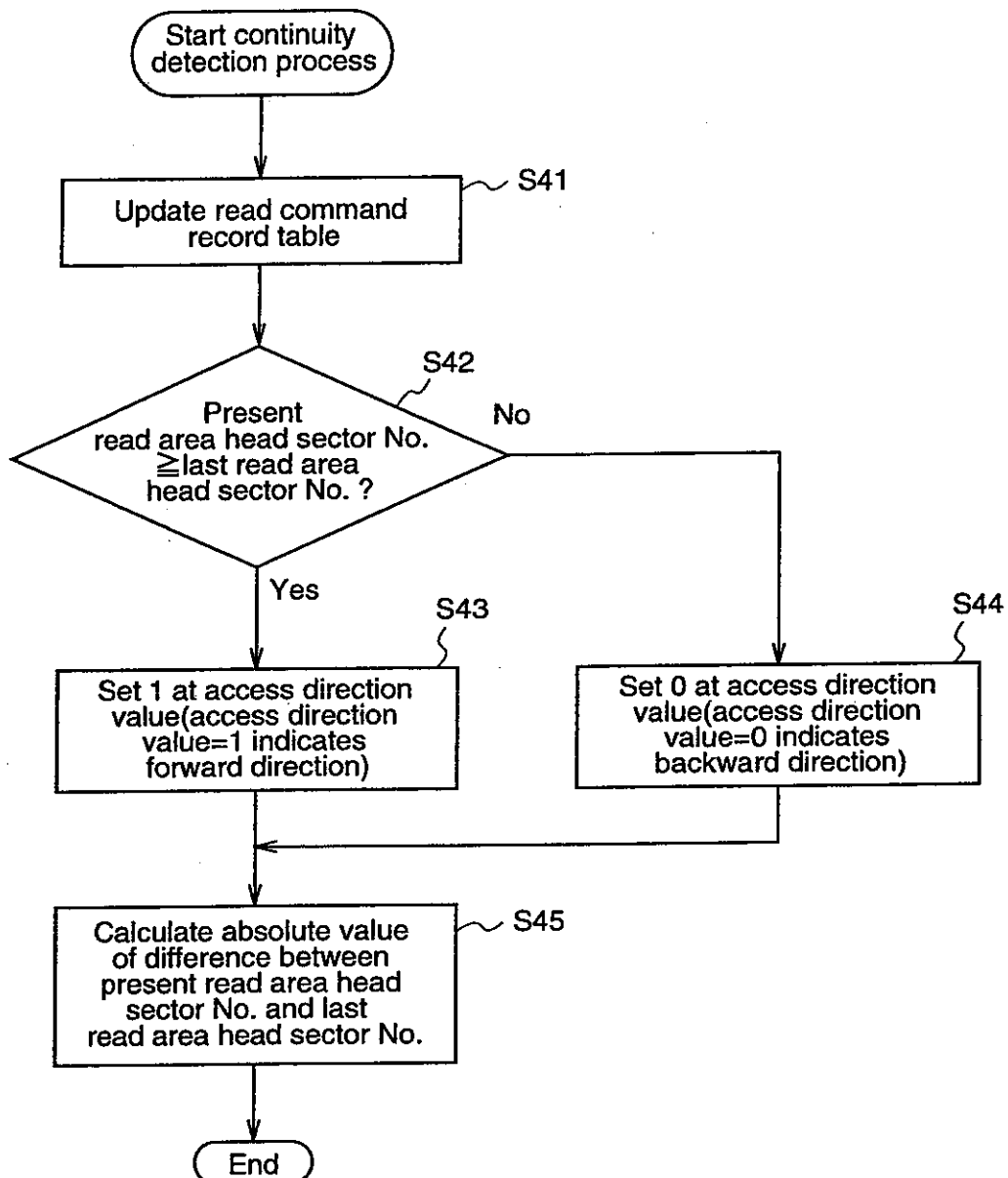


Fig.14

present read area head sector No.	G
present read area size	H
last read area head sector No.	A
last read area size	B
last-but-one read area head sector No.	C
last-but-one read area size	D
present access direction value	I
present area-to-area distance	J
last access direction value	E
last area-to-area distance	F

Fig.15

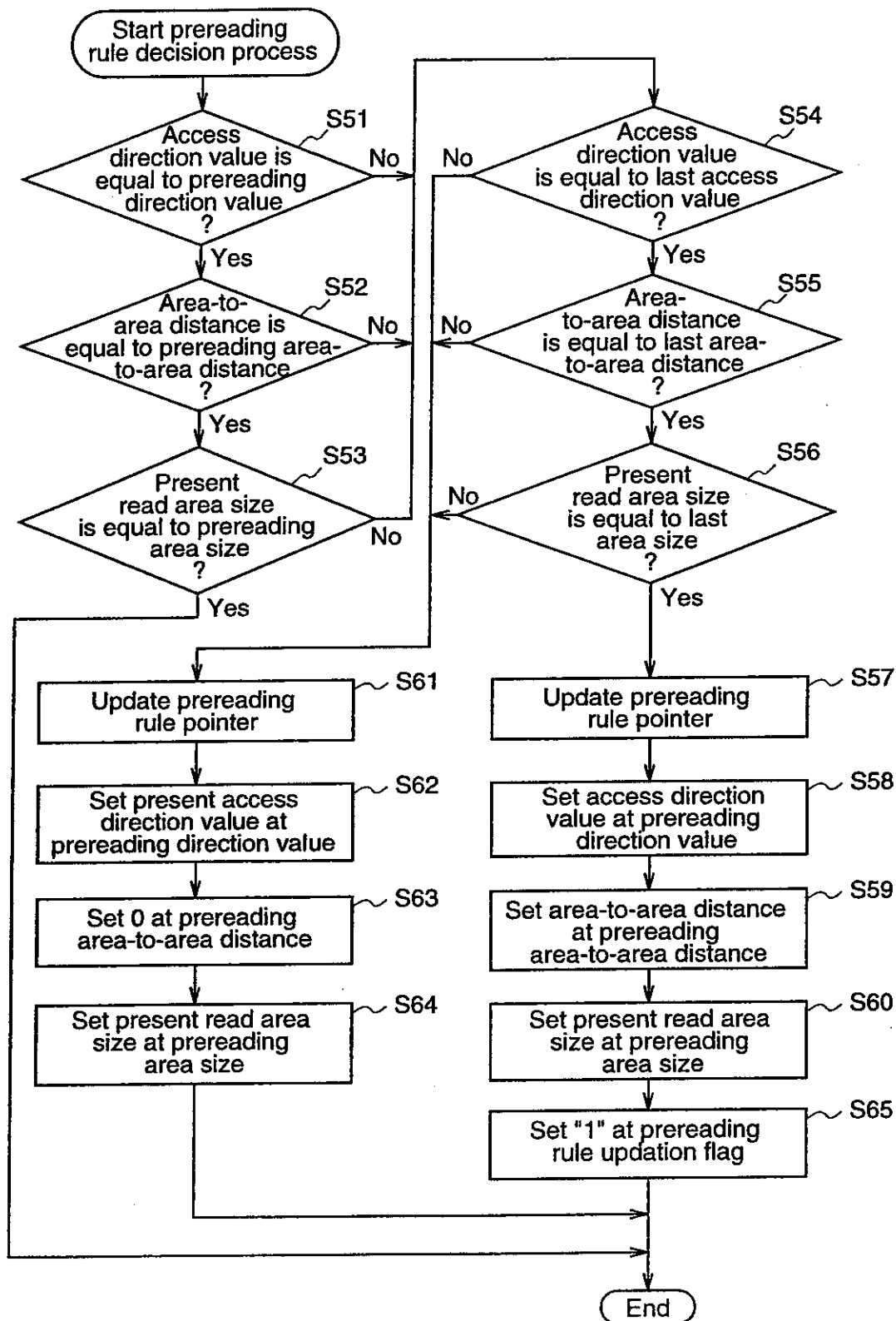


Fig.16

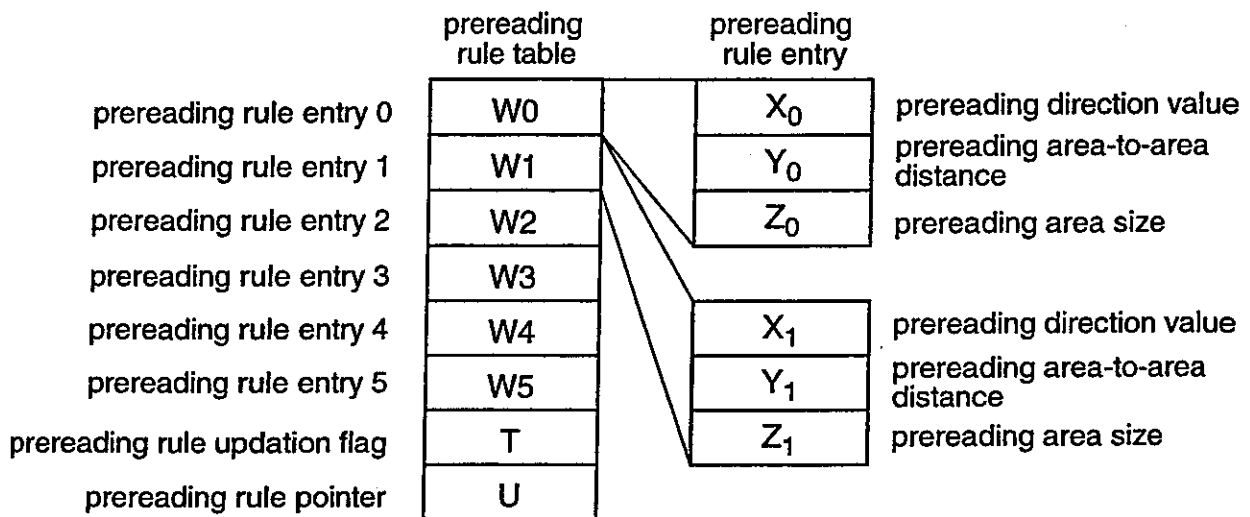


Fig.17

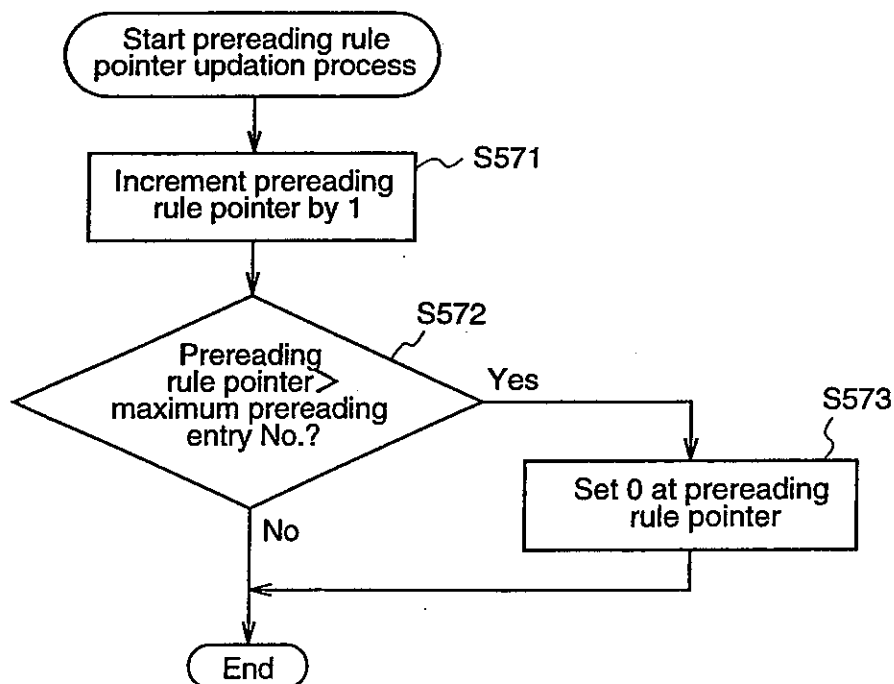


Fig.18

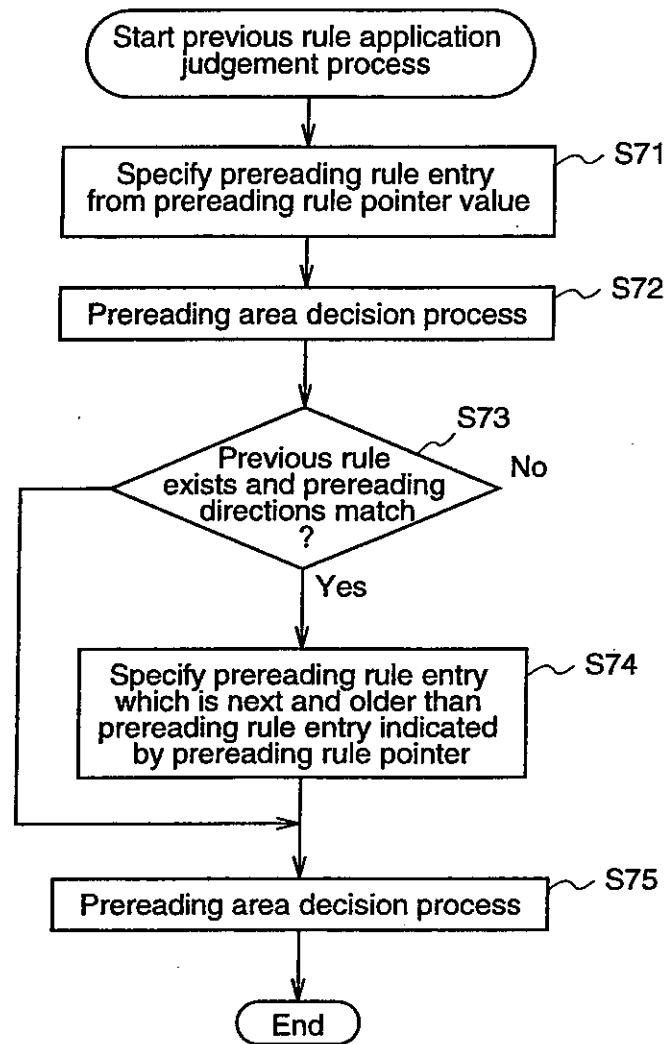
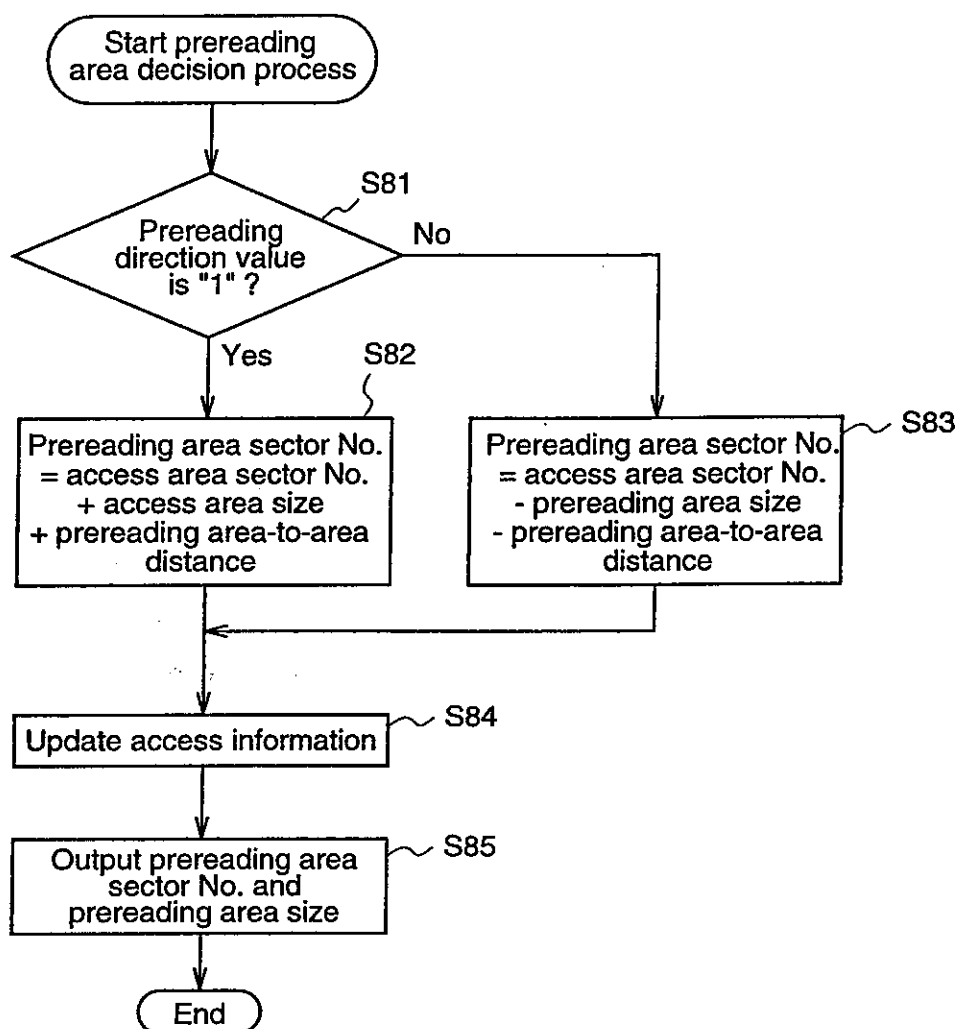


Fig.19



The diagram illustrates a cache control system architecture. At the top, a bracket indicates the system is connected to **104 RAM**. The system is divided into several functional blocks:

- Host Device (1)**: Connected to the **host I/F unit (2)** via **data** and **command** lines.
- Host I/F unit (2)**: A vertical block that interfaces with the host device and the **host transfer unit (11)**.
- Cache List (12)**: A cylinder representing a list of cache entries, connected to the **cache hit judgement unit (3)**.
- Cache Memory Pointer Storage Unit (18)**: A cylinder storing pointers to cache memory.
- Read Command Record Table (5)**: A cylinder recording read commands.
- Access Area Information Storage Unit (13)**: A cylinder storing information about access areas.
- Prereading Rule Table (15)**: A cylinder storing rules for prereading.
- Cache Hit Judgement Unit (3)**: Receives commands from the host I/F unit and checks the cache list. It sends data to the **host transfer unit (11)** and the **continuity detection unit (16)**.
- Continuity Detection Unit (16)**: Receives data from the cache hit judgement unit and sends it to the **prereading rule decision unit (14)** and the **prereading startup judgement unit (19)**.
- Prereading Rule Decision Unit (14)**: Receives data from the continuity detection unit and sends it to the **prereading area decision unit (17)**.
- Prereading Area Decision Unit (17)**: Receives data from the prereading rule decision unit and sends it to the **prereading startup judgement unit (19)**.
- Prereading Startup Judgement Unit (19)**: Receives data from the continuity detection unit and the prereading area decision unit. It sends data to the **prereading startup unit (7)**.
- Prereading Startup Unit (7)**: Receives data from the prereading startup judgement unit and sends it to the **disk transfer unit (8)**.
- Host Transfer Unit (11)**: Receives data from the host I/F unit and the cache hit judgement unit. It is connected to the **cache memory (10)**.
- Cache Memory (10)**: A block representing the main cache memory, connected to the host transfer unit and the disk transfer unit.
- Disk Transfer Unit (8)**: Receives data from the prereading startup unit and the cache memory. It is connected to the **disk (9)**.
- 105 CPU**: A bracket at the bottom indicates the central processing unit, which is connected to the cache hit judgement unit, the continuity detection unit, the prereading rule decision unit, the prereading area decision unit, the prereading startup judgement unit, the prereading startup unit, the host transfer unit, and the disk transfer unit.

Fig.21

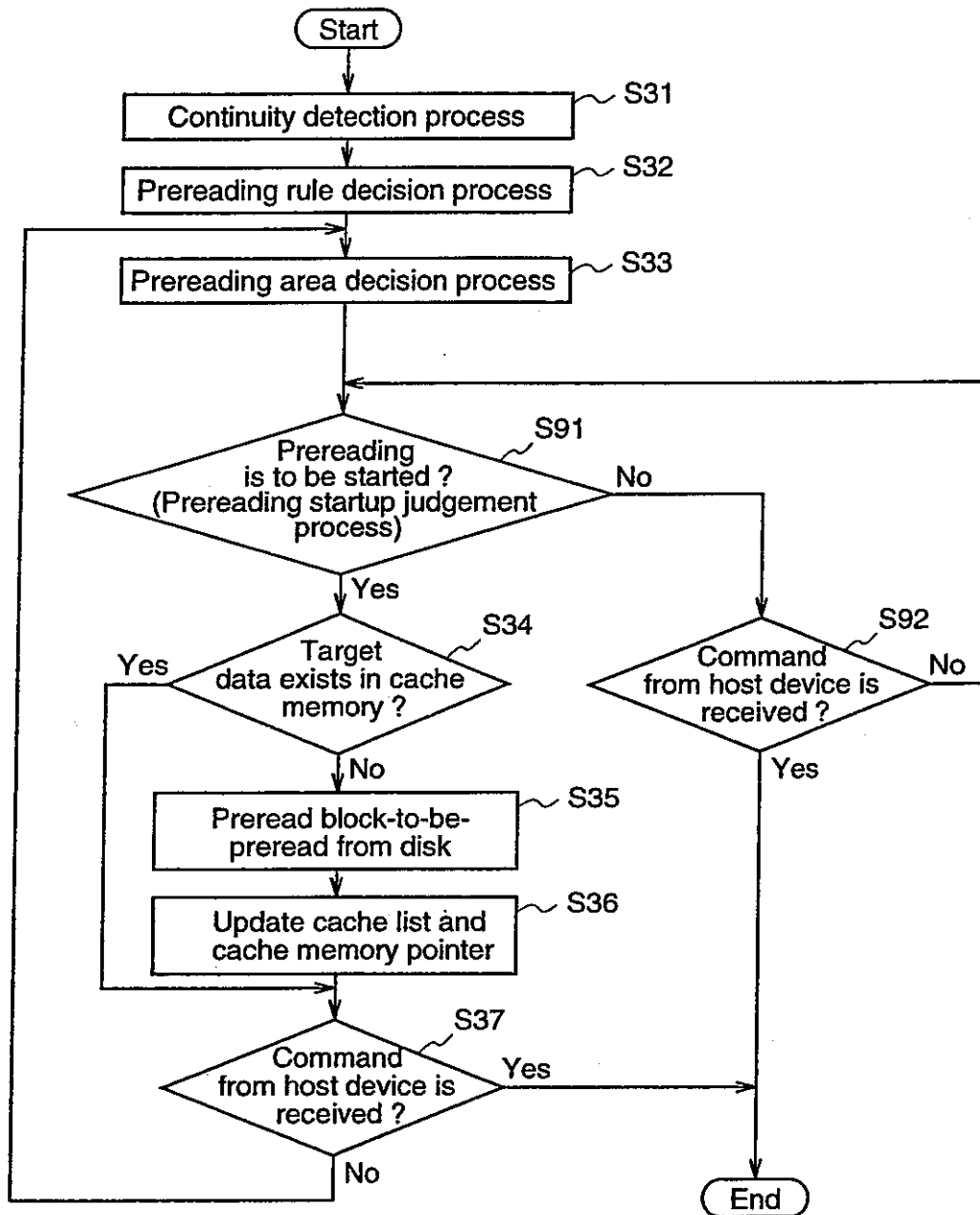
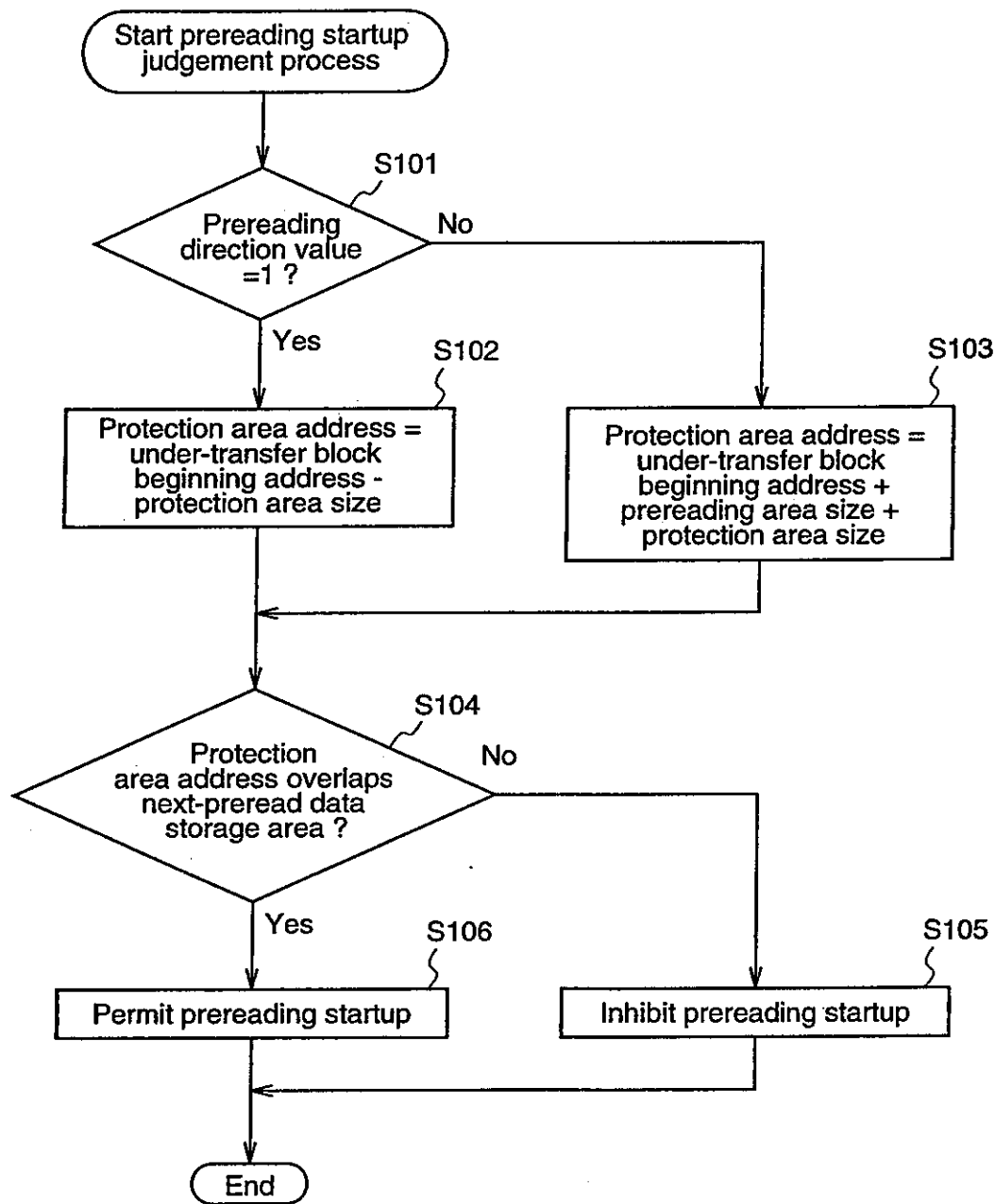


Fig.22



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Fig.23

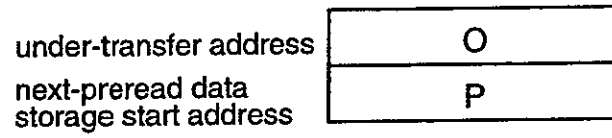


Fig.24

