

INTEGRATION OF DRY DEVELOPMENT AND ETCH PROCESSES FOR EUV PATTERNING IN A SINGLE PROCESS CHAMBER

INCORPORATION BY REFERENCE

[0001] A PCT Request Form is filed concurrently with this specification as part of the present application. Each application that the present application claims benefit of or priority to as identified in the concurrently filed PCT Request Form is incorporated by reference herein in their entireties and for all purposes.

BACKGROUND

[0002] The fabrication of semiconductor devices such as integrated circuits is a multi-step process involving photolithography. In general, the process includes deposition of a material on a wafer and patterning the material through lithographic techniques to form structural features (*e.g.*, transistors and circuitry) of the semiconductor device. The steps of a typical photolithography process include: preparing the substrate; applying a photoresist, such as by spin coating; exposing the photoresist to light in a desired pattern, causing the exposed areas of the photoresist to become more or less soluble in a developer solution; developing the photoresist pattern by applying a developer solution to remove either the exposed or the unexposed areas of the photoresist; and subsequent processing to create features on the areas of the substrate from which the photoresist has been removed, such as by etching or material deposition.

[0003] The evolution of semiconductor design has created the need and has been driven by the ability to create ever smaller features on semiconductor substrate materials. One challenge in manufacturing devices having such small features is the ability to reliably and reproducibly create photolithographic masks having sufficient resolution. Current photolithography processes typically use 193 nm ultraviolet (UV) light to expose a photoresist. The fact that the light has a wavelength significantly greater than the desired size of the features to be produced on the semiconductor substrate creates inherent issues. Achieving feature sizes smaller than the wavelength of the light requires use of complex resolution enhancement techniques such as multipatterning. Thus, there is significant interest and research towards developing photolithographic techniques using shorter wavelength light, such as extreme ultraviolet radiation (EUV), having a wavelength of from 10 nm to 15 nm, *e.g.*, 13.5 nm.

[0004] EUV photolithographic processes can present challenges however, including low power output, loss of light during patterning and metal cross-contamination stemming from metal outgassing. Accordingly, there remains a need for improved EUV photoresist processes that will produce materials having desired properties in a more efficient manner.

[0005] The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

SUMMARY

[0006] The present disclosure relates to methods and apparatuses for integration of dry development and dry development post- processes into a single process chamber. This integration increases throughput and reduces handling of wafers; augmenting the efficiency of semiconductor manufacturing by virtue of higher wafer productivity and better lithographic control. The dry development post-process of etching with a plasma may be performed in the same process chamber as dry development; eliminating the necessity for a post-dry development bake to control outgassing. In some instances, O₂ flash treatment or pattern transfer may be utilized in conjunction with dry development in a single process chamber.

[0007] Accordingly, in a first aspect, the present disclosure encompasses an apparatus for integrating dry development and etch semiconductor processes in a single process chamber. In some embodiments, the apparatus includes one or more process chambers; one or more pressure regulating devices; one or more pumps fluidly coupled with the pressure regulating device; a plasma processing system; one or more gas inlets into the process chambers and associated flow-control hardware; and a controller having at least one processor and a memory, wherein the at least one processor and the memory are communicatively connected with one another, the at least one processor is at least operatively connected with the associated flow-control hardware, and the memory stores computer-executable instructions for controlling the at least one processor to at least control the associated flow-control hardware to: perform thermal dry development at a first pressure in a process chamber; perform plasma dry development and etching at a second pressure lower than the first pressure in the same process chamber; transition pressure in the same process chamber from the first pressure to the second pressure in ten seconds or less; and maintain one or more process parameters uniformly.

[0008] In some embodiments, the one or more pressure regulating devices includes a pressure control valve assembly.

[0009] In some embodiments, the pressure control valve assembly includes a throttle valve.

[0010] In some embodiments, the one or more pumps includes a roughing pump and a turbo pump.

[0011] In some embodiments, the first pressure is from five to one fifty times higher than the second pressure.

[0012] In some embodiments, the one or more process parameters includes pumping, gas delivery or pumping and gas delivery.

[0013] In a second aspect, the present disclosure encompasses an apparatus for processing a metal-containing photoresist. In some embodiments, the apparatus includes one or more process chambers; one or more pressure regulating devices; one or more pumps fluidly coupled with the pressure regulating device; one or more gas inlets into the process chambers and associated flow-control hardware; a plasma processing system; and a controller having at least one processor and a memory, wherein the at least one processor and the memory are communicatively connected with one another, the at least one processor is at least operatively connected with the associated flow-control hardware, and the memory stores computer-executable instructions for controlling the at least one processor to at least control the associated flow-control hardware to: perform thermal dry development at a first pressure in a process chamber; perform plasma dry development and etching at a second pressure lower than the first pressure in the same process chamber; modulate pressure in the same process chamber from the first pressure to the second pressure in ten seconds or less; return pressure in the same process chamber from the second pressure back to the first pressure after plasma dry development and etching in twenty seconds or less; and maintain one or more process parameters uniformly.

[0014] In some embodiments, the plasma processing system includes a radiofrequency power amplifier.

[0015] In some embodiments, the radiofrequency power amplifier is operated continuously or pulsed.

[0016] In a third aspect, the present disclosure encompasses a method for processing a semiconductor substrate. In some embodiments, the method includes providing a patterned photoresist on a semiconductor substrate in a process chamber; thermally dry developing the patterned photoresist with a process gas at a first pressure to form a thermally dry developed patterned resist; and plasma dry developing and etching the dry developed patterned resist with an etchant at a second pressure to form a patterned substrate; wherein thermal dry developing, plasma dry developing and etching occur in the same process chamber; wherein the process chamber is transitioned before etching from the first pressure to the second pressure in ten seconds or less and returned to the first pressure after etching in twenty seconds or less; and wherein the patterned photoresist is a metal-containing photoresist.

[0017] In some embodiments, the first pressure is from about 200 to 500 mTorr and the second pressure is from about 20 to 50 mTorr.

[0018] In some embodiments, the metal-containing photoresist includes a photopatterned EUV-sensitive organo-metal oxide, a photopatterned EUV-sensitive metal oxide or an organo-metal containing thin film EUV resist.

[0019] In some embodiments, the photopatterned EUV-sensitive metal oxide includes tin oxide.

[0020] In some embodiments, tin outgassing from the tin oxide is mitigated.

[0021] In some embodiments, the method also includes selective metal deposition.

[0022] In some embodiments, the etching includes exposure to an etchant plasma.

[0023] In some embodiments, the etchant plasma includes a hardmask opening gas.

[0024] In some embodiments, the hardmask opening gas includes carbonyl sulfide, oxygen, carbon dioxide, nitrogen, hydrogen or a combination thereof.

[0025] In some embodiments, the hardmask opening gas comprises oxygen plasma.

[0026] In some embodiments, the exposure to oxygen plasma is for a duration of from about 0.5 to about 4 seconds.

[0027] These and other aspects are described further below with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] **FIG. 1** presents a flow diagram of a conventional process for depositing, development, and treating a photoresist.

[0029] **FIGS. 2A–2C** are cross-sectional schematic illustrations of various processing stages including development and treatment of photoresist.

[0030] **FIG. 3** presents a flow diagram of an example method of the overall process for treating a photoresist on a substrate after development in a single process chamber accordance with certain disclosed embodiments.

[0031] **FIG. 4** presents a flow diagram for an example method combining the steps of dry development and etching in the same process chamber in accordance with certain disclosed embodiments.

[0032] **FIG. 5** presents a flow diagram of another example method combining the steps of dry development and etching in the same process chamber and including selective metal deposition in accordance with certain disclosed embodiments.

[0033] **FIG. 6** depicts a schematic illustration of an example process station for maintaining an environment that is suitable for performing photoresist development, photoresist treatment, and/or etch operations in accordance with certain disclosed embodiments.

[0034] FIG. 7 depicts a schematic illustration of an example multi-station processing tool suitable for implementation of photoresist development, photoresist treatment, and/or etch operations described herein in accordance with certain disclosed embodiments.

[0035] FIG. 8 shows a cross-sectional schematic view of an example inductively-coupled plasma apparatus for implementing certain embodiments and operations described herein in accordance with certain disclosed embodiments.

[0036] FIG. 9 depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules that interface with a vacuum transfer module, suitable for implementations of processes described herein in accordance with certain disclosed embodiments.

DETAILED DESCRIPTION

[0037] In the following description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments will be described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

DEFINITIONS

[0038] As used herein, the term “about” is understood to account for minor increases and/or decreases beyond a recited value, which changes do not significantly impact the desired function of the parameter beyond the recited value(s). In some cases, “about” encompasses +/-10% of any recited value. As used herein, this term modifies any recited value, range of values, or endpoints of one or more ranges.

[0039] As used herein, the terms “top,” “bottom,” “upper,” “lower,” “above,” and “below” are used to provide a relative relationship between structures. The use of these terms does not indicate or require that a particular structure must be located at a particular location in the apparatus.

[0040] The implementations disclosed below describe deposition of a material on a substrate such as a wafer, substrate, or other work piece. The work piece may be of various shapes, sizes, and materials. In this application, the terms “semiconductor wafer,” “wafer,” “substrate,” “wafer substrate,” and “partially fabricated integrated circuit” are used interchangeably. One of ordinary skill in the art would understand that the term “partially fabricated integrated circuit” can refer to a silicon wafer during any of many stages of integrated circuit fabrication thereon. A wafer or substrate used in the semiconductor device industry typically has a diameter of 200 mm, or 300 mm, or 450 mm. Unless otherwise stated, the processing details recited herein (e.g., flow rates,

power levels, etc.) are relevant for processing 300 mm diameter substrates, or for treating chambers that are configured to process 300 mm diameter substrates and can be scaled as appropriate for substrates or chambers of other sizes. In addition to semiconductor wafers, other work pieces that may be used implementations disclosed herein include various articles such as printed circuit boards and the like. The processes and apparatuses can be used in the fabrication of semiconductor devices, displays, LEDs, photovoltaic panels and the like.

[0041] As used herein, the phrase “at least one of A, B, and C” should be construed to mean a logical (A or B or C), using a non-exclusive logical “or”, and should not be construed to mean “at least one of A, at least one of B and at least one of C”.

[0042] As used herein, the term “photoresist” and derivatives thereof refer to a light-sensitive material used in processes such as photolithography, photoetching or photoengraving to form a patterned coating on a surface. Photoresist materials change solubility with respect to a developer solution when exposed to certain wavelengths of light. Photoresist layers may be composed of positive (exposed region becomes soluble) or negative (exposed region becomes insoluble) photoresist material.

INTRODUCTION AND CONTEXT

[0043] This disclosure relates generally to the field of semiconductor processing. In particular, this disclosure is directed to post-development treatment of photoresists including metal-containing photoresists. Such metal and/or metal oxide-containing photoresists may undergo treatment to change the chemical, physical, and/or optical properties of the photoresist after development and prior to pattern transfer. The photoresist treatment enhances the performance of the photoresist. For instance, the photoresist treatment can reduce dose-to-size (DtS), reduce LWR, increase line CD, improve etch resistance, reduce outgassing of tin or other elements, and/or reduce defects/line breaks.

[0044] Patterning of thin films in semiconductor processing is often an important step in the fabrication of semiconductors. Patterning involves lithography. In conventional photolithography, such as 193 nm photolithography, patterns are printed onto a photosensitive photoresist film by exposing the photoresist to photons in selective areas defined by a photomask, thereby causing a chemical reaction in the exposed photoresist and creating a chemical contrast that can be leveraged in the development step to remove certain portions of the photoresist to form the pattern. The patterned and developed photoresist film then can be used as an etch mask to transfer the pattern into underlying films that are composed of metal, oxide, etc.

[0045] Advanced technology nodes (as defined by the International Technology Roadmap for

Semiconductors) include nodes 22 nm, 16 nm, and beyond. In the 16 nm node, for example, the width of a via or line in a Damascene structure is typically no greater than about 30 nm. Scaling of features on advanced semiconductor integrated circuits (ICs) and other devices is driving lithography to improve resolution.

[0046] Extreme ultraviolet (EUV) lithography can extend lithography technology by moving to smaller imaging source wavelengths than would be achievable with conventional photolithography methods. EUV light sources at approximately 10–20 nm, or 11–14 nm wavelength, for example 13.5 nm wavelength, can be used for leading-edge lithography tools, also referred to as scanners. The EUV radiation is strongly absorbed in a wide range of solid and fluid materials including quartz and water vapor, and so operates in a vacuum.

[0047] EUV lithography makes use of EUV resists that are patterned to form masks for use in etching underlying layers. EUV resists may be polymer-based chemically amplified resists (CARs) produced by liquid-based spin-on techniques. An alternative to CARs is directly photopatternable metal oxide-containing films, such as those available from Inpria Corp. (Corvallis, OR), and described, for example, in U.S. Pat. Nos. US 2017/0102612, US 2016/0216606, and US 2016/0116839, incorporated by reference herein at least for their disclosure of photopatternable metal oxide-containing films. Such films may be produced by spin-on techniques or dry vapor-deposited. The metal oxide-containing film can be patterned directly (i.e., without the use of a separate photoresist) by EUV exposure in a vacuum ambient providing sub-30 nm patterning resolution, for example as described in U.S. Pat. No. 9,996,004, issued June 12, 2018 and titled EUV PHOTOPATTERNING OF VAPOR-DEPOSITED METAL OXIDE-CONTAINING HARDMASKS, and/or in International Appl. No. PCT/US19/31618, published as International Pub. No. WO 2019/217749, filed May 9, 2019, and titled METHODS FOR MAKING EUV PATTERNABLE HARD MASKS, the disclosures of which at least relating to the composition, deposition, and patterning of directly photo-patternable metal oxide films to form EUV resist masks is incorporated by reference herein. Generally, the patterning involves exposure of the EUV resist with EUV radiation to form a photo pattern in the resist, followed by development to remove a portion of the resist according to the photo pattern to form the mask.

[0048] Directly photo-patternable EUV or DUV resists may be composed of or contain metals and/or metal oxides mixed within organic components. The metals/metal oxides can enhance the EUV or DUV photon adsorption, generate secondary electrons, and/or show increased etch selectivity to an underlying film stack and device layers. These resists can be developed using a wet (solvent) approach, which requires the wafer to move to the track, where it is exposed to

developing solvent, dried, and then baked. Such resists may also be developed using a dry approach or a combination of wet and dry approaches, as described herein.

[0049] Generally, resists can be employed as a positive tone resist or a negative tone resist by controlling the chemistry of the resist and/or the solubility or reactivity of the developer. It would be beneficial to have a EUV or DUV resist that can serve as either a negative tone resist or a positive tone resist.

[0050] While the following may describe techniques as relating to EUV processes, such techniques may also be applicable to other next generation lithographic techniques. Various radiation sources may be employed, including EUV (generally about 13.5 nm), DUV (deep-UV, generally in the 248 nm or 193 nm range with excimer laser sources), X-ray (including EUV at the lower energy range of the X-ray range), and e-beam (including a wide energy range).

[0051] The present disclosure relates to post-development treatment of photoresist. A metal or metal oxide-containing photoresist may be wet or dry deposited. The metal or metal oxide-containing photoresist may have high absorption of EUV radiation so that the photoresist may be patterned by EUV exposure to form exposed and unexposed regions. After development selectively removes exposed or unexposed regions of the photopatterned metal or metal oxide-containing photoresist, the post-developed photoresist may be treated. Such treatment may include one or more of the following operations: (i) thermal annealing, (ii) plasma exposure, (iii) reactive gas exposure, and (iv) selective deposition of protective layer. Such treatment may achieve one or more of the following advantages: reduced defectivity, reduced LWR, reduced DtS, reduced outgassing (e.g., tin outgassing), increased etch resistance, and increased line CD, thereby improving performance of the metal or metal oxide-containing photoresist during etch.

[0052] Reference is made herein in detail to specific embodiments of the disclosure. Examples of the specific embodiments are illustrated in the accompanying drawings. While the disclosure will be described in conjunction with these specific embodiments, it will be understood that it is not intended to limit the disclosure to such specific embodiments. On the contrary, it is intended to cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the disclosure. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. The present disclosure may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail so as to not unnecessarily obscure the present disclosure.

[0053] FIG. 1 presents a flow diagram of the steps of a conventional method for depositing,

development, and treating a photoresist. At block 102 of the process 100, a layer of photoresist is deposited. This may be either a dry deposition process such as a vapor deposition process or a wet deposition process such as a spin-on deposition process. In one embodiment, a metal-containing precursor is deposited as a solution by using a liquid-based spin-on technique. In another embodiment, a metal-containing precursor is deposited in vapor form by using a dry technique (e.g., chemical vapor deposition).

[0054] A photoresist film can be deposited on a substrate. Such a film can be deposited by using wet or dry deposition processes, in which a metal-containing precursor (e.g., a tin-containing precursor, such as any described herein) is provided in proximity to a substrate. In one embodiment, the metal-containing precursor is deposited as a solution by using a liquid-based spin-on technique. In another embodiment, the metal-containing precursor is deposited in vapor form by using a dry technique (e.g., chemical vapor deposition). While the present disclosure often shows the metal-containing precursor being a tin-containing precursor, other metal atoms can be employed.

[0055] The layers and films described herein may include an element (e.g., a metal atom or a non-metal atom) having a high photoabsorption cross-section, such as equal to or greater than $1 \times 10^7 \text{ cm}^2/\text{mol}$. Such elements can be provided by depositing one or more precursor(s) to provide the imaging layer.

[0056] In some embodiments, the film is a radiation-sensitive film (e.g., an EUV-sensitive film). This film, in turn, can serve as an EUV resist, as further described herein. In particular embodiments, the layer or film can include one or more ligands (e.g., EUV labile ligands) that can be removed, cleaved, or cross-linked by radiation (e.g., EUV or DUV radiation).

[0057] The precursor can provide a patternable film that is sensitive to radiation (or a patterning radiation-sensitive film or a photopatternable film). Such radiation can include EUV radiation, DUV radiation, or UV radiation that is provided by irradiating through a patterned mask, thereby being a patterned radiation. The film itself can be altered by being exposed to such radiation, such that the film is radiation-sensitive or photosensitive. In particular embodiments, the precursor is an organometallic compound, which includes at least one metal center.

[0058] The precursor can have any useful number and type of ligand(s). In some embodiments, the ligand can be characterized by its ability to react in the presence of a counter-reactant, or in the presence of patterned radiation. For instance, the precursor can include a ligand that reacts with a counter-reactant, which can introduce linkages between metal centers (e.g., an -O- linkage). In another instance, the precursor can include a ligand that eliminates in the presence of patterned

radiation.

[0059] The precursor may include a metal or a metalloid or an atom with a high patterning radiation-absorption cross-section (e.g., an EUV absorption cross-section that is equal to or greater than 1×10^7 cm²/mol). In some embodiments, M is tin (Sn), bismuth (Bi), tellurium (Te), cesium (Cs), antimony (Sb), indium (In), molybdenum (Mo), hafnium (Hf), iodine (I), zirconium (Zr), iron (Fe), cobalt (Co), nickel (Ni), copper (Cu), zinc (Zn), silver (Ag), platinum (Pt), and lead (Pb).

[0060] In particular embodiments, the precursor includes tin. Non-limiting tin precursors include SnF₂, SnH₄, SnBr₄, SnCl₄, SnI₄, tetramethyl tin (SnMe₄), tetraethyl tin (SnEt₄), trimethyl tin chloride (SnMe₃Cl), dimethyl tin dichloride (SnMe₂Cl₂), methyl tin trichloride (SnMeCl₃), tetraallyltin, tetravinyl tin, hexaphenyl ditin (IV) (Ph₃Sn-SnPh₃, in which Ph is phenyl), dibutyldiphenyltin (SnBu₂Ph₂), trimethyl(phenyl) tin (SnMe₃Ph), trimethyl(phenylethynyl) tin, tricyclohexyl tin hydride, tributyl tin hydride (SnBu₃H), dibutyltin diacetate (SnBu₂(CH₃COO)₂), tin(II) acetylacetonate (Sn(acac)₂), tributyltin ethoxide (SnBu₃(OEt)), dibutyltin dimethoxide (SnBu₂(OMe)₂), tributyltin methoxide (SnBu₃(OMe)), tin(IV) tert-butoxide (Sn(*t*-BuO)₄), *n*-butyltin tributoxide (Sn(*n*-Bu)(*t*-BuO)₃), tetrakis(dimethylamino)tin (Sn(NMe₂)₄), tetrakis(ethylmethylamino)tin (Sn(NMeEt)₄), tetrakis(diethylamino)tin(IV) (Sn(NEt₂)₄), (dimethylamino)trimethyl tin(IV) (Sn(Me)₃(NMe₂), Sn(*i*-Pr)(NMe₂)₃, Sn(*n*-Bu)(NMe₂)₃, Sn(*s*-Bu)(NMe₂)₃, Sn(*i*-Bu)(NMe₂)₃, Sn(*t*-Bu)(NMe₂)₃, Sn(*t*-Bu)₂(NMe₂)₂, Sn(*t*-Bu)(NEt₂)₃, Sn(tbba), Sn(II) (1,3-bis(1,1-dimethylethyl)-4,5-dimethyl-(4*R*,5*R*)-1,3,2-diazastannolidin-2-ylidene), or bis[bis(trimethylsilyl)amino] tin (Sn[N(SiMe₃)₂]₂).

[0061] Exemplary deposition techniques (e.g., for a film) include any described herein, such as ALD (e.g., thermal ALD and plasma-enhanced ALD), spin-coat deposition, PVD including PVD co-sputtering, CVD (e.g., PE-CVD or LP-CVD), sputter deposition, e-beam deposition including e-beam co-evaporation, etc., or a combination thereof, such as ALD with a CVD component, such as a discontinuous, ALD-like process in which precursors and counter-reactants are separated in either time or space.

[0062] Further description of precursors and methods for their deposition as EUV photoresist films applicable to this disclosure may be found in International Application No. PCT/US19/31618, published as International Publication No. WO 2019/217749, filed May 9, 2019, and titled METHODS FOR MAKING EUV PATTERNABLE HARD MASKS. The thin films may include optional materials in addition to a precursor and a counter-reactant to modify the chemical or physical properties of the film, such as to modify the sensitivity of the film to EUV or enhancing etch resistance. Such optional materials may be introduced, such as by doping during

vapor phase formation prior to deposition on the substrate, during deposition on the substrate, and/or after deposition of the film. In some embodiments, a gentle remote H₂ plasma may be introduced so as to replace some Sn-L bonds with Sn-H, for example, which can increase reactivity of the resist under EUV. In other embodiments, CO₂ may be introduced to replace some Sn-O bonds with Sn-CO₃ bonds, which can be more resistant to wet development.

[0063] Various atoms present in the precursor and/or counter-reactant can be provided within a capping layer, which in turn is disposed on any useful layer or structure. The capping layer can be any useful thickness (e.g., any thickness described herein, including from about 0.1 nm to about 5 nm).

[0064] Furthermore, two or more different precursors can be employed within each layer (e.g., a film or a capping layer). For instance, two or more of any metal-containing precursors herein can be employed to form an alloy. Yet other exemplary EUV-sensitive materials, as well as processing methods and apparatuses, are described in U.S. Patent No. 9,996,004; International Patent Publication No. WO 2020/102085; and International Patent Publication No. WO 2019/217749, each of which is incorporated herein by reference in its entirety.

[0065] At block 104 of the process 100, the backside surface or bevel of the substrate can be optionally cleaned, and/or an edge bead of the photoresist that was deposited in the prior step can be removed. Such cleaning or removing steps can be useful for removing particles that may be present after depositing a photoresist layer. The removing step can include processing the wafer with a wet metal oxide (MeOx) edge bead removal (EBR) step.

[0066] At block 106 of the process 100, a post-application bake (PAB) or a post-application treatment can be optionally performed. Such treatment can improve etch resistance of unexposed material to aqueous or non-aqueous solution. In one instance, such treatment can enhance the chemical composition difference (or contrast) between unexposed and exposed regions, thus the PAB operation is conducted. In another instance, such treatment can reduce the chemical composition difference (or contrast) between unexposed and exposed regions, thus the PAB operation is not conducted. In yet another instance, use of PAB removes residual moisture from the layer to form a hardened resist film. The PAB can involve some combination of thermal treatment, chemical exposure, and/or moisture to increase the EUV sensitivity of the film, thereby reducing the EUV dose to develop a pattern in the film. In particular embodiments, the PAB step is conducted at a temperature greater than about 100°C or at a temperature of from about 100°C to about 200°C or from about 100°C to about 250°C. In other embodiments, the PAB step is conducted at a temperature from about 190°C to about 350°C in the absence of an O-containing

gas. In another instance, post-application treatment includes exposing the film to an inert gas or CO₂, which can optionally include cooling or heating. Use of an inert gas can provide metal-oxygen-metal species, and use of CO₂ can provide metal carbonate species within the film.

[0067] At block 108 of the process 100, the film is exposed to EUV radiation to develop a pattern. Generally, the EUV exposure causes a change in the chemical composition of the film, creating a contrast in etch selectivity that can be used to remove a portion of the film. Such a contrast can provide a positive tone resist. However, it will be understood that the EUV exposure can alternatively cause a contrast such that unexposed regions are selectively removed. Such a contrast can provide a negative tone resist, as described herein. EUV exposure can include, e.g., an exposure having a wavelength in the range of about 10 nm to about 20 nm in a vacuum ambient (e.g., about 13.5 nm in a vacuum ambient).

[0068] At block 110 of the process 100, a post-exposure bake (PEB) is performed on the exposed film, thereby further removing residual moisture, promoting chemical condensation within the film, or increasing contrast in etch selectivity of the exposed film; or post-treating the film in any useful manner. In one instance, such treatment can reduce the chemical composition difference (or contrast) between unexposed and exposed regions, thus the PEB operation is not conducted. In another instance, the exposed film can be thermally treated (e.g., at a low temperature and/or optionally in the presence of various chemical species) to promote reactivity within the EUV exposed or unexposed portions of the resist upon exposure to a stripping agent or a positive tone developer (e.g., a halide-based aqueous acid, such as HCl, HBr, HI, or combinations thereof). In another instance, the exposed film can be thermally treated (e.g., at a low temperature) to further cross-link ligands within the EUV unexposed portions of the resist, thereby providing EUV exposed portions that can be selectively removed upon exposure to a stripping agent (e.g., a positive tone developer). In yet another instance, PEB is omitted.

[0069] At block 112 of the process 100, the photoresist pattern is developed by way of positive tone development or negative tone development. In various embodiments of development, the unexposed regions are selectively removed (to provide a pattern within a negative tone resist). These steps may be wet processes using one or more developers or developing solutions, followed by an optional rinse operation (e.g., with deionized water or another solvent) or an optional dry operation (e.g., with air or under inert conditions with optional heat). In particular embodiments, the development step is a wet process applied to a tin-based film. In other embodiments, the development step is a dry process applied to a tin-based film. For example, the dry process includes a halide-containing chemistry.

[0070] After block 112, an after development inspection may be performed. If needed, rework is performed by returning to repeat operation 102.

[0071] At block 114 of the process 100, the photoresist undergoes treatment prior to pattern transfer. The treatment may be a thermal treatment, plasma treatment, chemical treatment, selective deposition treatment, or a combination of the aforementioned treatments. Thermal treatment may expose the photoresist to an elevated temperature between about 200°C and about 300°C to reduce defectivity and LWR. Plasma treatment may expose the photoresist to plasma such as a direct (*in-situ*) plasma or remote plasma in order to densify the photoresist and reduce LWR. Chemical treatment may expose the photoresist to reactive chemical species such as halide-based species (e.g., tungsten hexafluoride) or carbon-containing precursor (e.g., carbon monoxide, metal organic precursors) to improve etch resistance, reduce outgassing, and increase line CD. Selective deposition treatment may expose the photoresist to chemical precursors for selectively depositing a protective coating on the photoresist to reduce DtS, improve etch resistance, reduce outgassing, and increase line CD. Any one or more of the foregoing treatments are applied to the photoresist after development to improve the performance of the photoresist during pattern transfer.

[0072] At block 116 of the process 100, one or more substrate layers are etched using the photoresist mask for pattern transfer. Such substrate layers are underlying the photoresist mask and may be removable by lithographic etching. Pattern transfer etching may etch material to a desired depth to form a plurality of patterned features. In some embodiments, the one or more substrate layers may include amorphous carbon (a-C), amorphous silicon (a-Si), tin oxide (e.g., SnO_x), silicon oxide (e.g., SiO₂), silicon oxynitride (e.g., SiO_xN_y), silicon oxycarbide (e.g., SiO_xC_y), silicon nitride (e.g., Si₃N₄), titanium oxide (e.g., TiO₂), titanium nitride (e.g., TiN), tungsten (e.g., W), doped carbon (e.g., W-doped C), tungsten oxide (e.g., WO_x), hafnium oxide (e.g., HfO₂), zirconium oxide (e.g., ZrO₂), and aluminum oxide (e.g., Al₂O₃). Any defects or variations in CD in the photoresist mask are replicated in the material being patterned during pattern transfer etching. Additionally, poor etch resistance adversely impacts transfer of patterns to underlying substrate layers over the course of etching. Post-development treatment of the photoresist mask mitigates the foregoing issues to ensure successful pattern transfer during pattern transfer etching.

[0073] After pattern transfer, an after etch inspection may be performed. If needed, rework is performed by returning to repeat operation 102.

[0074] FIGS. 2A–2C show cross-sectional schematic illustrations providing an overview of the

various processing stages including development and treatment of photoresist. As shown in **FIG. 2A**, a wafer 200 includes a substrate 202 and a substrate layer 204 to be etched. The patterning structure can include any useful substrate. For instance, an incoming wafer can be prepared with a substrate surface of a desired material, with the uppermost material being the layer into which the resist pattern is transferred. While the material selection may vary depending on integration, it is generally desired to select a material which can be etched with high selectivity to (i.e., much faster than) the EUV resist or imaging layer.

[0075] In some embodiments, the substrate is a hardmask, which is used in lithographic etching of an underlying semiconductor material. The hardmask may comprise any of a variety of materials, including amorphous carbon (a-C), tin oxide (e.g., SnO_x), silicon oxide (e.g., SiO_x , including SiO_2), silicon oxynitride (e.g., SiO_xN_y), silicon oxycarbide (e.g., SiO_xC_y), silicon nitride (e.g., Si_3N_4), titanium oxide (e.g., TiO_2), titanium nitride (e.g., TiN), tungsten (e.g., W), doped carbon (e.g., W -doped C), tungsten oxide (e.g., WO_x), hafnium oxide (e.g., HfO_2), zirconium oxide (e.g., ZrO_2), and aluminum oxide (e.g., Al_2O_3). Suitable substrate materials can include various carbon-based films (e.g., ashable hardmask (AHM), silicon-based films (e.g., SiO_x , SiC_x , SiO_xC_y , SiO_xN_y , $\text{SiO}_x\text{C}_y\text{N}_z$), a-Si:H, poly-Si, or SiN), or any other (generally sacrificial) film applied to facilitate the patterning process). For example, the substrate may preferably comprise SnO_x , such as SnO_2 . In various embodiments, the layer may be from 1 nm to 100 nm thick, or from 2 nm to 10 nm thick.

[0076] In some embodiments, the substrate layer 204 includes an ashable hard mask such as amorphous carbon, spin-on carbon, or other material, e.g., silicon, silicon oxide, silicon nitride, silicon carbide, etc. In some embodiments, the substrate layer 204 may be a layer stack disposed on the substrate 202. The wafer 200 further includes a photopatterned metal-containing EUV resist film 206. For example, the photopatterned metal-containing EUV resist film 206 may be an organometal-containing layer disposed on the substrate layer 204 to be etched. The photopatterned metal-containing EUV resist film 206 may have a thickness between about 5 nm and about 50 nm or between about 10 nm and about 30 nm. The photopatterned metal-containing EUV resist film 206 may be provided in a process chamber after photopatterning in an EUV scanner and/or after a PEB treatment. The photopatterned metal-containing EUV resist film 306 includes non-EUV exposed regions 206a and EUV exposed regions 206b.

[0077] As shown in **FIG. 2B**, the non-EUV exposed regions 206a of the photopatterned metal-containing EUV resist film 206 is removed in a development process. The development may use a wet development chemistry or dry development chemistry. Where dry development chemistry

is applied, the dry development may proceed with or without striking a plasma. In some implementations, the dry development chemistry may include a halide-containing chemistry. A photoresist mask of the photopatterned metal-containing EUV resist film 206 is formed after development by removal of the non-EUV exposed regions 206a. Though **FIGS. 2A–2C** depict negative tone development, it will be understood that positive tone development may alternatively be applied in the present disclosure.

[0078] As shown in **FIG. 2C**, the substrate layer 204 is etched using the photoresist mask 208 to form recessed features in the wafer 200 defined by the photoresist mask 208. The wafer 200 undergoes pattern transfer etching so that an etchant selectively removes the substrate layer 204 relative to the chemically modified photoresist mask 208. Pattern transfer etching may be performed with dry etching or wet etching. For example, dry etching may utilize a fluorine-based plasma etch process or oxygen-based plasma etch process. Pattern transfer etching may etch through the substrate layer 204 according to a pattern defined by the photoresist mask 208. In some embodiments, the photoresist mask 208 preserves or at least substantially preserves the increased line CD after pattern transfer etching.

[0079] Returning to **FIG. 1**, the steps of the process 100 represented by blocks 112, 114 and 116 are conventionally conducted in separate chambers, involving wafer transfer from one process chamber to the next process chamber for subsequent operations. To improve upon efficiency and throughput of the process, the number of steps and/or chambers for the various operations can be reduced by the methods disclosed herein.

[0080] In particular, the efficiency of the conventional process 100 as shown in **FIG. 1** can be improved by performing the steps represented by blocks 112 and 116 in the same process chamber in a manner that eliminates the need for the post dry-development bake 114.

THE INTEGRATED METHODS

[0081] As discussed above, the present disclosure provides methods for films on semiconductor substrates, which may be patterned using EUV or other next generation lithographic techniques. Methods include those where polymerized organometallic materials are produced in a vapor and deposited on a substrate. In some embodiments, dry deposition can employ any useful precursor (e.g., metal halides, capping agents, or organometallic agents described herein). In other embodiments, a spin-on formulation may be used. Deposition processes can include applying a EUV-sensitive material as a resist film or an EUV-sensitive film.

[0082] Such EUV-sensitive films comprise materials which, upon exposure to EUV, undergo changes, such as the loss of bulky pendant ligands bonded to metal atoms. If the unexposed region

includes a dense M-O-M rich material, then EUV induced cleavage can provide intermediates that are more readily removed by positive tone developers.

[0083] Through EUV patterning, areas of the film are created that have altered physical or chemical properties relative to unexposed regions. These properties may be exploited in subsequent processing, such as to dissolve either unexposed or exposed regions or to selectively deposit materials on either the exposed or unexposed regions. In some embodiments, the unexposed film has a hydrophobic surface, and the exposed film has a hydrophilic surface (it being recognized that the hydrophilic properties of exposed and unexposed regions are relative to one another) under the conditions at which such subsequent processing is performed. For example, the removal of material may be performed by leveraging differences in chemical composition, density, and cross-linking of the film. Removal may be by wet processing or dry processing, as further described herein.

[0084] The thickness of the EUV-patternable film formed on the surface of the substrate may vary according to the surface characteristics, materials used, and processing conditions. In various embodiments, the film thickness may range from about 0.5 nm to about 100 nm. Preferably, the film has a sufficient thickness to absorb most of the EUV light under the conditions of EUV patterning. For example, the overall absorption of the resist film may be 30% or less (e.g., 10% or less, or 5% or less), so that the resist material at the bottom of the resist film is sufficiently exposed. In some embodiments, the film thickness is from 10 nm to 20 nm. Without limiting the mechanism, function, or utility of the present disclosure, it is believed that, the processes of the present disclosure can be applied to a wide variety of substrates. Moreover, as discussed above, the deposited films may closely conform to surface features, providing advantages in forming masks over substrates, such as substrates having underlying features, without “filling in” or otherwise planarizing such features.

[0085] The film may be composed of a metal oxide layer deposited in any useful manner. Such a metal oxide layer can be deposited or applied by using any EUV-sensitive material described herein, such as a precursor (e.g., metal-containing precursor, a metal halide, a capping agent, or an organometallic agent) in combination with a counter-reactant. In exemplary processes, a polymerized organometallic material is formed in vapor phase or *in-situ* on the surface of the substrate in order to provide the metal oxide layer. The metal oxide layer may be employed as a film, an adhesion layer, or a capping layer.

[0086] In general, methods can include mixing a vapor stream of a precursor (e.g., a metal-containing precursor, such as an organometallic agent) with an optional vapor stream of a counter-

reactant so as to form a polymerized organometallic material, and depositing the organometallic material onto the surface of the semiconductor substrate. In some embodiments, mixing the precursor and optional counter-reactant can form a polymerized organometallic material. As will be understood by one of ordinary skill in the art, the mixing and depositing aspects of the process may be concurrent, in a substantially continuous process.

[0087] In an exemplary continuous CVD process, two or more gas streams, in separate inlet paths, of sources of precursor and optional counter-reactant are introduced to the deposition chamber of a CVD apparatus, where they mix and react in the gas phase, to form agglomerated polymeric materials (e.g., via metal-oxygen-metal bond formation) or a film on the substrate. Gas streams may be introduced, for example, using separate injection inlets or a dual-plenum showerhead. The apparatus is configured so that the streams of precursor and optional counter-reactant are mixed in the chamber, allowing the precursor and optional counter-reactant to react to form a polymerized organometallic material or a film (e.g., a metal oxide coating or agglomerated polymeric materials, such as via metal-oxygen-metal bond formation).

[0088] For depositing metal oxide, the CVD process is generally conducted at reduced pressures, such as from 0.1 Torr to 10 Torr. In some embodiments, the process is conducted at pressures from 1 Torr to 2 Torr. The temperature of the substrate is preferably below the temperature of the reactant streams. For example, the substrate temperature may be from 0°C to 250°C, or from ambient temperature (e.g., 23°C) to 150°C.

[0089] For depositing agglomerated polymeric materials, the CVD process is generally conducted at reduced pressures, such as from 10 mTorr to 10 Torr. In some embodiments, the process is conducted at from 0.5 to 2 Torr. The temperature of the substrate is preferably at or below the temperature of the reactant streams. For example, the substrate temperature may be from 0°C to 250°C, or from ambient temperature (e.g., 23°C) to 150°C. In various processes, deposition of the polymerized organometallic material on the substrate occurs at rates inversely proportional to surface temperature. Without limiting the mechanism, function or utility of present disclosure, it is believed that the product from such vapor-phase reaction becomes heavier in molecular weight as metal atoms are crosslinked by counter-reactants and is then condensed or otherwise deposited onto the substrate. In various embodiments, the steric hindrance of the bulky alkyl groups further prevents the formation of densely packed network and produces low density films having increased porosity.

[0090] A potential advantage of using dry deposition methods is ease of tuning the composition of the film as it grows. In a CVD process, this may be accomplished by changing the relative

flows of a first precursor and a second precursor during deposition. Deposition may occur between 30°C and 200°C at pressures between 0.01 Torr to 100 Torr, but more generally between about 0.1 Torr and 10 Torr.

[0091] A film (e.g., a metal oxide coating or agglomerated polymeric materials, such as via metal-oxygen-metal bond formation) may also be deposited by an ALD process. For example, the precursor(s) and optional counter-reactant are introduced at separate times, representing an ALD cycle. The precursors react on the surface, forming up to a monolayer of material at a time for each cycle. This may allow for excellent control over the uniformity of film thickness across the surface. The ALD process is generally conducted at reduced pressures, such as from 0.1 Torr to 10 Torr. In some embodiments, the process is conducted from 1 Torr to 2 Torr. The substrate temperature may be from 0°C to 250°C, or from ambient temperature (e.g., 23°C) to 150°C. The process may be a thermal process or, preferably, a plasma-assisted deposition.

[0092] Any of the deposition methods herein can be modified to allow for use of two or more different precursors. In one embodiment, the precursors can include the same metal but different ligands. In another embodiment, the precursors can include different metal groups. In one non-limiting instance, alternating flows of various volatile precursors can provide a mixed metal-containing layer, such as use of a metal alkoxide precursor having a first metal (e.g., Sn) with a silyl-based precursor having a different second metal (e.g., Te).

[0093] Processes herein can be used to achieve a surface modification. In some iterations, a vapor of the precursor may be passed over the wafer. The wafer may be heated to provide thermal energy for the reaction to proceed. In some iterations, the heating can be between about 50°C to about 250°C. In some cases, pulses of the precursor may be used, separated by pump and/or purging steps. For instance, a first precursor may be pulsed between pulses of a second precursor pulses resulting in ALD or ALD-like growth. In other cases, both precursors may be flowed at the same time. Examples of elements useful for surface modification include I, F, Sn, Bi, Sb, Te, and oxides or alloys of these compounds.

[0094] The processes herein can be used to deposit a thin metal oxide or metal by ALD or CVD. Examples include tin oxide (SnO_x), bismuth oxide (BiO_x), and Te. Following deposition, the film may be capped with an alkyl substituted precursor of the form $\text{M}_a\text{R}_b\text{L}_c$, as described elsewhere herein. A counter-reactant may be used to better remove the ligands, and multiple cycles may be repeated to ensure complete saturation of the substrate surface. The surface can then be ready for the EUV-sensitive film to be deposited. One possible method is to produce a thin film of SnO_x . Possible chemistries include growth of SnO_2 by cycling tetrakis(dimethylamino)tin and a counter-

reactant such as water or O₂ plasma. After the growth, a capping agent could be used. For example, isopropyltris(dimethylamino)tin vapor may be flown over the surface.

[0095] Deposition processes can be employed on any useful surface. As referred to herein, the “surface” is a surface onto which a film of the present technology is to be deposited or that is to be exposed to EUV during processing. Such a surface can be present on a substrate (e.g., upon which a film is to be deposited) or on a film (e.g., upon which a capping layer can be deposited).

[0096] Such underlying topographical features may include regions in which material has been removed (e.g., by etching) or regions in which materials have been added (e.g., by deposition) during processing prior to conducting a method of this technology. Such prior processing may include methods of this technology or other processing methods in an iterative process by which two or more layers of features are formed on the substrate. Without limiting the mechanism, function, or utility of the present disclosure, it is believed that, in some embodiments, methods of the present disclosure offer advantages, such as conformance of the films of the present disclosure to underlying features without “filling in” or otherwise planarizing such features and the ability to deposit films on a wide variety of material surfaces.

Exposure of metal-containing resist material

[0097] The photoresist film may be exposed to radiation. The photoresist film is exposed to radiation according to a desired pattern to form exposed and unexposed regions of the photoresist film. Exposure causes a change in the chemical composition and cross-linking in the photoresist film, creating a contrast in etch selectivity that can be exploited for subsequent development.

[0098] EUV exposure of the film can provide EUV exposed regions having activated reactive centers including a metal atom (M), which are produced by EUV-mediated cleavage events. Such reactive centers can include dangling metal bonds, M-H groups, cleaved M-ligand groups, dimerized M-M bonds, or M-O-M bridges.

[0099] EUV exposure can have a wavelength in the range of about 10 nm to about 20 nm in a vacuum ambient, such as a wavelength of from 10 nm to 15 nm, e.g., 13.5 nm. In particular, patterning can provide EUV exposed regions and EUV unexposed regions to form a pattern. In some embodiments, such patterning includes a radiation dose of about 1-50 mJ/cm², 1-40 mJ/cm², 1-30 mJ/cm², 1-20 mJ/cm², or 1-10 mJ/cm².

[0100] The present disclosure can include patterning using EUV, as well as DUV or e-beam. In such patterning, the radiation is focused on one or more regions of the imaging layer. The exposure can be performed such that imaging layer film comprises one or more regions that are not exposed to the radiation. The resulting imaging layer may comprise a plurality of exposed and unexposed

regions, creating a pattern consistent with the creation of transistor or other features of a semiconductor device, formed by addition or removal of material from the substrate in subsequent processing of the substrate. EUV, DUV and e-beam radiation methods and equipment among useful herein include methods and equipment known in the art.

[0101] In some EUV lithography techniques, an organic hard mask (e.g., an ashable hard mask of PECVD amorphous hydrogenated carbon) is patterned using a photoresist process. During photoresist exposure, EUV radiation is absorbed in the resist and in the substrate below, producing highly energetic photoelectrons (e.g., about 100 eV) and in turn a cascade of low-energy secondary electrons (e.g., about 10 eV) that diffuse laterally by several nanometers. These electrons increase the extent of chemical reactions in the resist which increases its EUV dose sensitivity. However, a secondary electron pattern that is random in nature is superimposed on the optical image. This unwanted secondary electron exposure results in loss of resolution, observable line edge roughness (LER) and linewidth variation in the patterned resist. These defects are replicated in the material to be patterned during subsequent pattern transfer etching.

[0102] In various embodiments described herein, a deposition (e.g., condensation) process (e.g., ALD or MOCVD carried out in a PECVD tool) can be used to form a thin film of a metal-containing film, such a photosensitive metal salt or metal-containing organic compound (organometallic compound), with a strong absorption in the EUV (e.g., at wavelengths on the order of 10 nm to 20 nm), for example at the wavelength of the EUVL light source (e.g., 13.5 nm = 91.8 eV). This film photo-decomposes upon EUV exposure and forms a metal mask that is the pattern transfer layer during subsequent etching (e.g., in a conductor etch tool).

[0103] Following deposition, the EUV-patternable thin film is patterned by exposure to a beam of EUV light, in some instances under relatively high vacuum. For EUV exposure, the metal-containing film can then be deposited in a chamber integrated with a lithography platform (e.g., a wafer stepper) and transferred under vacuum so as not to react before exposure. Integration with the lithography tool is facilitated by the fact that EUVL also requires a greatly reduced pressure given the strong optical absorption of the incident photons by ambient gases such as H₂O, O₂, etc. In other embodiments, the photosensitive metal film deposition and EUV exposure may be conducted in the same chamber.

[0104] Photolithography processes can involve one or more bake steps, to facilitate the chemical reactions required to produce chemical contrast between exposed and unexposed regions of the photoresist. For high volume manufacturing (HVM), such bake steps can be performed on tracks where the wafers are baked on a hot-plate at a pre-set temperature under ambient air or in some

cases N₂ flow. More careful control of the bake ambient as well as introduction of additional reactive gas component in the ambient during these bake steps can help further reduce the dose requirement and/or improve pattern fidelity.

[0105] According to various aspects of this disclosure, one or more post-treatments to metal and/or metal oxide-based photoresists after deposition (e.g., post-application bake (PAB) or another post-application treatment) and/or exposure (e.g., post-exposure bake (PEB), which can be omitted; or another post-exposure treatment) and/or development (e.g., post-development bake (PDB) or another post-development treatment) are capable of increasing material property differences between exposed and unexposed photoresist and therefore decreasing dose-to-size (DtS), improving PR profile, and improving line edge and width roughness (LER/LWR) after subsequent dry development. Such processing can involve a thermal process with the control of temperature, gas ambient, and moisture, resulting in improved dry development performance in processing to follow. In some instances, a remote plasma might be used. Yet in certain instances, PAB and/or PEB and/or PDB are not performed.

[0106] In the case of post-application processing (e.g., PAB), a thermal process with control of temperature (e.g., with heating or cooling), gas atmosphere (e.g., air, H₂O, CO₂, CO, O₂, O₃, CH₄, CH₃OH, N₂, H₂, NH₃, N₂O, NO, Ar, He, or their mixtures) or under vacuum, and moisture can be used after deposition and before exposure to change the composition of unexposed metal and/or metal oxide photoresist. The change can increase the EUV sensitivity of the material and thus lower dose to size and edge roughness can be achieved after exposure and dry development.

[0107] In the case of post-exposure processing (e.g., PEB), a thermal process with the control of temperature, gas atmosphere (e.g., air, H₂O, CO₂, CO, O₂, O₃, CH₄, CH₃OH, N₂, H₂, NH₃, N₂O, NO, Ar, He, or their mixtures) or under vacuum, and moisture can be used to change the composition of both unexposed and exposed photoresist. The change can increase the composition/material properties difference between the unexposed and exposed photoresist and the etch rate difference of dry development etch gas between the unexposed and exposed photoresist. A higher etch selectivity can thereby be achieved. Due to the improved selectivity, a squarer PR profile can be obtained with improved surface roughness, and/or less photoresist residual/scum. In particular embodiments, PEB can be performed in air and in the optional presence of moisture and CO₂. In other embodiments, PEB can be omitted.

[0108] In the case of post-development processing (e.g., post-development bake or PDB), a thermal process with the control of temperature, gas atmosphere (e.g., air, H₂O, CO₂, CO, O₂, O₃, CH₄, CH₃OH, N₂, H₂, NH₃, N₂O, NO, Ar, He, or their mixtures) or under vacuum (e.g., with UV),

and moisture can be used to change the composition of the unexposed photoresist. In particular embodiments, the condition also includes use of plasma (e.g., including O₂, O₃, Ar, He, or their mixtures). The change can increase the hardness of material, which can be beneficial if the film will be used as a resist mask when etching the underlying substrate.

[0109] In these cases, in alternative implementations, the thermal process could be replaced by a remote plasma process to increase reactive species to lower the energy barrier for the reaction and increase productivity. Remote plasma can generate more reactive radicals and therefore lower the reaction temperature/time for the treatment, leading to increased productivity.

[0110] Accordingly, one or multiple processes may be applied to modify the photoresist itself to increase wet or dry development selectivity. This thermal or radical modification can increase the contrast between unexposed and exposed material and thus increase the selectivity of the subsequent development step. The resulting difference between the material properties of unexposed and exposed material can be tuned by adjusting process conditions including temperature, gas flow, moisture, pressure, and/or RF power.

[0111] For wet-developed or dry-developed resist films, the treatment temperature in a PAB or PEB can be varied to tune and optimize the treatment process, for example from about 90°C to 250°C for PAB and about 170°C to 250°C or more for PEB.

[0112] In particular embodiments, the PAB and/or PEB treatments may be conducted with gas ambient flow in the range of 100 sccm to 10000 sccm, moisture content in the amount of a few percent up to 100% (e.g., 20%–50%), at a pressure between atmospheric and vacuum, and for a duration of about 30 s to 15 min, for example about 1 to 2 min. In particular embodiments, PEB is omitted.

[0113] Depending on the selectivity requirements/constraints of the semiconductor processing operation, a thermal treatment such as described herein can be used to lower the EUV dose needed. Or, if higher selectivity is required and higher dose can be tolerated, much higher selectivity, up to 100 times exposed vs. unexposed, can be obtained.

[0114] Yet other steps can include *in-situ* metrology, in which physical and structural characteristics (e.g., critical dimension, film thickness, etc.) can be assessed during the photolithography process. Modules to implement *in-situ* metrology include, e.g., scatterometry, ellipsometry, downstream mass spectroscopy, and/or plasma enhanced downstream optical emission spectroscopy modules.

[0115] A substrate may be provided in a process chamber, where the substrate is a semiconductor substrate comprising a substrate layer and the post-developed photoresist mask

over the substrate layer. The substrate layer may be underlying the post-developed photoresist mask and may include any suitable material to facilitate the patterning process. The substrate layer may be etched with high selectivity to the post-developed photoresist mask. In some implementations, the substrate layer may include spin-on carbon (SoC), spin-on glass (SOG), amorphous carbon (a-C), tin oxide (e.g., SnO_x), silicon (e.g., a-Si), silicon oxide (e.g., SiO_x), silicon oxynitride (e.g., SiO_xN_y), silicon oxycarbide (e.g., SiO_xC_y), silicon nitride (Si_3N_4), silicon carbide (SiC_x), titanium oxide (e.g., TiO_2), titanium nitride (e.g., TiN), tungsten (e.g., W), doped carbon (e.g., W-doped C), tungsten oxide (e.g., WO_x), hafnium oxide (HfO_2), zirconium oxide (e.g., ZrO_2), or aluminum oxide (Al_2O_3).

[0116] The metal-containing photoresist may be dry or wet deposited on the substrate layer. The metal-containing photoresist may be provided as a positive tone or negative tone resist having EUV-exposed and EUV-unexposed regions after EUV exposure. After deposition, the metal-containing photoresist may be photopatterned in an EUV lithography chamber (scanner). After exposure and an optional PEB treatment, the metal-containing photoresist may undergo development to selectively remove portions (e.g., EUV-unexposed portions) of the metal-containing photoresist to form a patterned photoresist mask over the substrate layer. In some implementations, the metal-containing photoresist is a metal-containing EUV photoresist, where the metal-containing EUV photoresist is an organo-metal oxide or organo-metal containing film. For instance, the metal-containing EUV photoresist may include Sn, O, and C atoms.

[0117] The process chamber may provide an enclosed space for treating the substrate after development. Chamber walls in the process chamber may be fabricated from stainless steel, aluminum, plastic, or other suitable material. In some embodiments, the chamber walls are coated with corrosion-resistant films, such as polymers or inorganic coatings. The process chamber may include a substrate support (e.g., pedestal or electrostatic chuck) on which the substrate is supported. In some embodiments, the process chamber for post-development treatment may be a deposition chamber, a bevel edge and/or backside clean chamber, a PAB treatment chamber, a PEB treatment chamber, a development chamber, or an etch chamber. That way, the process chamber for post-development treatment may be the same chamber used in a previous operation for photoresist processing or the same chamber used in a subsequent operation for photoresist processing, thereby minimizing substrate transfers to reduce exposure to air breaks in between operations. The process chamber may include one or more heating elements for exposing the substrate to elevated temperatures. In some embodiments, the one or more heating elements may include one or more infrared (IR) lamps or one or more light-emitting-diodes (LEDs) located in a

substrate support for controlling a temperature of the substrate. The process chamber may include one or more gas lines for delivering gas into the process chamber. For example, the one or more gas lines may include a showerhead for supplying reactive gases towards the substrate in the process chamber. In some implementations, the process chamber may be a plasma-generating chamber or may be coupled to a plasma-generating chamber separate from the process chamber. The plasma-generating chamber may be an inductively-coupled plasma (ICP) reactor, a transformer-coupled plasma (TCP) reactor, or a capacitively-coupled plasma (CCP) reactor. In some cases, the process chamber further includes one or more gas outlets for exhausting gases, which may or may not be coupled to a vacuum pump to maintain a desired pressure within the process chamber.

[0118] The post-developed metal-containing photoresist mask is treated using one or more of the following operations: (i) thermally annealing the post-developed metal-containing photoresist mask, (ii) exposing the post-developed metal-containing photoresist mask to plasma, (iii) exposing the post-developed metal-containing photoresist mask to one or more reactive gases, and (iv) selectively depositing a protective layer on the post-developed metal-containing photoresist mask. Post-development treatment of the substrate may utilize one of the foregoing thermal anneal, plasma, chemical, or selective deposition treatment operations, or a combination of the foregoing treatments. The post-development treatment improves the performance of the metal-containing photoresist mask during pattern transfer etching. The foregoing thermal anneal, plasma, chemical, and selective deposition treatment techniques are discussed in detail below.

[0119] The substrate layer is etched to form recessed features using the post-developed metal-containing photoresist mask. This process may be referred to as pattern transfer or pattern transfer etching. The etch may selectively remove portions of the substrate layer without removing the post-developed metal-containing photoresist mask. A wet or dry etchant may be employed to etch through the portions of the substrate layer exposed by post-developed metal-containing photoresist mask. The metal-containing photoresist mask may define a pattern by which features are to be etched. Features are etched through the substrate layer according to the pattern defined by the metal-containing photoresist mask. After post-development treatment, the metal-containing photoresist mask may have an increased line CD and/or improved etch resistance during pattern transfer etching. The features to be etched can maintain or substantially maintain the line CD provided by the metal-containing photoresist mask. In some cases, the metal-containing photoresist mask may have reduced defectivity and/or roughness. As a result, defects and roughness do not get transferred to the features that are formed after pattern transfer etching.

Thermal Treatment

[0120] In some implementations, the substrate may be thermally treated by heating the substrate to an elevated temperature. Thermal treatment of the substrate may serve to reduce defects and reduce roughness from the metal-containing photoresist mask prior to pattern transfer etching. In particular, thermal treatment of the substrate may improve chemical contrast in the metal-containing photoresist mask by removing scum.

[0121] After wet or dry development, residue or scum may remain on the substrate. The residue or scum may remain in areas of the photoresist mask that were removed by development. The residue or scum may include residual etch byproducts adsorbed on surfaces of the substrate. For example, the vapors of halogens used in certain development chemistries may react with moisture or oxygen to form residual etch byproducts that are difficult to remove. Wet processing techniques often employ moisture and/or oxygen, which more easily leads to scum and residue formation. In some cases, the residue may include high metal concentrations or particles or clusters of metal oxide (e.g., SnO_x) that can contribute to a loss of chemical contrast during pattern transfer and contaminate downstream processing tools.

[0122] After wet or dry development, roughness may form on sidewalls of etched features in a developed pattern of the photoresist mask. Some of this may be attributed to stochastics or non-optimal Gaussian distribution of light resulting in partially or fully exposed material in areas where photoresist should remain unexposed or vice versa. Moreover, scumming on sidewalls of etched features of the photoresist mask may exacerbate roughness.

[0123] During thermal treatment, the substrate may be heated to an elevated temperature between about 50°C and about 500°C, between about 100°C and about 400°C, between about 100°C and about 300°C, or between about 100°C and about 250°C. The substrate may be heated to the elevated temperature using one or more temperature-controllable elements in the process chamber. The pressure may be maintained between about 0.1 Torr and about 760 Torr, for example between about 0.1 Torr and about 1 Torr in some cases. The substrate may be exposed to the elevated temperature for a duration between about 1 minute and about 10 minutes, for example between about 2 minutes and about 5 minutes in some cases. In some implementations, thermal treatment is performed with one or more inert gases. For instance, thermal treatment may be performed with a flow of nitrogen (N_2), helium (He), neon (Ne), argon (Ar), or xenon (Xe). In some implementations, thermal treatment is performed in atmosphere.

[0124] Higher temperatures in post-development thermal treatment may lead to increased descumming, reduced defectivity, and reduced roughness. However, higher temperatures may

simultaneously lead to reduced line CD. It has been observed that higher temperatures during thermal anneal result in photoresist lateral shrinkage and photoresist height shrinkage. The reduced line CD results in a higher dose-to-size. Post-development thermal treatment may suffer from a tradeoff between reduced defectivity and roughness with a higher dose-to-size. This limits the thermal treatment to a desired temperature range and desired treatment duration to optimize the benefits of reduced defectivity and roughness while minimizing increases in dose-to-size.

Plasma Treatment

[0125] In some implementations, the substrate may be exposed to plasma for post-development treatment. Plasma treatment may serve to densify the metal-containing photoresist mask and lower roughness prior to pattern transfer etching. In some cases, plasma treatment may further improve chemical contrast in the metal-containing photoresist mask by removing scum. Plasma treatment may employ plasma of inert gas species or plasma of reactive gas species. Plasma of reactive gas species may chemically react with the metal-containing photoresist mask or selectively deposit a protective film on the metal-containing photoresist mask.

[0126] Exposure to plasma may be facilitated by generating plasma in a remote plasma generator or generating plasma in the process chamber where the substrate is being treated. One or more gases may be flowed to a plasma-generating region, which may be a remote plasma generator or the process chamber, and plasma is ignited. A plasma-generating chamber may be an inductively-coupled plasma (ICP), transformed-coupled plasma (TCP), or capacitively-coupled plasma (CCP) reactor. Plasma energy is provided to activate one or more gases into ions, radicals, neutral species, and other plasma-activated species. Ions, radicals, neutral species, and other plasma-activated species may interact with the metal-containing photoresist mask to improve the performance of the metal-containing photoresist mask during pattern transfer etching.

[0127] The one or more gases may include oxygen-containing species such as oxygen (O₂), carbon dioxide (CO₂), and carbon monoxide (CO). Additionally or alternatively, the one or more gases may include halogen-containing species such as boron trichloride (BCl₃), silicon tetrachloride (SiCl₄), tin tetrachloride (SnCl₄), tungsten hexafluoride (WF₆), and difluoromethane (CH₂F₂). Additionally or alternatively, the one or more gases may include inert gas species such as nitrogen (N₂), helium (He), neon (Ne), argon (Ar), and xenon (Xe). Other gases may include hydrogen (H₂), ammonia (NH₃), hydrogen halides (HCl, HBr, HF, HI), and various hydrocarbons (C_xH_y) such as methane (CH₄). In some cases, the plasma may be an oxygen-based plasma, nitrogen-based plasma, inert gas plasma, and/or carbon-based plasma. In some implementations, the plasma is a remote plasma. In some other implementations, the plasma is an *in-situ* plasma.

[0128] Process conditions for plasma treatment may be tuned to achieve a desired result. Such process conditions include but are not limited to plasma power, plasma frequency, plasma exposure time, bias voltage, duty cycle, temperature (e.g., pedestal temperature), pressure (e.g., chamber pressure), and flow rate of the one or more gases. The plasma in operation may be generated at a plasma power less than about 6 kW, such as between about 50 W and about 4000 W, between about 50 W and about 1000 W, or between about 100 W and about 500 W. In some instances, the plasma may be provided at a low plasma power and high ion energy. A directionality of the plasma may be controlled by the bias voltage. In some implementations, the bias voltage may be applied that is between about 1 V and about 500 V, between about 10 V and about 400 V, or between about 30 V and about 300 V. Plasma treatment may be applied for a duration between about 0.5 seconds and about 120 seconds, between about 1 second and about 60 seconds, or between about 2 seconds and about 40 seconds. Plasma treatment may modulate duty cycles of the plasma in operation to achieve the desired result, where the RF power supply may deliver plasma at any suitable duty cycle, such as between about 1% and about 99%, or between about 10% and about 90%. In some embodiments, chamber pressure may be between about 0.1 Torr and about 760 Torr, or between about 0.1 Torr and about 1 Torr in some cases. In some embodiments, a substrate temperature may be between about 0°C and about 400°C, between about 50°C and about 300°C, or between about 100°C and about 250°C.

[0129] As discussed below, plasma treatment may be accompanied by reactive gas species. Plasma of reactive gas species may induce chemical reactions in the metal-containing photoresist mask to improve mask properties such as etch resistance. Plasma of reactive gas species may selectively deposit a protective film on the metal-containing photoresist mask to increase line CD and reduce dose-to-size.

Chemical Treatment

[0130] In some implementations, the metal-containing photoresist mask may be exposed to one or more reactive gas species. Reactive gas species may chemically react with the metal-containing photoresist mask. In fact, certain reactive gas species may be reactive with the metal-containing photoresist mask and unreactive with the substrate layer of the substrate. In some implementations, the reactive gas species may convert an entirety or a substantial entirety of the metal-containing photoresist mask from a first material to a second material. The change in chemistry of the metal-containing photoresist mask may alter one or more properties of the metal-containing photoresist mask. In some implementations, the reactive gas species may convert only an outer portion of the metal-containing photoresist mask from a first material to a second material,

which may be used as a protective film as described further below.

[0131] The reactive gas species may react with the metal-containing photoresist mask to increase line CD and reduce dose-to-size. The reactive gas species may react with the metal-containing photoresist mask to reduce roughness (e.g., LWR/LER) or at least maintain the same roughness. The reactive gas species may densify the metal-containing photoresist mask. In some cases, the reactive gas species may react with the metal-containing photoresist mask to reduce defectivity (e.g., scumming). Additionally, the reactive gas species may reduce outgassing such as tin outgassing from the metal-containing photoresist mask. In some cases, the reactive gas species may react with the metal-containing photoresist mask to increase an etch resistance of the photoresist mask during subsequent etch operations. By way of an example, the reactive gas species may increase line CD and at least substantially maintain the increased line CD of the photoresist mask after pattern transfer etching.

[0132] The reactive gas species may be more reactive with the metal-containing photoresist relative to the underlying substrate layer(s). In particular implementations, chemical treatment using reactive gas species takes advantage of the chemistry of an EUV photoresist mask. The EUV photoresist mask may be composed of an organometallic oxide film such as an organotin oxide film having Sn, O, and C atoms. The organotin oxide film may be comprised of networks of Sn-Sn bonds, Sn-H bonds, Sn-C bonds, Sn-OH bonds, Sn-O bonds, Sn-O-Sn bonds, and Sn-O-C bonds. The reactive gas species may react with one or more elements of the organotin oxide film by oxidation, reduction, insertion, abstraction, or other chemical reaction mechanism to induce a chemical change in the EUV photoresist mask. In some instances, the reactive gas species may include carbon monoxide (CO), where tin species may have a catalytic reaction with the carbon monoxide. Without being limited by any theory, compounds of SnOC_x react with CO to form a new compound of $\text{SnOC}_x(\text{CO})_y$. The chemical reaction induces a change in the EUV photoresist mask by expanding the line CD. In some implementations, the etch resistance of the new compound in the EUV photoresist mask is improved.

[0133] Reactive gas species other than CO may be employed to induce a chemical reaction in the EUV photoresist mask. Examples of useful reactive gas species may include but are not limited to air, water vapor (H_2O), hydrogen peroxide (H_2O_2), carbon dioxide (CO_2), oxygen (O_2), ozone (O_3), methane (CH_4), methanol (CH_3OH), ethanol ($\text{CH}_3\text{CH}_2\text{OH}$), nitrogen (N_2), hydrogen (H_2), ammonia (NH_3), nitrous oxide (N_2O), nitric oxide (NO), nitrogen dioxide (NO_2), acetyl acetone ($\text{C}_5\text{H}_8\text{O}_2$), formic acid (CH_2O_2), acetic acid (CH_3COOH), hydrogen cyanide (HCN), boron trichloride (BCl_3), silicon tetrachloride (SiCl_4), chlorine (Cl_2), bromine (Br_2), hydrogen chloride

(HCl), hydrogen bromide (HBr), hydrogen iodide (HI), hydrogen fluoride (HF), fluoromethane (CH_3F), difluoromethane (CH_2F_2), and combinations thereof. In some cases, the reactive gas species may include an oxygen-containing gas, a carbon-containing gas, a hydrogen-containing gas, a nitrogen-containing gas, a halogen-containing gas, or combinations thereof. Other reactive gas species may include metal precursors such as tungsten hexafluoride (WF_6), tin tetrachloride (SnCl_4), molybdenum hexafluoride (MoF_6), molybdenum dichloride dioxide (MoO_2Cl_2), and molybdenum chloride (MoCl_5). Other reactive gas species may include metal organic precursors such as tin tetrakis(dimethylamide) ($\text{Sn}(\text{N}(\text{CH}_3)_2)_4$), hafnium tetrakis(dimethylamide) ($\text{Hf}(\text{N}(\text{CH}_3)_2)_4$), dimethyl aluminum ($(\text{CH}_3)_2\text{Al}$), trimethyl aluminum ($(\text{CH}_3)_3\text{Al}$), titanium isopropoxide ($\text{Ti}(\text{OCH}(\text{CH}_3)_2)_4$), tungsten carbonyl ($\text{W}(\text{CO})_x$), molybdenum carbonyl ($\text{Mo}(\text{CO})_x$), ruthenium carbonyl ($\text{Ru}(\text{CO})_x$), iron carbonyl ($\text{Fe}(\text{CO})_x$), and combinations thereof. Thus, in some cases, the reactive gas species may include a metal halide or organometallic precursor such as a metal carbonyl precursor. Conventional polymer-based photoresist materials may not be reactive with metal halides or certain organometallic precursors, but metal-containing or metal oxide-containing photoresist materials of the present disclosure may be more prone to react with metal halides and organometallic precursors. Without being limited by any theory, where there are M-OH bonds in an organometallic photoresist, M-O-M' bridges may form where M' is from the metal precursor (e.g., metal halide or organometallic precursor).

[0134] The reactive gas species may be co-flowed with other gases. In some implementations, the reactive gas species may be co-flowed with an inert gas species such as helium, neon, argon, or xenon. In some implementations, combinations of reactive gas species may be co-flowed with each other. By way of illustration, a halogen-containing gas such as boron trichloride may be co-flowed with a carbon-containing gas such as methane. In another example, a metal precursor such as tungsten hexafluoride may be co-flowed with a carbon-containing gas such as difluoromethane. The reactive gas species, alone or in combination with other reactive gas species, may convert the photoresist mask to another material or selectively deposit a protective film on the photoresist mask.

[0135] In some implementations, the reactive gas species may be supplied to the process chamber from a gas source fluidly coupled to the process chamber. Gas sources such as gas storage tanks may be fluidly coupled to the process chamber via gas supply lines. Gas reactants may be pre-mixed prior to entering the process chamber or mixed upon entering the process chamber. In some implementations, the reactive gas species may be generated *in-situ* in the process chamber. Gas reactants may react with one another to form reaction products that react with the metal-

containing photoresist mask to induce chemical change. Or a gas reactant may react with one or more chamber components (e.g., metal-based chamber lines) to form a reaction product that reacts with the metal-containing photoresist mask to induce chemical change. The gas reactant may be a carbon-containing precursor that reacts with a metallic chamber component to form an organometallic precursor. This reaction may be driven thermally to generate the organometallic precursor. For example, carbon monoxide supplied into the process chamber may react with iron-containing chamber lines to form iron carbonyl ($\text{Fe}(\text{CO})_x$) that readily reacts with an EUV photoresist mask, thereby increasing the line CD of the EUV photoresist mask. Without being limited by any theory, the iron carbonyl causes deposition of iron oxide on the EUV photoresist mask. In another example, carbon monoxide or carbon dioxide supplied into the process chamber may react with tungsten-containing chamber lines (e.g., hotwire) to form tungsten carbonyl ($\text{W}(\text{CO})_x$) that readily reacts with an EUV photoresist mask.

[0136] Chemical treatment of the metal-containing photoresist mask involving one or more reactive gas species may be employed with one or both of thermal treatment and plasma treatment. Whereas thermal treatment or plasma treatment alone may exhibit tradeoffs, such tradeoffs may be offset by further applying a chemical treatment to the metal-containing photoresist mask. Specifically, chemical treatment may be combined with thermal treatment so that one or more reactive gas species are flowed to the metal-containing photoresist mask at elevated temperatures. Though elevated temperatures may decrease line CD, the one or more reactive gas species may increase line CD in the metal-containing photoresist mask. In fact, the increased line CD resulting from the one or more reactive gas species may exceed the decreased line CD resulting from the elevated temperatures. This reduces dose-to-size while reducing defectivity and roughness in the metal-containing photoresist mask. In some embodiments, chemical treatment may be combined with plasma treatment so that radicals and/or ions of the reactive gas species are flowed to the metal-containing photoresist mask. The radicals and/or ions may increase reactivity of the reactive gas species with the metal-containing photoresist mask. The metal-containing photoresist mask may be exposed to one or more reactive gas species in plasma, which can change the chemical composition of the metal-containing photoresist mask and increase line CD and density. This can be done without necessarily compromising defectivity or roughness of the metal-containing photoresist mask. Plasma may be applied at a power to avoid damage to the substrate.

[0137] Inducing a surface reaction or bulk reaction in the metal-containing photoresist mask may occur by applying energy to the reaction. Some amount of energy from thermal exposure and/or plasma exposure may be sufficient to induce the surface reaction or bulk reaction.

Accordingly, process conditions such as temperature and plasma power may be tuned to achieve the desired outcome. In some implementations, a substrate temperature may be between about 0°C and about 400°C, between about 50°C and about 300°C, or between about 100°C and about 250°C during chemical treatment with one or more reactive gas species. In some implementations, plasma power may be less than about 6 kW, between about 50 W and about 4000 W, between about 50 W and about 1000 W, or between about 100 W and about 500 W during chemical treatment with the one or more reactive gas species.

[0138] Other process conditions such as plasma frequency, exposure time, bias voltage, pressure, and flow rates may be tuned to facilitate chemical treatment using the one or more reactive gas species. In some implementations, the bias voltage may be applied that is less than about 800 V, between about 0 V and about 500 V, between about 10 V and about 400 V, or between about 30 V and about 300 V. In some implementations, exposure to the one or more reactive gas species may be applied for a duration between about 1 second and about 10 minutes, between about 5 seconds and about 8 minutes, or between about 30 seconds and about 4 minutes. In some implementations, chamber pressure may be between about 0.1 Torr and about 760 Torr, or between about 1 mTorr and about 100 mTorr in some cases. A first reactive gas species may be flowed into the process chamber at a flow rate between about 1 sccm and about 1000 sccm, between about 2 sccm and about 500 sccm, or between about 5 sccm and about 300 sccm. An optional second reactive gas species may be co-flowed into the process chamber at a flow rate between about 5 sccm and about 1000 sccm, between about 10 sccm and about 500 sccm, or between about 20 sccm and about 300 sccm. An optional inert gas species may be co-flowed into the process chamber at a flow rate between about 20 sccm and about 2000 sccm, between about 30 sccm and about 1000 sccm, or between about 50 sccm and about 500 sccm. By way of an example, carbon monoxide may be flowed into the process chamber at a flow rate of about 500 sccm at a substrate temperature of about 240°C for a duration between about 20 seconds and about 5 minutes. The carbon monoxide may react with an EUV photoresist mask to change the chemical composition of the EUV photoresist mask. In an alternative example, tungsten hexafluoride may replace carbon monoxide to react with the EUV photoresist mask to change the chemical composition of the photoresist mask. The EUV photoresist mask may exhibit increased etch resistance during subsequent pattern transfer etching.

[0139] Certain embodiments of the disclosed methods are illustrated by FIG. 3. In FIG. 3, blocks 302 – 310 represent the same operations as blocks 102-110 of FIG. 1. The operation at block 312 represents an integrated dry development and pattern transfer (etch) operation, which is

performed in a single process chamber. Operation 312 can be performed in place of the operations 112, 114 and 116 of **FIG. 1**. In so doing, productivity is improved and defects, overlay and CD can be controlled more effectively. Combining the steps of dry development and pattern transfer allows for reduction of metal outgassing such as tin outgassing without the need to add an additional step of post-dry development bake which takes place in a different process chamber. The combination of dry development and etch in a single chamber is counter-intuitive due to the diametrically opposed process conditions each operation requires, particularly in terms of pressure. They are conventionally performed in different chambers with different process tools, to practically manage pressure requirements. Thermal processes require high pressure to obtain a high etch rate. The high partial pressure leads to better selectivity. Conversely, for plasma processes, low pressures are required to achieve anisotropic etch. If performed in a single process chamber, a pressure drop of several orders of magnitude must be rapidly accomplished, in from about 1 to about 10 seconds. Dry development may take place at a pressure of about 400 to 500 mTorr; but etch is performed at a pressure of about 20 to 50 mTorr. Use of a throttle valve, a specialized pump, multiple pumps or control of the flow of process gases can effect the pressure drop rapidly; on the order of ten seconds or less. In some embodiments, the pressure drop takes place in 8 seconds, 7 seconds, 6 seconds, 5 seconds, 4 seconds, 3 seconds or 2 seconds.

[0140] When the metal-containing photoresist is a metal oxide such as tin oxide, metal outgassing such as tin outgassing can be controlled without the need for a post-dry develop bake.

[0141] For the purposes of this disclosure, “metal” used in this context should be understood to mean conductor with a maximum resistivity of 500 micro Ohm cm, including metals and conductive metal salts, in particular conductive metal nitrides, e.g., TiN.

[0142] “Tin oxide” is referred to herein as including any and all stoichiometric possibilities for Sn_xO_y , including integer values of x and y and non-integer values of x and y. For example, “tin oxide” includes compounds having the formula SnO_n , where $1 \leq n \leq 2$, where n can be an integer or non-integer values. “Tin oxide” can include sub-stoichiometric compounds such as $\text{SnO}_{1.8}$. “Tin oxide” also includes tin dioxide (SnO_2 or stannic oxide) and tin monoxide (SnO or stannous oxide). “Tin oxide” also includes both natural and synthetic variations and also includes any and all crystalline and molecular structures. “Tin oxide” also includes amorphous tin oxide.

[0143] Exemplary methods for performing the integrated operation of block 312 are described in greater detail in **FIGS. 4** and **5**. The operations of the process 300 may be performed in different orders and/or with different, fewer, or additional operations. One or more operations of the process

300 may be performed using an apparatus described in any one of **FIGS. 6-9**. In some embodiments, the operations of the process 300 may be implemented, at least in part, according to software stored in one or more non-transitory computer readable media.

[0144] **FIG. 4** illustrates a process 400 for integrated dry development and etch in a single process chamber in accordance with certain disclosed embodiments. The operation at block 410 is a thermal dry development. As described herein, dry development processes can be used to process a film. Non-limiting processes can include use of halides, such as HCl- or HBr-based processes. While this disclosure is not limited to any particular theory or mechanism of operation, the approach is understood to leverage the chemical reactivity of the dry-deposited EUV photoresist films with the clean chemistry (e.g., HCl, HBr, and BCl₃) to form volatile products using vapors or plasma. Such volatile products can be removed in any manner (e.g., by treating with an aqueous acid, as described herein). The dry-deposited EUV photoresist films can be removed with etch rates of up to 1 nm/s. The quick removal of dry-deposited EUV photoresist films by these chemistries is applicable to chamber cleaning, backside clean, bevel clean, and PR developing. Although the films can be removed using vapors at various temperatures (e.g., HCl or HBr at a temperature greater than -10°C, or BCl₃ at a temperature greater than 80°C, for example), a plasma can also be used to further accelerate or enhance the reactivity.

[0145] In thermal development processes, the substrate is exposed to dry development chemistry (e.g., a Lewis Acid) in a vacuum chamber (e.g., oven). Suitable chambers can include a vacuum line, a dry development hydrogen halide chemistry gas (e.g., HBr, HCl) line, and heaters for temperature control. In some embodiments, the chamber interior can be coated with corrosion resistant films, such as organic polymers or inorganic coatings. One such coating is polytetrafluoroethylene ((PTFE), e.g., Teflon™). Such materials can be used in thermal processes of this disclosure without risk of removal by plasma exposure.

[0146] The process conditions for the dry development may be reactant flow of 100 sccm to 500 sccm (e.g., 500 sccm HBr or HCl), temperature of -10°C to 120°C (e.g., -10°C), pressure of 1 mTorr to 500 mTorr (e.g., 300 mTorr) with no plasma and for a time of about 10 sec to 1 min, dependent on the photoresist film and their composition and properties. In some embodiments, the pressure is 400- 500 mTorr for a duration of 10 to 20 seconds.

[0147] Between blocks 410 and 420, flow path 415 represents the rapid pressure change procedure occurring within the chamber. The required pressure drop is accomplished within the process chamber enabling both high and low pressure processes to occur in the same chamber. The pressure change may be managed by a throttle valve, a specialized pump, multiple pumps,

control of the flow of process gases or a combination of these techniques. If more than one pump is utilized, one of the pumps may be a roughing pump and one of the pumps may be a turbo pump.

[0148] Following thermal dry development, the operation at block 420 represents a plasma dry development step with O₂ flash treatment. Plasma processes include transformer coupled plasma (TCP), inductively coupled plasma (ICP) or capacitively coupled plasma (CCP), employing equipment and techniques among those known in the art. For example, a process may be conducted at a pressure of > 0.5 mTorr (e.g., such as from 1 mTorr to 100 mTorr), at a power level of < 1000 W (e.g., < 500 W). Temperatures may be from 30°C to 300°C (e.g., 30°C to 120°C), at flow rate of 100 to 1000 standard cubic centimeters per minute (sccm), e.g., about 500 sccm, for from 1 to 3000 seconds (e.g., 10 seconds to 600 seconds).

[0149] Where the halide reactant flows are of hydrogen gas and halide gas, a remote plasma/UV radiation is used to generate radicals from the H₂ and Cl₂ and/or Br₂, and the hydrogen and halide radicals are flowed to the reaction chamber to contact the patterned EUV photoresist on the substrate layer of the wafer. Suitable plasma power may range from 100 W to 500 W, with no bias. It should be understood that while these conditions are suitable for some processing reactors, a wider range of process conditions may be used according to the capabilities of the processing reactor.

[0150] The O₂ flash treatment process at block 420 includes delivering a flash gas of 1,000 sccm to 2,000 sccm of oxygen (O₂) to the process chamber. In certain embodiments, a radio frequency power of 100 to 3,000 watts is delivered at 13.56 MHz to transform the flash gas into a plasma. A pressure of 20 mTorr to 100 mTorr is provided. This backside cleaning process may be referred to as an “O₂ flash” operation, since the time during which the power is delivered is relatively fast, from about 0.5 seconds to about 4 seconds. The O₂ flash operation induces pattern transfer.

[0151] Subsequent to the pattern transfer, an optional wet cleaning process 430 may be performed to remove metal oxide as well as other contaminants. The wet cleaning process occurs after opening the chamber. For the backside and bevel clean process, the vapor and/or the plasma can be limited to a specific region of the wafer to ensure that only the backside and the bevel are removed, without any film degradation on the frontside of the wafer. The dry-deposited EUV photoresist films being removed are generally composed of Sn, O and C, but the same clean approaches can be extended to films of other metal oxide resists and materials. In addition, this approach can also be used for film strip and photoresist rework.

[0152] For a wet cleaning, solutions include compounds such as tetramethylammonium hydroxide (TMAH), complexing amines such as ethylene diamine or diethylene triamine, semi-

aqueous fluoride strippers or diluted hydrofluoric acid strippers. Metal oxides can be removed by using an acid such as citric acid, acetic acid, octanoic acid or other organic or inorganic acids can be used. Additionally, very dilute (i.e. less than 0/1%) peroxide-containing acids such as sulfuric-peroxide mixtures can also be used. Combinations of any of the above-mentioned wet cleaners may also be utilized.

[0153] FIG. 5 illustrates an alternative process 500 for integrated dry development and etch in a single process chamber in accordance with certain disclosed embodiments. The operation at block 510 represents thermal dry development as described for block 410 in FIG. 4 above.

[0154] Between blocks 510 and 520, flow path 515 represents the rapid pressure change procedure occurring within the chamber. As described for flow path 415 above, the required pressure drop is accomplished within the process chamber enabling both high and low pressure processes to occur in the same chamber. The pressure change may be managed by a throttle valve, a specialized pump, multiple pumps, control of the flow of process gases or a combination of these techniques. If more than one pump is utilized, one of the pumps may be a roughing pump and one of the pumps may be a turbo pump.

[0155] Following thermal dry development, the operation at block 520 represents a plasma descum step and pattern transfer. Scum refers to the non-desired carbon-based material such as footings, stringers or other forms of undesirable substrate surface roughness remaining on a substrate after lithography. The scum may be removed either by an atomic layer etching process with plasma or thermally.

[0156] Operation 530 is a selective deposition of metal. Selective deposition may be utilized for photoresist repair such as performing selective metal oxide deposition on a photoresist for photoresist hardening; or for adding more selectivity to the photoresist during pattern transfer. Metal oxides for the selective deposition include SnO_x .

[0157] Subsequent to selective deposition 530, an optional wet cleaning process 540 may be performed, similar to the operation as described for block 430 in FIG. 4 above.

[0158] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application or uses. The broad teaching of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification and the following claims. It should be understood that one or more steps within a method may be executed in a different order (or concurrently) without altering the principles of the present disclosure. Further, although each of

the embodiments is described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

APPARATUS

[0159] An apparatus of the present disclosure is configured for post-development treatment of a patterned metal-containing photoresist mask. The apparatus may be configured for other processing operations such as deposition, bevel and backside cleaning, post-application baking, EUV scanning, post-exposure baking, development, etching, and other operations. In some implementations, the apparatus is configured to perform multiple dry operations. In some implementations, the apparatus is configured to perform a combination of wet and dry operations. The apparatus may include a single wafer chamber or multiple stations in the same process chamber. With multiple stations in the same process chamber, various processing operations such as those described in the present disclosure may be performed in different stations in the same process chamber. In some embodiments, a process chamber for post-development treatment of the present disclosure may be performed in the same chamber as development, in the same chamber as pattern transfer etching, or in the same chamber as both development and pattern transfer etching.

[0160] The apparatus configured to post-development treatment includes a process chamber with a substrate support. The apparatus may include at least a reactive gas source in fluid communication with the process chamber. The apparatus may include one or more gas lines for delivery of one or more reactive gas species. In some embodiments, the one or more reactive gas species may include an organic gas species, an organometallic gas species, a metal-containing gas species, or combinations thereof. In some embodiments, the one or more reactive gas species may include an oxygen-containing gas, a carbon-containing gas, a hydrogen-containing gas, a nitrogen-containing gas, a halogen-containing gas, or combinations thereof. The one or more reactive gas species may be delivered to the process chamber via the one or more gas lines to treat a post-developed metal-containing photoresist mask. The apparatus may include one or more heating elements for temperature control. Such heating elements may be provided in the process chamber and/or in the substrate support. Alternatively, such heating elements may be provided outside the process chamber. In some implementations, the apparatus may include a plasma source for

generating plasma during treatment of the post-developed metal-containing photoresist mask. In some implementations, the one or more reactive species may selectively deposit a protective film on the post-developed metal-containing photoresist mask. The apparatus may further include one or more sensors for sensing particle count, wafer count, thickness count, or other parameters for triggering an endpoint of the post-development treatment.

[0161] **FIG. 6** depicts a schematic illustration of an example process station for maintaining an environment that is suitable for performing photoresist development, photoresist treatment, and/or combined etch operations according to some embodiments. For simplicity, the process station 600 is depicted as a standalone process station having a process chamber body 602 for maintaining a low-pressure environment. However, it will be appreciated that a plurality of process stations 600 may be included in a common process tool environment. Further, it will be appreciated that, in some embodiments, one or more hardware parameters of process station 600, including those discussed in detail below, may be adjusted programmatically by one or more computer controllers.

[0162] A plurality of process stations 600 may be included in a common low-pressure process tool environment. For example, **FIG. 7** depicts an implementation of a multi-station processing tool 700. In some implementations, one or more hardware parameters of the process tool 700 including those discussed in detail below may be adjusted programmatically by one or more computer controllers 750.

[0163] A process station may be configured as a module in a cluster tool. **FIG. 9** depicts a semiconductor process cluster tool architecture with vacuum-integrated deposition and patterning modules suitable for implementation of the implementations described herein. Such a cluster process tool architecture can include resist deposition, resist exposure (EUV scanner), resist development, resist rework, and etch modules, as described above and further below with reference to **FIGS. 6** and **7**.

[0164] Returning to **FIG. 6**, process station 600 fluidly communicates with reactant delivery system 601 for delivering process gases to a showerhead 606. Reactant delivery system 601 optionally includes a mixing vessel 604 for blending and/or conditioning process gases, for delivery to showerhead 606. One or more mixing vessel inlet valves 620 may control introduction of process gases to mixing vessel 604. Where plasma exposure is used, plasma may also be delivered to the showerhead 606 or may be generated in the process station 600. As noted above, in at least some implementations, non-plasma thermal exposure is favored.

[0165] **FIG. 6** includes an optional vaporization point 603 for vaporizing liquid reactant to be supplied to the mixing vessel 604. In some implementations, a liquid flow controller (LFC)

upstream of vaporization point 603 may be provided for controlling a mass flow of liquid for vaporization and delivery to process station 600. For example, the LFC may include a thermal mass flow meter (MFM) located downstream of the LFC. A plunger valve of the LFC may then be adjusted responsive to feedback control signals provided by a proportional-integral-derivative (PID) controller in electrical communication with the MFM.

[0166] Showerhead 606 distributes process gases toward substrate 612. In the implementation shown in **FIG. 6**, the substrate 612 is located beneath showerhead 606 and is shown resting on a pedestal 608. Showerhead 606 may have any suitable shape and may have any suitable number and arrangement of ports for distributing process gases to substrate 612.

[0167] In some implementations, pedestal 608 may be raised or lowered to expose substrate 612 to a volume 607 between the substrate 612 and the showerhead 606. It will be appreciated that, in some implementations, pedestal height may be adjusted programmatically by a suitable computer controller. In some implementations, the showerhead 606 may have multiple plenum volumes with multiple temperature controls.

[0168] In some implementations, pedestal 608 may be temperature controlled via heater 610. In some implementations, the pedestal 608 may be heated to a temperature of greater than 0°C and up to 300°C, for example 50°C to 280°C, such as about 100°C to 240°C, during post-development treatment, as described in disclosed implementations. In some implementations, the heater 610 of the pedestal 608 may include a plurality of independently controllable temperature control zones.

[0169] Further, in some implementations, pressure control for process station 600 may be provided by a butterfly valve 618. As shown in the implementation of **FIG. 6**, butterfly valve 618 throttles a vacuum provided by a downstream vacuum pump (not shown). However, in some implementations, pressure control of process station 600 may also be adjusted by varying a flow rate of one or more gases introduced to the process station 600.

[0170] In some implementations, a position of showerhead 606 may be adjusted relative to pedestal 608 to vary a volume between the substrate 612 and the showerhead 606. Further, it will be appreciated that a vertical position of pedestal 608 and/or showerhead 606 may be varied by any suitable mechanism within the scope of the present disclosure. In some implementations, pedestal 608 may include a rotational axis for rotating an orientation of substrate 612. It will be appreciated that, in some implementations, one or more of these example adjustments may be performed programmatically by one or more suitable computer controllers.

[0171] Where plasma may be used, for example in descumming, treatment, deposition, or smoothing operations, showerhead 606 and pedestal 608 electrically communicate with a radio frequency (RF) power supply 614 and matching network 616 for powering a plasma. In some implementations, the plasma energy may be controlled by controlling one or more of a process station pressure, a gas concentration, an RF source power, an RF source frequency, and a plasma power pulse timing. For example, RF power supply 614 and matching network 616 may be operated at any suitable power to form a plasma having a desired composition of radical species. Examples of suitable powers are up to about 1000 W.

[0172] In some implementations, instructions for a computer controller (not shown) may be provided via input/output control (IOC) sequencing instructions. In one example, the instructions for setting conditions for a process phase may be included in a corresponding recipe phase of a process recipe. In some cases, process recipe phases may be sequentially arranged, so that all instructions for a process phase are executed concurrently with that process phase. In some implementations, instructions for setting one or more reactor parameters may be included in a recipe phase. For example, a recipe phase may include instructions for setting a flow rate of an etch gas, such as a hydrogen halide, and time delay instructions for the recipe phase. In some implementations, the controller may include any of the features described below with respect to controller 750 of FIG. 7.

[0173] As described above, one or more process stations may be included in a multi-station processing tool. FIG. 7 shows a schematic view of an implementation of a multi-station processing tool 700 with an inbound load lock 702 and an outbound load lock 704, either or both of which may include a remote plasma source. A robot 706 at atmospheric pressure is configured to move wafers from a cassette loaded through a pod 708 into inbound load lock 702 via an atmospheric port 710. A wafer is placed by the robot 706 on a pedestal 712 in the inbound load lock 702, the atmospheric port 710 is closed, and the load lock is pumped down. Where the inbound load lock 702 includes a remote plasma source, the wafer may be exposed to a remote plasma treatment to treat the substrate surface in the load lock prior to being introduced into a processing chamber 714. Further, the wafer also may be heated in the inbound load lock 702 as well, for example, to remove moisture and adsorbed gases. Next, a chamber transport port 716 to processing chamber 714 is opened, and another robot (not shown) places the wafer into the reactor on a pedestal of a first station shown in the reactor for processing. While the implementation depicted in FIG. 7 includes load locks, it will be appreciated that, in some implementations, direct entry of a wafer into a process station may be provided.

[0174] The depicted processing chamber 714 includes four process stations, numbered from 1 to 4 in the implementation shown in **FIG. 7**. Each station has a heated pedestal (shown at 718 for station 1), and gas line inlets. It will be appreciated that in some implementations, each process station may have different or multiple purposes. For example, in some implementations, a process station may be switchable between development and etch process modes. Additionally or alternatively, in some implementations, processing chamber 714 may include one or more matched pairs of development and etch process stations. While the depicted processing chamber 714 includes four stations, it will be understood that a processing chamber according to the present disclosure may have any suitable number of stations. For example, in some implementations, a processing chamber may have five or more stations, while in other implementations a processing chamber may have three or fewer stations.

[0175] **FIG. 7** depicts an implementation of a wafer handling system 790 for transferring wafers within processing chamber 714. In some implementations, wafer handling system 790 may transfer wafers between various process stations and/or between a process station and a load lock. It will be appreciated that any suitable wafer handling system may be employed. Non-limiting examples include wafer carousels and wafer handling robots. **FIG. 7** also depicts an implementation of a controller 750 (e.g., system controller) employed to control process conditions and hardware states of process tool 700. Controller 750 may include one or more memory devices 756, one or more mass storage devices 754, and one or more processors 752. Processor 752 may include a CPU or computer, analog, and/or digital input/output connections, stepper motor controller boards, etc.

[0176] In some implementations, controller 750 controls all of the activities of process tool 700. Controller 750 executes system control software 758 stored in mass storage device 754, loaded into memory device 756, and executed on processor 752. Alternatively, the control logic may be hard coded in the controller 750. Applications Specific Integrated Circuits, Programmable Logic Devices (e.g., field-programmable gate arrays, or FPGAs) and the like may be used for these purposes. In the following discussion, wherever “software” or “code” is used, functionally comparable hard coded logic may be used in its place. System control software 758 may include instructions for controlling the timing, mixture of gases, gas flow rates, chamber and/or station pressure, chamber and/or station temperature, wafer temperature, target power levels, RF power levels, substrate pedestal, chuck and/or susceptor position, and other parameters of a particular process performed by process tool 700. System control software 758 may be configured in any suitable way. For example, various process tool component subroutines or control objects may be

written to control operation of the process tool components used to carry out various process tool processes. System control software 758 may be coded in any suitable computer readable programming language.

[0177] In some implementations, system control software 758 may include input/output control (IOC) sequencing instructions for controlling the various parameters described above. Other computer software and/or programs stored on mass storage device 754 and/or memory device 756 associated with controller 750 may be employed in some implementations. Examples of programs or sections of programs for this purpose include a substrate positioning program, a process gas control program, a pressure control program, a heater control program, and a plasma control program.

[0178] A substrate positioning program may include program code for process tool components that are used to load the substrate onto pedestal 718 and to control the spacing between the substrate and other parts of process tool 700.

[0179] A process gas control program may include code for controlling process gas composition and flow rates and optionally for flowing gas into one or more process stations prior to deposition in order to stabilize the pressure in the process station. A pressure control program may include code for controlling the pressure in the process station by regulating, for example, a throttle valve in the exhaust system of the process station, a gas flow into the process station, etc.

[0180] A heater control program may include code for controlling the current to a heating unit that is used to heat the substrate. Alternatively, the heater control program may control delivery of a heat transfer gas (such as helium) to the substrate.

[0181] A plasma control program may include code for setting RF power levels applied to the process electrodes in one or more process stations in accordance with the implementations herein.

[0182] A pressure control program may include code for maintaining the pressure in the reaction chamber in accordance with the implementations herein.

[0183] In some implementations, there may be a user interface associated with controller 750. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[0184] In some implementations, parameters adjusted by controller 750 may relate to process conditions. Non-limiting examples include process gas composition and flow rates, temperature, pressure, plasma conditions (such as RF bias power levels), etc. These parameters may be provided to the user in the form of a recipe, which may be entered utilizing the user interface.

[0185] Signals for monitoring the process may be provided by analog and/or digital input connections of controller 750 from various process tool sensors. The signals for controlling the process may be output on the analog and digital output connections of process tool 700. Non-limiting examples of process tool sensors that may be monitored include mass flow controllers, pressure sensors (such as manometers), thermocouples, etc. Appropriately programmed feedback and control algorithms may be used with data from these sensors to maintain process conditions.

[0186] Controller 750 may provide program instructions for implementing the above-described deposition processes. The program instructions may control a variety of process parameters, such as DC power level, RF bias power level, pressure, temperature, etc. The instructions may control the parameters to operate development, clean, and/or etch processes according to various implementations described herein.

[0187] The controller 750 will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with disclosed implementations. Machine-readable media containing instructions for controlling process operations in accordance with disclosed implementations may be coupled to the controller 750.

[0188] In some implementations, the controller 750 is part of a system, which may be part of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller 750, depending on the processing conditions and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, wafer transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0189] Broadly speaking, the controller 750 may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The

integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller 750 in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor wafer or to a system. The operational parameters may, in some implementations, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

[0190] The controller 750, in some implementations, may be a part of or coupled to a computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller 750 may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller 750 receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller 750 is configured to interface with or control. Thus as described above, the controller 750 may be distributed, such as by including one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0191] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor

deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an ALD chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, an EUV lithography chamber (scanner) or module, a development chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor wafers.

[0192] As noted above, depending on the process step or steps to be performed by the tool, the controller 750 might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

[0193] ICP reactors which, in certain implementations, may be suitable for etch operations suitable for implementation of some implementations, are now described. Although ICP reactors are described herein, in some implementations, it should be understood that capacitively coupled plasma reactors may also be used.

[0194] FIG. 8 schematically shows a cross-sectional view of an inductively coupled plasma apparatus 800 appropriate for implementing certain implementations or aspects of implementations such as dry development, post-development treatment, and/or etch. In other implementations, other tools or tool types having the functionality to conduct the dry development, post-development treatment, and/or etch processes described herein may be used for implementation.

[0195] The inductively coupled plasma apparatus 800 includes an overall process chamber 824 structurally defined by chamber walls 801 and a window 811. The chamber walls 801 may be fabricated from stainless steel, aluminum, or plastic. The window 811 may be fabricated from quartz or other dielectric material. An optional internal plasma grid 850 divides the overall process chamber into an upper sub-chamber 802 and a lower sub chamber 803. In most implementations, plasma grid 850 may be removed, thereby utilizing a chamber space made of sub chambers 802 and 803. A chuck 817 is positioned within the lower sub-chamber 803 near the bottom inner surface. The chuck 817 is configured to receive and hold a semiconductor wafer 819 upon which the etching and deposition processes are performed. The chuck 817 can be an electrostatic chuck for supporting the wafer 819 when present. In some implementations, an edge ring (not shown) surrounds chuck 817 and has an upper surface that is approximately planar with a top surface of the wafer 819, when present over chuck 817. The chuck 817 also includes electrostatic electrodes

for chucking and dechucking the wafer 819. A filter and DC clamp power supply (not shown) may be provided for this purpose. Other control systems for lifting the wafer 819 off the chuck 817 can also be provided. The chuck 817 can be electrically charged using an RF power supply 823. The RF power supply 823 is connected to matching circuitry 821 through a connection 827. The matching circuitry 821 is connected to the chuck 817 through a connection 825. In this manner, the RF power supply 823 is connected to the chuck 817. In various implementations, a bias power of the electrostatic chuck may be set at about 50 V or may be set at a different bias power depending on the process performed in accordance with disclosed implementations. For example, the bias power may be between about 20 V and about 100 V, or between about 30 V and about 150 V.

[0196] Elements for plasma generation include a coil 833 is positioned above window 811. In some implementations, a coil is not used in disclosed implementations. The coil 833 is fabricated from an electrically conductive material and includes at least one complete turn. The example of a coil 833 shown in **FIG. 8** includes three turns. The cross sections of coil 833 are shown with symbols, and coils having an “X” extend rotationally into the page, while coils having a “●” extend rotationally out of the page. Elements for plasma generation also include an RF power supply 841 configured to supply RF power to the coil 833. In general, the RF power supply 841 is connected to matching circuitry 839 through a connection 845. The matching circuitry 839 is connected to the coil 833 through a connection 843. In this manner, the RF power supply 841 is connected to the coil 833. An optional Faraday shield 849 is positioned between the coil 833 and the window 811. The Faraday shield 849 may be maintained in a spaced apart relationship relative to the coil 833. In some implementations, the Faraday shield 849 is disposed immediately above the window 811. In some implementations, the Faraday shield 849 is between the window 811 and the chuck 817. In some implementations, the Faraday shield 849 is not maintained in a spaced apart relationship relative to the coil 833. For example, the Faraday shield 849 may be directly below the window 811 without a gap. The coil 833, the Faraday shield 849, and the window 811 are each configured to be substantially parallel to one another. The Faraday shield 849 may prevent metal or other species from depositing on the window 811 of the process chamber 824.

[0197] Process gases may be flowed into the process chamber through one or more main gas flow inlets 860 positioned in the upper sub-chamber 802 and/or through one or more side gas flow inlets 870. Likewise, though not explicitly shown, similar gas flow inlets may be used to supply process gases to a capacitively coupled plasma processing chamber. A vacuum pump, e.g., a one or two stage mechanical dry pump and/or turbomolecular pump 840, may be used to draw process

gases out of the process chamber 824 and to maintain a pressure within the process chamber 824. For example, the vacuum pump may be used to evacuate the lower sub-chamber 803 during a purge operation. A valve-controlled conduit may be used to fluidically connect the vacuum pump to the process chamber 824 so as to selectively control application of the vacuum environment provided by the vacuum pump. This may be done employing a closed loop-controlled flow restriction device, such as a throttle valve (not shown) or a pendulum valve (not shown), during operational plasma processing. Likewise, a vacuum pump and valve controlled fluidic connection to the capacitively coupled plasma processing chamber may also be employed. The wide range of pressure to be modulated within a process chamber for combined dry development and etch may be achieved with variable-speed vacuum systems, throttle valves, by adjusting the flow of process gases, or by using two pressure regulating systems.

[0198] During operation of the apparatus 800, one or more process gases may be supplied through the gas flow inlets 860 and/or 870. In certain implementations, process gas may be supplied only through the main gas flow inlet 860, or only through the side gas flow inlet 870. In some cases, the gas flow inlets shown in the figure may be replaced by more complex gas flow inlets, one or more showerheads, for example. The Faraday shield 849 and/or optional grid 850 may include internal channels and holes that allow delivery of process gases to the process chamber 824. Either or both of Faraday shield 849 and optional grid 850 may serve as a showerhead for delivery of process gases. In some implementations, a liquid vaporization and delivery system may be situated upstream of the process chamber 824, such that once a liquid reactant or precursor is vaporized, the vaporized reactant or precursor is introduced into the process chamber 824 via a gas flow inlet 860 and/or 870.

[0199] Radio frequency power is supplied from the RF power supply 841 to the coil 833 to cause an RF current to flow through the coil 833. The RF current flowing through the coil 833 generates an electromagnetic field about the coil 833. The electromagnetic field generates an inductive current within the upper sub-chamber 802. The physical and chemical interactions of various generated ions and radicals with the wafer 819 etch features of and selectively deposit layers on the wafer 819.

[0200] If the plasma grid 850 is used such that there is both an upper sub-chamber 802 and a lower sub-chamber 803, the inductive current acts on the gas present in the upper sub-chamber 802 to generate an electron-ion plasma in the upper sub-chamber 802. The optional internal plasma grid 850 limits the amount of hot electrons in the lower sub-chamber 803. In some

implementations, the apparatus 800 is designed and operated such that the plasma present in the lower sub-chamber 803 is an ion-ion plasma.

[0201] Both the upper electron-ion plasma and the lower ion-ion plasma may contain positive and negative ions, though the ion-ion plasma will have a greater ratio of negative ions to positive ions. Volatile etching and/or deposition byproducts may be removed from the lower sub-chamber 803 through port 822. The chuck 817 disclosed herein may operate at elevated temperatures ranging between about 10°C and about 250°C. The temperature will depend on the process operation and specific recipe.

[0202] Apparatus 800 may be coupled to facilities (not shown) when installed in a clean room or a fabrication facility. Facilities include plumbing that provide processing gases, vacuum, temperature control, and environmental particle control. These facilities are coupled to apparatus 800, when installed in the target fabrication facility. Additionally, apparatus 800 may be coupled to a transfer chamber that allows robotics to transfer semiconductor wafers into and out of apparatus 800 using typical automation.

[0203] In some implementations, a controller 830 (which may include one or more physical or logical controllers) controls some or all of the operations of a process chamber 824. The controller 830 may include one or more memory devices and one or more processors. In some implementations, the apparatus 800 includes a switching system for controlling flow rates and durations when disclosed implementations are performed. In some implementations, the apparatus 800 may have a switching time of up to about 500 ms, or up to about 750 ms. Switching time may depend on the flow chemistry, recipe chosen, reactor architecture, and other factors.

[0204] In some implementations, the controller 830 is part of a system, which may be part of the above-described examples. Various aspects of the controller 830 are described above.

[0205] EUVL patterning may be conducted using any suitable tool, often referred to as a scanner. The EUVL patterning tool may be a standalone device from which the substrate is moved into and out of for deposition and etching as described herein. Alternatively, as described below, the EUVL patterning tool may be a module on a larger multi-component tool.

[0206] FIG. 9 depicts a semiconductor process cluster tool architecture 900 with vacuum-integrated deposition, patterning, and treatment modules that interface with a vacuum transfer module, suitable for implementations of processes described herein. The arrangement of transfer modules to “transfer” wafers among multiple storage facilities and processing modules may be referred to as a “cluster tool architecture” system. Deposition, patterning, and treatment modules

are vacuum-integrated, in accordance with the requirements of a particular process. Other modules, such as for etch, may also be included on the cluster.

[0207] A vacuum transport module (VTM) 938 interfaces with four processing modules 920a–920d, which may be individually optimized to perform various fabrication processes. By way of example, processing modules 920a–920d may be implemented to perform deposition, evaporation, ELD, dry development, clean, etch, treatment, strip, and/or other semiconductor processes. For example, module 920a may be an ALD reactor that may be operated to perform in a non-plasma, thermal atomic layer depositions as described herein. Module 920b may be a PECVD tool. It should be understood that the figure is not necessarily drawn to scale.

[0208] Airlocks 942 and 946, also known as a loadlocks or transfer modules, interface with the VTM 938 and a patterning module 940. This tool architecture allows for work pieces, such as semiconductor substrates or wafers, to be transferred under vacuum so as not to react before exposure. Integration of the deposition modules with the lithography tool is facilitated by the fact that EUVL also requires a greatly reduced pressure given the strong optical absorption of the incident photons by ambient gases such as H₂O, O₂, etc.

[0209] As noted above, this integrated architecture is just one possible implementation of a tool for implementation of the described processes. The processes may also be implemented with a more conventional stand-alone EUVL scanner and a deposition reactor, either standalone or integrated in a cluster architecture with other tools, such as etch, strip etc. as modules, for example as described with reference to **FIG. 9** but without the integrated patterning module.

[0210] Airlock 942 may be an “outgoing” loadlock, referring to the transfer of a substrate out from the VTM 938 serving a deposition module 920a to the patterning module 940, and airlock 946 may be an “ingoing” loadlock, referring to the transfer of a substrate from the patterning module 940 back in to the VTM 938. The ingoing airlock 946 may also provide an interface to the exterior of the tool for access and egress of substrates. Each process module has a facet that interfaces the module to VTM 938. For example, deposition process module 920a has facet 936. Inside each facet, sensors, for example, sensors 1–18 as shown, are used to detect the passing of wafer 926 when moved between respective stations. Patterning module 940 and airlocks 942 and 946 may be similarly equipped with additional facets and sensors, not shown.

[0211] Main VTM robot 922 transfers wafer 926 between modules, including airlocks 942 and 946. In one implementation, robot 922 has one arm, and in another implementation, robot 922 has two arms, where each arm has an end effector 924 to pick wafers such as wafer 926 for transport. Front-end robot 944, in is used to transfer wafers 926 from outgoing airlock 942 into the patterning module 940, from the patterning module 940 into ingoing airlock 946. Front-end robot 944 may also transport wafers 926 between the ingoing loadlock and the exterior of the tool for access and egress of substrates. Because ingoing airlock module 946 has the ability to match the environment between atmospheric and vacuum, the wafer 926 is able to move between the two pressure environments without being damaged.

[0212] It should be noted that an EUVL tool typically operates at a higher vacuum than a deposition tool. If this is the case, it is desirable to increase the vacuum environment of the substrate during the transfer between the deposition to the EUVL tool to allow the substrate to degas prior to entry into the patterning tool. Outgoing airlock 942 may provide this function by holding the transferred wafers at a lower pressure, no higher than the pressure in the patterning module 940, for a period of time and exhausting any off-gassing, so that the optics of the patterning module 940 are not contaminated by off-gassing from the substrate. A suitable pressure for the outgoing, off-gassing airlock is no more than 1E-8 Torr.

[0213] In some implementations, a controller 950 (which may include one or more physical or logical controllers) controls some or all of the operations of the cluster tool and/or its separate modules. It should be noted that the controller can be local to the cluster architecture or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. The controller 950 may include one or more memory devices and one or more processors. The processor may include a central processing unit (CPU) or computer, analog and/or digital input/output connections, stepper motor controller boards, and other like components. Instructions for implementing appropriate control operations are executed on the processor. These instructions may be stored on the memory devices associated with the controller or they may be provided over a network. In certain implementations, the system controller executes system control software.

[0214] The system control software may include instructions for controlling the timing of application and/or magnitude of any aspect of tool or module operation. System control software may be configured in any suitable way. For example, various process tool component subroutines or control objects may be written to control operations of the process tool components necessary

to carry out various process tool processes. System control software may be coded in any suitable compute readable programming language. In some implementations, system control software includes input/output control (IOC) sequencing instructions for controlling the various parameters described above. For example, each phase of a semiconductor fabrication process may include one or more instructions for execution by the controller. The instructions for setting process conditions for condensation, deposition, evaporation, patterning and/or etching phase may be included in a corresponding recipe phase, for example.

[0215] In various implementations, an apparatus for post-development treatment is provided. The apparatus may include a processing chamber for patterning, treatment, deposition, and etch, and a controller including instructions for post-development treatment of a patterned photoresist mask. The instructions may include code for, in the processing chamber, treating a patterned metal-containing photoresist mask after development. Such treatment may include thermal treatment, plasma treatment, chemical treatment, or selective deposition of a protective layer on the patterned metal-containing photoresist mask.

[0216] It should be noted that the computer controlling the wafer movement can be local to the cluster architecture or can be located external to the cluster architecture in the manufacturing floor, or in a remote location and connected to the cluster architecture via a network. A controller as described above with respect to any of **FIGS. 6, 7, or 8** may be implemented with the tool in **FIG. 9**.

FURTHER IMPLEMENTATIONS

[0217] The apparatus and processes described herein may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels, and the like. Typically, though not necessarily, such apparatus and processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically comprises some or all of the following steps, each step enabled with a number of possible tools: (1) application of photoresist on a work piece, i.e., a substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or work piece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

CONCLUSION

[0218] In the foregoing description, numerous specific details are set forth to provide a thorough understanding of the presented embodiments. The disclosed embodiments may be practiced without some or all of these specific details. In other instances, well-known process operations have not been described in detail to not unnecessarily obscure the disclosed embodiments. While the disclosed embodiments are described in conjunction with the specific embodiments, it will be understood that it is not intended to limit the disclosed embodiments.

[0219] Although the foregoing embodiments have been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing the processes, systems, and apparatus of the present embodiments. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the embodiments are not to be limited to the details given herein.

[0220] The following claims are provided for further illustration of certain embodiments of the disclosure. The disclosure is not necessarily limited to these embodiments.

CLAIMS

What is claimed is:

1. An apparatus for integrating dry development and etch semiconductor processes in a single process chamber comprising:
 - one or more process chambers;
 - one or more pressure regulating devices;
 - one or more pumps fluidly coupled with the pressure regulating device;
 - a plasma processing system;
 - one or more gas inlets into the process chambers and associated flow-control hardware; and
 - a controller having at least one processor and a memory, wherein
 - the at least one processor and the memory are communicatively connected with one another,
 - the at least one processor is at least operatively connected with the associated flow-control hardware, and the memory stores computer-executable instructions for controlling the at least one processor to at least control the associated flow-control hardware to:
 - perform thermal dry development at a first pressure in a process chamber;
 - perform plasma dry development and etching at a second pressure lower than the first pressure in the same process chamber;
 - transition pressure in the same process chamber from the first pressure to the second pressure in ten seconds or less; and
 - maintain one or more process parameters uniformly.
2. The apparatus of claim 1, wherein the one or more pressure regulating devices comprises a pressure control valve assembly.

3. The apparatus of claim 2, wherein the pressure control valve assembly comprises a throttle valve.
4. The apparatus of claim 1, wherein the one or more pumps comprises a roughing pump and a turbo pump.
5. The apparatus of claim 4, wherein the first pressure is from five to one fifty times higher than the second pressure.
6. The apparatus of claim 1, wherein the one or more process parameters comprises pumping, gas delivery or pumping and gas delivery.
7. An apparatus for processing a metal-containing photoresist comprising:
 - one or more process chambers;
 - one or more pressure regulating devices;
 - one or more pumps fluidly coupled with the pressure regulating device;
 - one or more gas inlets into the process chambers and associated flow-control hardware;
 - a plasma processing system; and
 - a controller having at least one processor and a memory, wherein
 - the at least one processor and the memory are communicatively connected with one another,
 - the at least one processor is at least operatively connected with the associated flow-control hardware, and the memory stores computer-executable instructions for controlling the at least one processor to at least control the associated flow-control hardware to:
 - perform thermal dry development at a first pressure in a process chamber;
 - perform plasma dry development and etching at a second pressure lower than the first pressure in the same process chamber;

modulate pressure in the same process chamber from the first pressure to the second pressure in ten seconds or less;

return pressure in the same process chamber from the second pressure back to the first pressure after plasma dry development and etching in twenty seconds or less; and

maintain one or more process parameters uniformly.

8. The apparatus of claim 7, wherein the plasma processing system comprises a radiofrequency power amplifier.

9. The apparatus of claim 8, wherein the radiofrequency power amplifier is operated continuously or pulsed.

10. A method for processing a semiconductor substrate comprising:

providing a patterned photoresist on a semiconductor substrate in a process chamber;

thermally dry developing the patterned photoresist with a process gas at a first pressure to form a thermally dry developed patterned resist; and

plasma dry developing and etching the thermally dry developed patterned resist with an etchant at a second pressure to form a patterned substrate;

wherein thermally dry developing, plasma dry developing and etching occur in the same process chamber;

wherein the process chamber is transitioned before etching from the first pressure to the second pressure in ten seconds or less and returned to the first pressure after etching in twenty seconds or less; and

wherein the patterned photoresist is a metal-containing photoresist.

11. The method of claim 10, wherein the first pressure is from about 200 to 500 mTorr and the second pressure is from about 20 to 50 mTorr.

12. The method of claim 10, wherein the metal-containing photoresist comprises a photopatterned EUV-sensitive organo-metal oxide, a photopatterned EUV-sensitive metal oxide or an organo-metal containing thin film EUV resist.
13. The method of claim 12, wherein the photopatterned EUV-sensitive metal oxide comprises tin oxide.
14. The method of claim 13, whereby tin outgassing from the tin oxide is mitigated.
15. The method of claim 10, further comprising selective metal deposition.
16. The method of claim 10, wherein the etching comprises exposure to an etchant plasma.
17. The method of claim 16, wherein the etchant plasma comprises a hardmask opening gas.
18. The method of claim 17, wherein the hardmask opening gas comprises carbonyl sulfide, oxygen, carbon dioxide, nitrogen, hydrogen or a combination thereof.
19. The method of claim 18, wherein the hardmask opening gas comprises oxygen plasma.
20. The method of claim 19, wherein the exposure to oxygen plasma is for a duration of from about 0.5 to about 4 seconds.