



CLAIMS

1. (Amended) A semiconductor device comprising:
a plurality of sense amplifiers for amplifying signals,
which are read out of a plurality of memory cells onto a
plurality of data lines, to a first voltage on said plurality
5 of data lines;
a first wiring line commonly connected to power supply
nodes of said plurality of sense amplifiers;
a first switch for supplying the first voltage from
one end of said first wiring line;
10 a second wiring line disposed along said plurality
of sense amplifiers for supplying a second voltage which
is higher than the first voltage; and
a plurality of second switches disposed with
distributing along said plurality of sense amplifiers
15 between said first wiring line and said second wiring line.
2. A semiconductor device according to claim 1,
wherein said second wiring line is formed in a meshed
power line structure.
3. A semiconductor device according to claim 1,
wherein, for activation of said plurality of sense
amplifiers, said first switch is turned ON after said
plurality of second switches are turned ON for a
5 predetermined period of time.
4. (Amended) A semiconductor device having a memory array
including a plurality of sub-memory arrays comprising:



each of said plurality of sub-memory arrays including;

5 a plurality of memory cells disposed at respective intersection points of a plurality of word lines extending in a first direction and a plurality of data lines extending in a second direction;

 a plurality of sense amplifiers disposed
10 respectively in correspondence with said plurality of data lines, each of said plurality of sense amplifiers having a first MISFET pair of a first conduction type arranged in a cross-coupled form and a second MISFET pair of a second conduction type arranged in a cross-coupled
15 form;

 a first common source line extending to the first direction, said first common source line being coupled with sources of the first MISFET pair included in each of said plurality of sense amplifiers;

20 a second common source line extending to said first direction, said second common source line being coupled with sources of the second MISFET pair included in each of said plurality of sense amplifiers;

 a first power line extending to the first
25 direction, said first power line being supplied with a first potential;

 a second power line extending to the first direction, said second power line being supplied with a second potential;

30 a third power line arranged to be supplied with



a third potential;

a plurality of first switches disposed for a predetermined number of said plurality of sense amplifiers and disposed along said plurality of sense amplifiers between
35 said first common source line and said first power line;

a plurality of second switches disposed for a predetermined number of said plurality of sense amplifiers and disposed along said plurality of sense amplifiers between
said second common source line and said second power line;
40 and

a third switch coupling said first common source line with said third power line;

wherein the third potential is between the first potential and the second potential, and

45 wherein a signal read out of said memory cell is amplified to one of the second potential and the third potential on a corresponding one of said plurality of data lines.

5. A semiconductor device according to claim 4,
wherein, after one of said plurality of word lines is selected for reading out information from said memory cell onto a corresponding one of said plurality of data lines,
5 said plurality of first switches and said plurality of second switches are turned ON, and then after a lapse of a predetermined period of time, said plurality of first switches are turned ON, and said third switch is turned ON.

6. A semiconductor device according to claim 5,



wherein each of said plurality of first switches is a third MISFET of a first conduction type, each of said plurality of second switches is a fourth MISFET of a second conduction type, the first conduction type is a P type, the
5 second conduction type is an N type, the first potential is higher than the third potential, and the third potential is higher than the second potential.

7. A semiconductor device according to claim 4, wherein each of said plurality of sub-memory arrays has:

a first area formed in a square shape having
5 first and second sides meeting each other at a corner common thereto, said first area having said plurality of word lines, said plurality of data lines, and said plurality of memory cells;

a second area formed along said first side of
10 said first area, said second area having said plurality of sense amplifiers, said first and second common source lines, said first and second power lines, and said plurality of first and second switches;

a third area formed along said second side of
15 said first area, said third area having a plurality of connection parts for making connections between a plurality of word drivers disposed respectively in correspondence with said plurality of word lines or each of said plurality of word lines and said plurality of word lines arranged in
20 an upper layer; and



a fourth area enclosed by a corner of said first area, a side of said second area, and a side of said third area, a fourth area being disposed said third switch.

8. (Amended) A semiconductor device according to claim 4, wherein each of said plurality of sub-memory arrays includes:

5 a plurality of fourth power lines extending in the second direction and connected to said first power line at respective intersection points of said plurality of fourth power lines and said first power lines for supplying with the first potential; and

10 a plurality of fifth power lines extending in the second direction and connected to said second power line at respective intersection points of said plurality of fifth power lines and said second power lines for supplying with the second potential.

9. (Amended) A semiconductor device according to claim 8, wherein each of said plurality of fourth power lines and each of said plurality of fifth power lines are provided for a predetermined number of said plurality of sense
5 amplifiers.

10. A semiconductor device according to claim 4, wherein each of said plurality of memory cells is a dynamic memory cell having one MISFET and one capacitor.



11. (Amended) A semiconductor device having a memory array including a plurality of sub-memory arrays comprising:
each of said plurality of sub-memory arrays including;

5 a plurality of memory cells disposed at respective intersection points of a plurality of word lines extending in a first direction and a plurality of data lines extending in a second direction;

10 a plurality of sense amplifiers disposed respectively in correspondence with said plurality of data lines, each of said plurality of sense amplifiers having a first MISFET pair of a first conduction type arranged in a cross-coupled form and a second MISFET pair of a second conduction type arranged in a cross-coupled form;

15 a first common source line extending to the first direction, said first common source line being coupled with sources of the first MISFET pair included in each of said plurality of sense amplifiers;

20 a second common source line extending to the first direction, said second common source line being coupled with said sources of the second MISFET pair included in each of said plurality of sense amplifiers;

25 a first power line extending to the first direction, said first power line being supplied with a first potential;

a second power line extending to the first direction, said second power line being supplied with a second potential;



30 a third power line arranged to be supplied with
a third potential;

a fourth power line arranged to be supplied
with a fourth potential;

a plurality of first switches disposed for a
predetermined number of said plurality of sense amplifiers
35 and coupled said first common source line with said first
power line;

a plurality of second switches disposed for a
predetermined number of said plurality of sense amplifiers
and coupled said second common source line with said second
40 power line;

a third switch coupled said first common source
line with said third power line; and

a fourth switch coupled said second common
source line with said fourth power line;

45 wherein said third and fourth potentials are between
the first potential and the second potential, and

wherein a signal read out of said memory cell is
amplified to one of the third potential and the fourth
potential on a corresponding one of said plurality of data
50 lines.

12. A semiconductor device according to claim 11,
wherein each of said plurality of sub-memory arrays
includes:

a first area formed in a square shape having
5 first and second sides meeting each other at a corner common



thereto, said first area provided said plurality of word lines, said plurality of data lines, and said plurality of memory cells;

10 a second area formed along the first side of said first area, said second area having said plurality of sense amplifiers, said first and second common source lines, said first and second power lines, and said plurality of first and second switches;

15 a third area formed along the second side of said first area, said third area having a plurality of connection parts for making connections between a plurality of word drivers disposed respectively in correspondence with said plurality of word lines or each of said plurality of word lines and said plurality of word lines arranged in
20 an upper layer; and

a fourth area enclosed by a corner of said first area, a side of said second area, and a side of said third area, said fourth area having said third and fourth switches.

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13. A semiconductor device according to claim 12, wherein, after one of said plurality of word lines is selected for reading out information from said memory cell onto a corresponding one of said plurality of data
5 lines, said plurality of first switches and said plurality of second switches are turned ON, and then after a lapse of a predetermined period of time, said plurality of first switches and said plurality of second switches are turned



OFF, and said third and fourth switches are turned ON.

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14. A semiconductor device according to claim 11,
wherein each of said plurality of first switches is
a third MISFET of a first conduction type, each of said
plurality of second switches is a fourth MISFET of a second
5 conduction type, said third switch is a fifth MISFET of the
first conduction type, said fourth switch is a sixth MISFET
of the second conduction type, the first conduction type
is a P type, the second conduction type is an N type, the
first potential is higher than the third potential, the
10 third potential is higher than the fourth potential, and
the fourth potential is higher than the second potential.

15. A semiconductor device according to claim 11,
wherein said third and fourth power lines are
extending to the first direction along said first and second
power lines,

5 wherein said third switch is divided a plurality of
third unit switches, said plurality of third unit switches
being provided for a predetermined number of said plurality
of sense amplifiers, and

wherein said fourth switch is divided a plurality of
10 fourth unit switches, said plurality of fourth switches
being provided for a predetermined number of said plurality
of sense amplifiers.

16. A semiconductor device according to claim 15,



wherein each of said plurality of sub-memory arrays includes:

5 a first area formed in a square shape having first and second sides meeting each other at a corner common thereto, said first area having said plurality of word lines, said plurality of data lines, and said plurality of memory cells;

10 a second area formed along said first side of said first area, said second area having said plurality of sense amplifiers, said first and second common source lines, said first, second, third and fourth power lines, said plurality of first and second switches, and said third and fourth switches; and

15 a third area formed along said second side of said first area, said third area having a plurality of connection parts for making connections between a plurality of word drivers disposed respectively in correspondence with said plurality of word lines or each of said plurality of word lines and said plurality of word lines arranged in
20 an upper layer.

17. A semiconductor device according to claim 16, wherein, after one of said plurality of word lines is selected for reading out information from said memory cell onto a corresponding one of said plurality of data
5 lines, said plurality of first switches and said plurality of second switches are turned ON, and then after a lapse of a predetermined period of time, said plurality of first



switches and said plurality of second switches are turned OFF, and said third and fourth switch are turned ON.

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18. A semiconductor device according to claim 15,
wherein each of said plurality of first switches is
a third MISFET of a first conduction type, each of said
plurality of second switches is a fourth MISFET of a second
5 conduction type, each of said plurality of third unit
switches is a fifth MISFET of the first conduction type,
each of said plurality of fourth unit switches is a sixth
MISFET of the second conduction type, the first conduction
type is a P type, the second conduction type is an N type,
10 the first potential is higher than the third potential, the
third potential is higher than the fourth potential, and
the fourth potential is higher than the second potential.

19. (Amended) A semiconductor device comprising:
a plurality of sense amplifiers for amplifying
signals read out of a plurality of memory cells onto a
plurality of data lines;
5 a plurality of first MISFETs so arranged that a first
potential associated with a high level of an amplification
signal for said plurality of sense amplifiers is supplied
from a first meshed power line structure, each of said
plurality of first MISFETs being disposed for a
10 predetermined number of said plurality of sense amplifiers;
and
a plurality of second MISFETs so arranged that a



second potential associated with a low level of an
amplification signal for said plurality of sense amplifiers
15 is supplied from a second meshed power line structure, each
of said plurality of second MISFETs being disposed for a
predetermined number of said plurality of sense amplifiers;

wherein said plurality of first and second MISFETs
are of the same conduction type, and each gate of said first
20 and second MISFETs is connected to a common drive control
signal line;

said drive control line transmits a signal for
controlling the conduction state of said plurality of said
first and second MISFETs; and

25 an absolute value of the difference between an
effective level and an ineffective level is larger than an
absolute value of the difference between said first potential
and said second potential.

20. A semiconductor device according to claim 19,
wherein said plurality of first and second MISFETs
are arranged alternately on a virtual line extending in one
direction along said plurality of sense amplifiers, and

5 wherein said drive control signal line is formed
along said virtual line and used to provide a gate electrode
for said plurality of first and second MISFETs.

21. (Amended) A semiconductor device having a memory
array including a plurality of sub-memory arrays comprising:

each of said plurality of sub-memory arrays
includes;



5 a plurality of memory cells disposed at
respective intersection points of a plurality of word lines
extending in a first direction and a plurality of data lines
extending in a second direction;

 a plurality of sense amplifiers disposed
10 respectively in correspondence with a plurality of said
data lines, each of said plurality of sense amplifiers
including a first MISFET pair of a first conduction type
arranged in a cross-coupled form and a second MISFET pair
of a second conduction type arranged in a cross-coupled
15 form;

 a first common source line extending to the
first direction, said first common source line being
coupled with sources of the first MISFET pair included in
each of said plurality of sense amplifiers;

20 a second common source line extending to the
first direction, said second common sources line being
coupled with sources of the second MISFET pair included in
each of said plurality of sense amplifiers;

 a first power line extending to the first
25 direction, said first power line being supplied with a first
potential;

 a second power line extending to the first
direction, said second power line being supplied with a
second potential;

30 a plurality of third MISFETs of the second
conduction type disposed for a predetermined number of said
plurality of sense amplifiers, a source-drain path of said



plurality of third MISFETs connected between said first common source line and said first power line;

35 a plurality of fourth MISFETs of the second conduction type disposed for a predetermined number of said plurality of sense amplifiers, a source-drain path of said plurality of fourth MISFETs being coupled said second source line with said second power line; and

40 a first drive control line extending to the first direction, said first drive control line being connected to gates of said plurality of third and fourth MISFETs in common; and

 wherein the first MISFET pair included in each
45 of said plurality of sense amplifiers is disposed along a first virtual line extending to the first direction;

 wherein the second MISFET pair included in each of said plurality of sense amplifiers is disposed along a second virtual line extending to the first direction; and

50 wherein said plurality of third and fourth MISFETs are disposed along a third virtual line extending to the first direction between said first and second virtual lines.

22. (Cancelled)

23. (Amended) A semiconductor device according to claim 21,

 wherein said plurality of third and fourth MISFETs are arranged alternately on said third virtual line.



24. A semiconductor device according to claim 21,
wherein each of said plurality of sub-memory arrays
has:

5 a first area formed in a square shape having
first and second sides meeting each other at a corner common
thereto, said first area having said plurality of word lines,
said plurality of data lines, and said plurality of memory
cells;

10 a second area formed along said first side of
said first area, said second area having said plurality of
sense amplifiers, said first and second common source lines,
said first and second power lines, and said plurality of
third and fourth MISFETs;

15 a third area formed along said second side of
said first area, said third area having a plurality of
connection parts for making connections between a plurality
of word drivers disposed respectively in correspondence
with said plurality of word lines or each of said plurality
of word lines and said plurality of word lines arranged in
20 an upper layer; and

a fourth area enclosed by a corner of said first
area, a side of said second area, and a side of said third
area, said fourth area having a precharge circuit connected
to each end of said first and second common source lines.

25. A semiconductor device according to claim 21,
wherein a signal read out from a memory cell onto said
plurality of data lines is amplified to one of said first



potential and said second potential, and

- 5 wherein, for activation of a plurality of said sense amplifiers, there is provided a period of time that a voltage larger than a voltage between the first potential and the second potential is applied to said first drive control line.