CLAIMS

What is claimed is:

1. A memory device, comprising:

a plurality of first access lines extending in a first direction;

a plurality of second access lines extending in a second direction different from the first direction;

a first plurality of memory cells comprising a self-selecting material, the first plurality of memory cells in contact with a first access line of the plurality of second access lines;

a second plurality of memory cells comprising the self-selecting memory, the second plurality of memory cells in contact with a second access line of the plurality of second access lines; and

a dielectric material between the first plurality of memory cells and the second plurality of memory cells, the first plurality of memory cells and the second plurality of memory cells being positioned between the first access line and the second access line.

2. The memory device of claim 1, further comprising:

a plug in contact with a second end of the first access line of the plurality of second access lines; and

a plug in contact with a second end of the second access line of the plurality of second access lines, wherein the first access line is electrically isolated from the second access line.

3. The memory device of claim 2, further comprising:

a plug in contact with a first end of the first access line of the plurality of second access lines; and

a plug in contact with a first end of the second access line of the plurality of second access lines.

4. The memory device of claim 1, wherein the plurality of second access lines are shunted in at least one direction.

5. The memory device of claim 1, further comprising:

a second dielectric material between a first memory cell of the first plurality of memory cells and a second memory cell of the first plurality of memory cells.

6. The memory device of claim 5, wherein the dielectric material and the second dielectric material are a same material.

7. A method of forming a memory device, comprising:

forming a stack comprising a first dielectric material, a second dielectric material, and a third dielectric material;

removing material in a first direction to form a first plurality of lines in the first dielectric material, the second dielectric material, and the third dielectric material;

removing material in a second direction to form a second plurality of lines in the first dielectric material;

forming a plurality of first access lines in contact with the first dielectric material;

depositing a self-selecting material to form a plurality of memory cells in contact with at least a part of a plurality of second access lines, the plurality of second access lines in contact with the self-selecting memory.

8. The method of claim 7, further comprising:

forming a plurality of plugs, a first end of each of the plurality of plugs in contact with a second end of each of the plurality of second access lines; and

removing at least a portion of the plurality of second access lines in the first direction.

9. The method of claim 8, further comprising:

forming a second plurality of plugs, a first end of each of the second plurality of plugs in contact with a first end of each of the plurality of second access lines.

10. The method of claim 7, wherein at least one of the first plurality of lines comprises a width that is greater than another line of the first plurality of lines.

11. The method of claim 10, the first dielectric material and the second dielectric material are a same material.

12. The method of claim 7, wherein the self-selecting memory comprises chalcogenide.

13. A memory device, comprising:

a first vertical access line comprising a first side and a second side opposite the first side;

a first memory cell comprising a first self-selecting material, the first memory cell coupled with the first side;

a dielectric material between with the first memory cell and a second memory cell, wherein the second memory cell comprises a second self-selecting memory and is coupled with a second side of a second vertical access line that is opposite the first side of the first vertical access line.

14. The memory device of claim 13, further comprising:

a first horizontal access line coupled with the dielectric material and the first memory cell; and

a second horizontal access line coupled with the dielectric material and the second memory cell, the first horizontal access line in communication with the first vertical access line and the second horizontal access line in communication with the second vertical access line.

15. The memory device of claim 13, wherein the first vertical access line is electrically isolated from the second vertical access line.

16. The memory device of claim 15, further comprising:

a sealing material in contact with a second end of the first vertical access line and the second vertical access line, wherein the first vertical access line and the second vertical access line are isolated from each other based at least in part on the sealing material.

17. The memory device of claim 13, wherein the memory device comprises a plurality of first discrete self-selecting memory segments and a plurality of second discrete self-selecting memory segments, the plurality of first discrete segments including the first self-selecting memory and the plurality of second discrete segments including the second self-

selecting memory, and wherein the first memory cell includes one of the plurality of first discrete segments and the second memory cell includes one of the plurality of second discrete segments.

18. The memory device of claim 13, wherein each of the first self-selecting memory and the second self-selecting memory are continuous along a first plurality of memory cells coupled with the first side of the first vertical access line and along a second plurality of memory cells coupled with the second side of the second vertical access line, wherein each of the first plurality of memory cells and the second plurality of memory cells comprise chalcogenide.

19. A memory device, comprising:

a first plurality of memory cells and a second plurality of memory cells positioned between a first side of a first vertical access line of a plurality of vertical access lines and a second side of a second vertical access line of the plurality of vertical access lines, each of the memory cells comprising a discrete self-selecting material segment;

a dielectric material between the first plurality of memory cells and the second plurality of memory cells, wherein the first plurality of memory cells are coupled with the first vertical access line and the second plurality of memory cells are coupled with the second vertical access line.

20. The memory device of claim 19, further comprising:

a first plurality of horizontal access lines coupled with each of the first plurality of memory cells; and

a second plurality of horizontal access lines coupled with each of the second plurality of memory cells.

21. The memory device of claim 20, further comprising:

a first plurality of plugs in contact with a first end of each of the plurality of vertical access lines; and

a second plurality of plugs in contact with a second end of each of the plurality of vertical access lines, wherein at least the first vertical access line of the plurality of vertical access lines is electrically isolated from the second vertical access line of the plurality of vertical access lines.

22. The memory device of claim 21, further comprising:

a second dielectric material in contact with the first vertical access line and the second vertical access line, the second dielectric material different than the dielectric material.

23. The memory device of claim 22, wherein the dielectric material and the second dielectric material are different materials.

24. The memory device of claim 22, wherein the second dielectric material is in contact with the dielectric material in at least a first direction.

25. The memory device of claim 19, wherein a width of the dielectric material is greater than a width of at least one of the plurality of vertical access lines.

26. The memory device of claim 19, wherein each of the discrete self-selecting memory segments comprises chalcogenide.

27. The memory device of claim 19, wherein the first vertical access line is coupled with the second vertical access line.

28. A method of forming a memory device, comprising:

forming a stack comprising a first dielectric material, a second dielectric material, and a third dielectric material;

removing material in a first direction to form a first plurality of lines in the first dielectric material, the second dielectric material, and the third dielectric material;

removing material in a second direction to form a second plurality of lines in the first dielectric material;

forming a plurality of first access lines coupled with the first dielectric material;

forming a plurality of discrete self-selecting material segments coupled with the plurality of first access lines; and

forming a plurality of second access lines that are coupled with each of the plurality of discrete self-selecting memory segments, each of the plurality of discrete self-selecting memory segments positioned between a first side of a first access line of the plurality of

second access lines and a second side of a second access line of the plurality of second access lines.

29. The method of claim 28, further comprising:

forming a first plurality of plugs and a second plurality of plugs, each of the first plurality of plugs in contact with a first end of each of the plurality of second access lines, and each of the second plurality of plugs in contact with a second end of each of the plurality of second access lines; and

removing a portion of the plurality of second access lines in the first direction.

30. The method of claim 28, wherein each of the plurality of discrete self-selecting memory segments are formed adjacent to the first plurality of lines.

31. The method of claim 28, wherein a width of the first dielectric material, after removing the material in the second direction, is greater than a width of at least one of the plurality of second access lines.

32. The method of claim 30, wherein each of the first dielectric material, the second dielectric material, and the third dielectric material comprise a different material.

33. The method of claim 28, wherein at least some of the plurality of discrete self-selecting memory segments comprise chalcogenide.