BATTERY OPERATED COMPUTER POWER MANAGEMENT SYSTEM

DESCRIPTION

This invention relates to the field of data processing and, more particularly, to a battery operated computer having a battery power management system.

RELATED APPLICATIONS

Attention is directed to the following related European patent applications filed concurrently herewith and claiming priority respectively from:

(1) US Patent Application Serial No. 647120 filed in the US on 25 January 1991.

(2) US Patent Application Serial No. 646304 filed in the US on 25 January 1991.

(3) US Patent Application Serial No. 646138 filed in the US on 25 January 1991.

BACKGROUND OF THE INVENTION

High performance portable computers commonly include a primary or main battery for operating the computer when it is not plugged into an ac power supply. The type of battery selected is dependent upon size, weight, and power requirements and is preferably rechargeable. While there are many battery operated computers available in different sizes ranging from desktop models, to laptops, handheld, and pocket models, the invention is designed for use in high performance systems such as is currently available in many commercially available laptop models.

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Generally most such computers have very simplistic power management systems. Many provide only low battery warning signals allowing the user to save any volatile data on a disk, before the computer is shut off.

In accordance with the invention there is now provided a battery operated computer having a main processor for executing application programs under the control of an operating system, the computer comprising monitoring means including a power management processor for monitoring predetermined conditions including battery conditions and generating interrupt requests upon the occurrence of predetermined first conditions; logic means responsive to signals indicative of predetermined second conditions for generating interrupt requests in response thereto; a plurality of interrupt handlers stored in said computer; interrupt means including an interrupt controller for transmitting interrupt requests to said main processor in response to said interrupt requests from said power management processor and said logic means; and a power control register for controlling the distribution of power in said computer; said main processor being operable in response to said interrupt requests from said interrupt means to selectively execute said interrupt handlers and set said power control register in accordance therewith to thereby control power distribution in said computer.

Briefly, in accordance with a specific embodiment of the invention, a computer has two processors. A main processor operates under the control of an operating system and provides overall control of the computer for executing application programs. The main processor also assists in power management by executing certain interrupts and controlling a power control register to turn power on and off to various devices. A power management processor monitors battery conditions and generates interrupts as a result of predetermined changes. Such processor also controls charging of the battery. Logic means are responsive to predetermined conditions to also generate interrupts.

In the drawings:-

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Fig. 1 is a block diagram of a battery operated computer embodying the invention;

Fig. 2 is a is a plan view of the icon display shown in Fig. 1;

Fig. 3 is a block diagram illustrating the power distribution system shown in Fig. 1;

Fig. 4 is a flow chart of the PMP software interrupt handler operation;

Fig. 5 is a flow chart of the A/M switch handler operation;

Fig. 6 is a flow chart of the "wait on event" operation;

Fig. 7 is a flow chart of the resume handler operation;

Fig. 8 is a flow chart of the recovery-from-sleep operation; and

Fig. 9 is a flow chart of the suspend operation.

DETAILED DESCRIPTION

Referring now to the drawings and first to Fig. 1, a computer 10 selectively operates with power from a battery 11 or from an ac power source. Computer 10 comprises a main processor 12 which is a high performance microprocessor such as an 80386SX microprocessor. Processor 12 is the main or primary processor in computer 10 for executing application programs under the control of an operating system such as IBM DOS or OS/2. Processor 12 is connected to a system bus 14 which in turn is connected to I/O devices such as a backlighted liquid crystal display (LCD) 20, a floppy disk drive (FDD) 16, and a hard disk drive (HDD) 18. Bus 14 is also connected to a dynamic random access memory (DRAM) 22, a read only memory (ROM) 24, and a battery backed, capacitive

metal oxide semiconductor storage device referred to hereafter as CMOS 26. Such elements are conventional and are currently commercially available in portable computers such as laptop computers. Inasmuch as the invention is directed to managing or controlling the battery power, only so much of the structure and operation of conventional elements as is necessary for an understanding of the invention will be described herein.

FDD 16 has its own controller and turns off power consumption when the drive is not being accessed. Power to HDD 18 is controlled by the power management functions of the invention and allows the user to set the length of a time delay for turning off power to the HDD when it has not been accessed for the length of the delay. Power is restored upon any subsequent access to such disk. LCD 20 uses two power inputs to separately control blanking of the LCD screen and control backlighting of the screen to improve visibility. DRAM 22 is the computer main memory and stores application and operating system programs for execution by main processor 12. ROM 24 stores the various interrupt handlers described in detail hereinafter. CMOS 26 stores information on user selections and control flags, as described in detail below.

Bus 14 is further connected to a power control register (PCR) 108, and a power management processor (PMP) 30. PMP 30 is preferably a Hitachi controller chip 330/H8 having its own RAM, ROM, 16-bit CPU, eight analog input pins, watchdog timer (WDT), and sixteen digital I/O pins for receiving and emitting various signals to and from the devices controlled and monitored by the PMP. PMP 30 is connected to a keyboard 28 and monitors the operation of the keyboard in addition to performing power management functions. When a key is actuated or pressed, PMP 30 monitors contact bounce and produces a key scan code when the contacts close and open, much in the same manner as has been done in prior art personal computers by microprocessors dedicated to monitoring keyboard functions. PMP 30 includes a watchdog time (WDT) 32 used as described hereinafter. PMP 30 scans the various lines on a time sliced, round

robin basis, services those that require it and quickly passes over those that don't. PMP 30 has four internal registers (not shown) shared between it and MP 12 for communicating therebetween.

PMP 30 monitors or measures the ambient temperature, battery voltage, current and temperature (AT, V, I, and BT) and uses this information to control battery charging and power consumption. Such measurements are made using four operational amplifiers 38- 1-4 which are respectively connected to a thermistor 46, to a resistor 40 connected to battery 11, across resistor 40, and to a thermistor 42 mounted in the casing of battery 11. Amplifiers 38 are each connected to a different analog input 34 of PMP 30. A line 44 is connected between PMP 30 and amplifier 38-3 to allow a signal of predetermined value to be transmitted to such amplifier and calibrate measurements therefrom. PMP 30 is also connected to a humidity sensor 48 and a comparator 49 that produces a digital input indicating when the ambient humidity within computer 10 is above or below a preset value. When the humidity is above such preset value, the computer 10 is prevented from powering up if it is turned off or from resuming if it is suspended. Further details of monitoring such environmental conditions are described and claimed in the above mentioned related European patent application (2).

Battery 11 is charged when the computer is powered by an ac power source. Such charging occurs when the battery energy is below a fully charged level, and continues until the battery becomes fully charged. When the battery energy level is below the fully charged level, as determined by PMP 30, and the computer is connected to an ac power source, PMP 30 transmits a signal on line 51 to turn on an internal charger 50. The charger controls the rate at which the battery is charged. When the battery becomes fully charged, as determined by PMP 30, PMP 30 then transmits a signal on line 51 to turn off charger 50.

An or gate 54 is used to reset the PMP 30 under three input conditions; when the system voltage becomes "good" such as when a charged battery is installed, in response to a resume signal, and when

the ac adaptor is attached. Such conditions are fed as signals V. GOOD, RESUME, AND AC ADAPTOR ATTACHED on lines 58, 60, and 62. When the lid is closed, the system is suspended and most power is off. Since PMP 30 is used to control the charger, PMP 30 needs its own power to allow the battery to be recharged while the lid is closed. PMP 30 is thus reset when the ac adaptor is connected to a power source and to the computer. A line 62 indicates when the adaptor is attached.

PMP 30 controls an icon display 52 which produces the three icons shown in Fig. 2. The icons are formed in a panel 129 mounted on the computer housing in place conspicuous to the user. A charging icon 130 is highlighted when the battery is being charged. This icon is in the form of an arrow pointing into the battery. A battery shaped fuel icon 136 contains three panels 137. When the battery has a full charge, all three panels are highlighted. As power is consumed, the panels are consecutively turned off to indicate 2/3 full, 1/3 full. When the remaining battery energy is too low, all three panels and the entire icon 136 is flashed indicating an empty battery. A suspend icon 134 has a standard shape for such function and is highlighted when the computer is in suspended mode. Such icon is flashed during resume operations and is shut off after the completion of resume when the system becomes active. Further details of control and operation of display 52 are disclosed and claimed in the above mentioned related European patent application (1).

PMP 30 outputs a LOW BATTERY signal on line 72 when battery 11 becomes discharged and provides an alarm signal on line 118. Line 72 is connected to an or gate 76 which also receives a LID CLOSED signal on input line 74. An and gate 78 receives the output of or gate 76 along with a MOT DOCKED signal on line 80. Computer 10 can also be connected to a docking station (not shown) which is an expansion unit allowing AT cards to be attached to the system, and a NOT DOCKED signal is generated by gate 78 in response to the low battery signal when the computer 10 is not connected to the docking station. The output of gate 78 is a SUSPEND signal that is fed by line 82 into a MUX 96 and controls when the system

is suspended. In summary, the system is suspended when the system is not docked and either the lid is closed and/or the battery is discharged. Further details concerned with the docking station are contained in related European patent application (3).

MUX 96 has a plurality of inputs which are monitored or polled by the MUX for any active inputs. In response to detecting an active input on any line, MUX produces an interrupt request signal PMP INT on output line 98 along with coded signals on line 99 representing or identifying the particular input line having the active signal. Lines 98 and 99 are connected to a controller 100. Controller 100 is a Western Digital 76C10, which includes timers 106 to control backlighting of LCD 20. Timers 106 are reset when keyboard or mouse activity occurs on display 20. The timers count up to a preset value which, when reached, shuts off the display while leaving the backlight on. Controller 100 is connected by lines 102 to processor 12 for interrupting the processor in accordance with its architecture and executing a power management interrupt handler in accordance with the particular type of interrupt. Controller also outputs a signal on line 104 for resetting the power control register when the power comes on after a resume operation.

Line 64 is connected between PMP 30 and MUX 96 and receives an active PMP SOFTWARE INT signal when the software executing in PMP 30 initiates an interrupt. This will happen under the watchdog timeout, beyond temperature, and low battery conditions described with reference to Fig.4. A comparator 70 is connected to an input line 66 of MUX 96 and has an input line 68 receiving a signal indicating the system voltage. Such input is compared against a preset internal value in comparator 70 and when the input is at the normal level of five volts, an V. GOOD signal is generated to thereby initiate a power management interrupt. System voltage is the voltage at the output of the regulated converter 142 (Fig. 3). Such V. GOOD signal becomes active when battery 11 is replaced with a charged battery and when ac power is turned on.

Another MUX input line 84 is connected to a latch 86 that receives an input from the output of an or gate 87 having three inputs 90, 92 and 94 for respectively receiving a time of day alarm signal TOD ALARM, a LID OPENED signal, and a MODEM RING signal. The output of latch 86 is a RESUME signal for switching the computer from the suspended mode to the active mode. This occurs when the lid is opened, when a modem (not shown) is ringing and when a certain time of day has been reached. These last two signals allow the computer to be operated even though the lid is closed giving the user the opportunity to receive modem signals, such as those connected with a FAX operation, or to accomplish a task at a certain time of day, e.g., emit an alarm signal like an alarm clock. Another MUX input is connected to automatic/manual switch A/M 83 so that a power management interrupt is generated when the switch position is changed.

Under battery power, computer 10 operates in two different modes, active and suspend. When active, processor 12 runs at a preselected speed dependent on the setting of switch 83 and the user selection of a manual speed. An application can also shut off power to the processor 12 by turning off its Vcc input, as described below. Processor 12 is connected to a clock speed control 110, which is part of controller 100 and produces three predetermined clock rates of 5, 10 and 20 MHz. When the computer is running under battery power or ac power, the processor is run at a 20 MHz rate or at a rate preselected. When operating under battery power, processor 12 is run at 5, 10 or 20 MHz dependent on the setting of a switch 83 settable to a manual or an automatic position. When set to the manual position, processor 12 operates at a rate preselected by the user. When the switch is set to the automatic position, processor 12 is run in accordance with two options for energy management one of which is preselected by the user, a "high performance" option or a "long battery life" option. The processor speed is automatically managed in accordance with which option is selected. When in the active mode, the various devices including the keyboard, are monitored for activity and if there is no activity after a preset timeout period, the processor is switched to the "sleep" condition in

which the processor is turned off via its Vcc input. Such condition is transparent to the user, and the display is not affected.

An or gate 114 operates speaker 112 with tones from the tone generator 116 or line 118. Tones are changed when the system goes from a full to 2/3, and 2/3 to 1/3, and about 3 minutes before the system suspends. Different Tones are created when the system suspends and resumes, and for keyboard key clicking. Tone generator 116 is controlled by processor 12 executing interrupt routines.

The actual turning on and off of the power to individual devices is controlled by the setting of PCR 108 which is turn is controlled by processor 12 executing the interrupt handling routines. Processor 12 controls the settings of register 108 to provide output signals for controlling power to LCD blanking, mouse keyboard power, optional power, HDD power, backlight power, main processor, planar power, and RS232 drivers power. Register 108 also provides a signal for resetting latch 86 by reset line 85.

Battery 11 is preferably a rechargeable nickel-cadmium (NiCad) battery chosen because of the high watt hours per unit weight and watt hours per unit size ratios. Such technology has proven successful for the past several years, and provides to the user a relatively cheap, readily available replacement. As will be obvious to those skilled in the art, some of the power management techniques used herein are generic to both rechargeable and non-rechargeable batteries. Other techniques are generic to rechargeable batteries. Others such as the particular algorithms to run the fuel gage and determine the battery energy or fuel level as a function of BT, V and I, are limited to NiCad batteries. The difficulty with NiCAd batteries is that the relationship between the remaining energy is not linear with e.g. voltage. Also the charging control might be different for other types of batteries.

Current battery operated computers sometimes have a low battery indicator which when activated provides the user with a signal that is

rather indefinite as to how much time remains. In computer 10, the battery is preferably used until it becomes fully discharged whereupon operation is suspended. The user can then remove the discharged battery and replace it with a fully charged one or plug in the ac adaptor. Such operation has the added advantage of fully discharging a battery to thereby avoid battery memory effects.

Battery 11 is also connected to a power distribution system (PDS) 122, the details of which are generally shown in Fig. 3. Battery 11 is connected by line 146 to a regulated DC/DC converter 142 which converts the battery voltage, which varies in the range 12 to 9 volts, into a system voltage of 5 volts. System voltage is regulated within close tolerances, eg, 2%. Line 150 is connected to the output of converter 142 and to a plurality of field effect transistors (FET) which supply the power to the various devices. The output lines of power control register 108 are respectively connected to the control inputs of the FETs so they are turned on and off dependent on the setting of the control register.

As illustrated in Fig. 2, line 150 is connected to FET 158 and 160 whose output lines 166 and 168 supply power to, e.g., HDD 18 and LCD 20. As shown in Fig. 1, a power line 123 is connected to FET 120, and line 124 is connected between FET 120 and the output line for the MP POWER signal. The output of FET 120 is fed to the Vcc input of processor 12 and is used to turn the processor off when an application calls a BIOS wait loop.

A standby battery 140 is connected by line 152 to a second DC/DC converter 144. Battery 140 supplies a lower voltage (3.3 volts) that is stepped up by converter 144 to the system voltage level and is used to power DRAM 22 when the main battery has been removed for replacement. A charger 146 is connected to line 148 to charge battery 140 from battery 11 so long as 11 has a charge.

Rom 24 stores a basic input/output operating system (BIOS) which includes various power management interrupt handlers and routines for

processing PMP interrupts and accomplishing certain power management functions that will now be described. Referring to Fig. 4, PMP interrupt handler 170 makes a series of decisions as to the type of interrupt and then performs operations dependent on such decisions. Steps 172-180 respectively determine if the interrupt is a watchdog timeout interrupt, a interrupt caused by the ambient temperature being beyond or out of range, a low battery interrupt, a lid closed interrupt, or an A/M switch interrupt. If the decisions in steps 172-178 are negative, and step 180 makes a positive determination, step 182 branches to the A/M switch handler 202 shown in Fig. 5. If step 180 results in a negative determination, then step 184 treats the interrupt as coming from an unknown source e.g., spurious line noise) and returns.

If step 172 concludes the interrupt is from the watchdog timer, step 186 determines if there is a pending suspend, i.e., the suspend operation has already begun but was delayed and has not completed. If so, step 188 restarts the suspend routine. If not, step 190 decrements the suspend timeout. Next, step 192 determines if any I/O device is active. If so, step 194 resets the suspend timeout. If not, step 198 determines if such timeout has expired. If not, step 196 returns to the application in progress. If so, then step 200 starts the suspend routine. Positive determinations from steps 174-178 also branch to step 200 to start the suspend routine.

At the start of the A/M switch handler 202 shown in Fig. 5, step 104 branches to either steps 206 or 216 dependent upon the position of switch 83. If the switch is set to the automatic position, step 206 decides if the user has selected the system to be run to provide high performance or a long battery life. For high performance, step 208 sets up the cpu clock, through clock speed control 110, so that both high and low speed operations are both at 20 Mhz. For long battery life, step 214 sets the clock to run at 20 MHz for high speed and at 5 MHz for low speed. Step 210 thereupon clears the "manual" flag setting in the CMOS and step 212 returns to the application. If the switch is set to the manual position, step 216 copies from CMOS the manual speed which the

user has preselected so that the clock is set at 5, 10, or 20 MHZ for manual speed. Step 218 then sets the "manual" flag in the CMOS and step 212 then returns.

Referring to Fig. 6, routine 220 is invoked when a wait on event" call is made to BIOS by an application program. This routine allows the user the opportunity to conserve battery drainage by shutting off processor 12 and placing is in a sleep condition. Step 222 decides if the "manual" flag has been set. If so, step 224 returns. If not, step 226 determines if the current operation is the first time though routine 202 and if so, branches to step 228 to enable PMP interrupts. Step 230 decides if the computer has a V86 mode of operation. If so, step 232 sets the cpu clock to run at 5 MHz and step 234 returns. If not, step 236 stores all of the real mode CPU registers in processor 12. Then step 238 sets the shutdown code to indicate a sleep condition. Step 240 then holds the CPU and turns off the power to Vcc to effectively provide a 0 MHz speed causing (step 242) processor 12 to be in a sleep condition.

Resume handler 244 (Fig. 7) first flashes (step 246) the suspend icon to indicate that the resume operation is in progress. Next, step 248 restores the parameter settings for any FAX and modems (not shown) present in computer 10. Step 250 then restores the parameter setting for HDD 18 and FDD 16. Step 252 clears any pending interrupts. Steps 254 and 256 respectively turn off the suspend icon to indicate resume has been completed and setup the tone generator to emit a distinctive sound indicating the end of the resume operation. Step 258 then restores the time and date stored in DRAM 22, step 260 restores all cpu registers, and step 262 returns to the application.

When the processor 12 is in a sleep condition, power to processor 12 is turned off. Recovery from sleep routine 264 (Fig. 8) is invoked by a keyboard interrupt which first sets PCR 108 to activate the MP POWER signal and restore power to the processor. Routine 264 first resets the cpu in step 266. Step 268 analyses the shutdown code. If the code is not set to indicate sleep mode, step 274 branches to the resume handler.

If the shutdown code indicates sleep mode, step 270 then restores the cpu registers and step 272 returns.

Referring to Fig. 9, suspend handler 280 is executed in response to the SUSPEND signal and generally performs the task of shutting down all power to the system except for CMOS 26, which has its own backup battery for retaining information stored therein, when the computer has been shut off, and except for DRAM 22. When handler 280 is executed, the following operations occur. First, step 282 decides if any external devices are busy. If none is, then step 292 disables power to LCD 20, to the backlight for the LCD, and to HDD 18. The contents of the cpu registers in main processor 12 are then saved by storing them in DRAM 22 by step 294. A shutdown flag in CMOS 26 is then set by step 296 to direct a Resume operation when the computer is subsequently reset. ext, step 298 saves the contents of registers in the planar and in external devices such as modem, optional devices, etc. Step 300 the sets the hardware to reset the cpu upon commencing a subsequent Resume operation. Step 302 then disables power to the rest of the planar devices, the modem, VGA, communication ports, and keyboard/mouse by setting the control bits stored in PCR 108 accordingly. Step 304 then powers down the cpu and sets it to a halt state. If in step 282 a determination is made that one or more external devices are still busy, step 284 then requests a watchdog timer delay from PMP 30, and a return to application is made by step 286. This action has the effect schematically indicated by line 288 of causing a time delay to wait for any busy device to become idle. Afterwards, a repeat of step 282 results in a negative determination on busy devices and the negative branch operations beginning with step 292 are performed as described above.

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CLAIMS

1. A battery operated computer 10 having a main processor 12 for executing application programs under the control of an operating system, the computer comprising:

monitoring means including a power management processor 30 for monitoring predetermined conditions including battery conditions and generating interrupt requests upon the occurrence of predetermined first conditions;

logic means 96 responsive to signals indicative of predetermined second conditions for generating interrupt requests in response thereto;

a plurality of interrupt handlers stored in said computer;

interrupt means including an interrupt controller 100 for transmitting interrupt requests to said main processor 12 in response to said interrupt requests from said power management processor and said logic means;

and a power control register 108 for controlling the distribution of power in said computer;

said main processor 12 being operable in response to said interrupt requests from said interrupt means to selectively execute said interrupt handlers and set said power control register in accordance therewith to thereby control power distribution in said computer.

2. A computer in accordance with claim 1, wherein:

the power management processor is arranged to monitor a fully discharged battery, over/under ambient temperature, and/or excessive ambient humidity.

3. A computer in accordance with claim 1 or 2 wherein:

the logic means 96 is responsive to signals indicative of a closed/open computer lid, a system voltage level, a time of day alarm, and/or a modem ring.



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4. A computer in accordance with claim 1, 2 or 3 wherein;

said power management processor is arranged to generate an interrupt request signal LOW BATTERY when battery energy level reaches a fully discharged condition;

said interrupt means being responsive to said LOW BATTERY signal to generate a suspend interrupt;

and said interrupt handlers include a suspend interrupt handler operable upon execution to power down said computer into a suspended state.

5. A computer in accordance with claim 1, 2, 3 or 4 comprising:

a dynamic random access memory (DRAM) main memory 22 and a standby battery for powering said DRAM.

6. A computer in accordance with any one of the preceding claims comprising:

second monitoring means for monitoring system voltage and in response to said system voltage reaching a predetermined level as a result of connecting a charged battery to said computer, generating an interrupt causing said computer to be repowered and normal operation to be resumed.

7. A computer in accordance with any one of the preceding claims comprising:

a selectively actuated internal battery charger 50 connectable to a main battery;

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means for connecting said computer to an ac power source;

said power management processor being operable when said computer is connected to said ac power source to monitor the main battery and turn on said charger when said main battery is below a fully charged level.

8. A computer in accordance with claim 7 comprising:

means operable when said main battery becomes discharged to provide visual and sound indications indicative of such condition.

9. A computer in accordance with any one of the preceding claims comprising:

a clock speed controller selectively settable to operate said main processor at a plurality of predetermined rates;

and speed control means operable when said computer is running at a high rate to reduce said speed to a lower rate in response to inactivity of predetermined components in said system.

10. A computer in accordance with claim 9 comprising:

a keyboard connected to said power management processor;

said power management processor being operable to monitor keyboard activity and actuate said speed control means to reduce said speed after a predetermined period of keyboard inactivity.

11. A computer in accordance with claim 9 or 10 comprising:

a non-volatile storage for storing a user selectable performance objective for producing either high performance or long battery life;

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said speed control means being responsive to said performance objective to control said speed in accordance with such objective.

12. A computer in accordance with claim 11 comprising:

a switch selectively settable to a manual position and to an automatic position;

said speed control means being operable to operate said main processor at one of a plurality of predetermined speeds when said switch is in said manual position, said speed control means being operable to operate said processor in accordance with said performance objective when said switch is in said automatic position.

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BATTERY OPERATED COMPUTER POWER MANAGEMENT SYSTEM

ABSTRACT

A computer has two processors. A main processor operates under the control of an operating system and provides overall control of the computer for executing application programs. The main processor also assists in power management by executing certain interrupts and controlling a power control register to turn power on and off to various devices. A power management processor monitors ambient temperature and humidity, and battery conditions, and generates interrupts as a result of predetermined changes. Such processor also controls charging of the battery. Logic means are responsive to predetermined conditions to also generate interrupts.

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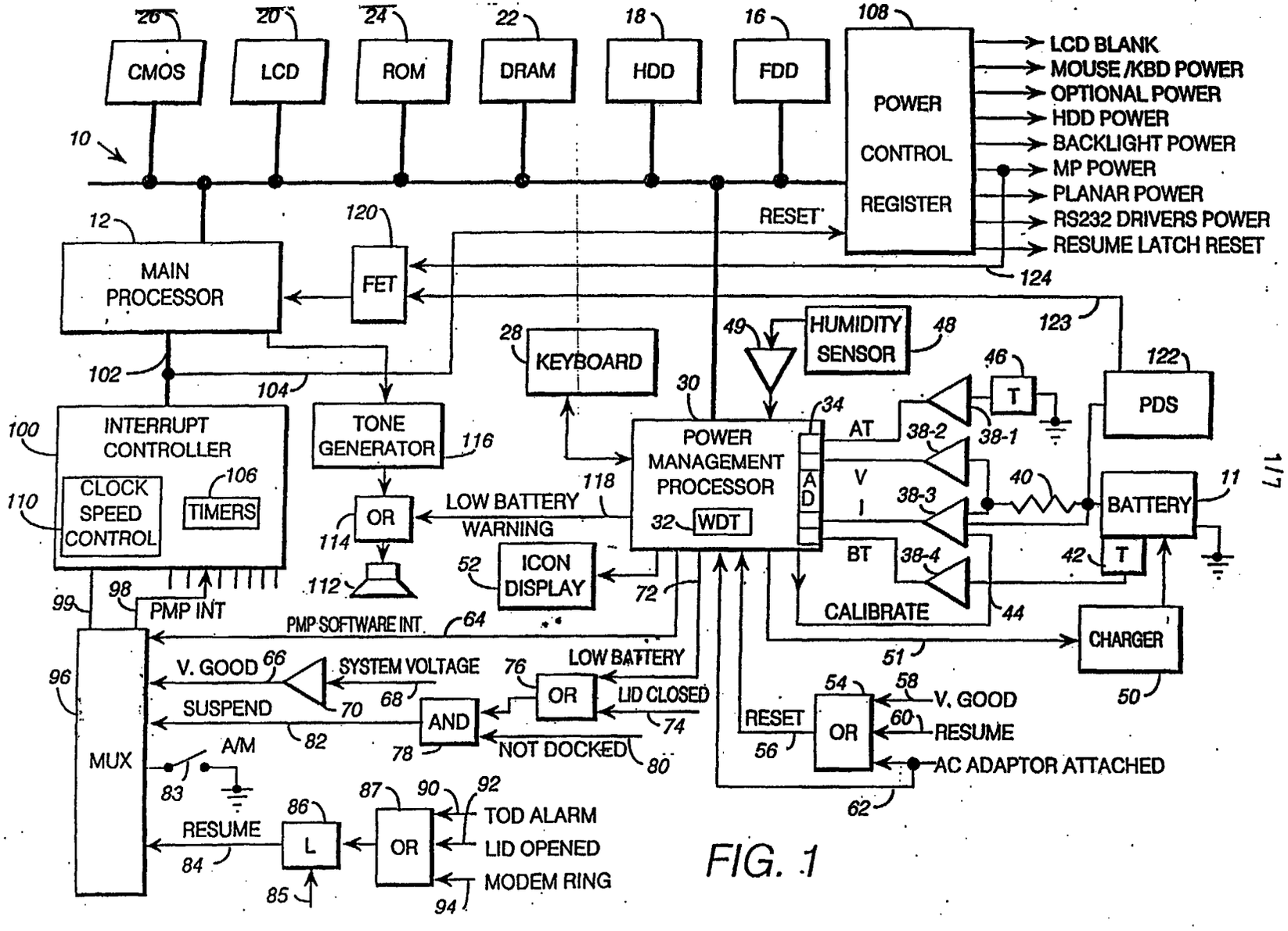
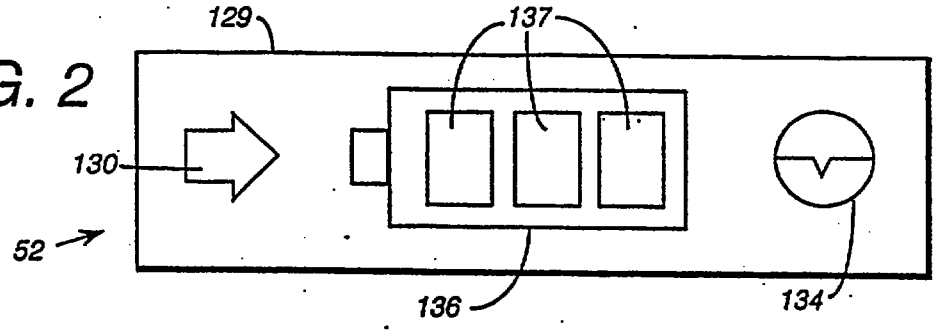

CMOS
LCD
ROM
DRAM
HDD
FDD
POWER CONTROL REGISTER
LCD BLANK
MOUSE /KBD POWER
OPTIONAL POWER
HDD POWER
BACKLIGHT POWER
MP POWER
PLANAR POWER
RS232 DRIVERS POWER
RESUME LATCH RESET
RESET
MAIN PROCESSOR
FET
KEYBOARD
HUMIDITY SENSOR
PDS
INTERRUPT CONTROLLER
CLOCK SPEED CONTROL
TIMERS
TONE GENERATOR
POWER MANAGEMENT PROCESSOR
WDT
AD
AT
V
I
BT
T
BATTERY
LOW BATTERY WARNING
OR
ICON DISPLAY
PMP INT
PMP SOFTWARE INT.
CALIBRATE
CHARGER
MUX
V. GOOD
SYSTEM VOLTAGE
LOW BATTERY
LID CLOSED
SUSPEND
AND
NOT DOCKED
A/M
RESUME
L
TOD ALARM
LID OPENED
MODEM RING
RESET
V. GOOD
RESUME
AC ADAPTOR ATTACHED

FIG. 1

FIG. 2


129
137
130
52
136
134

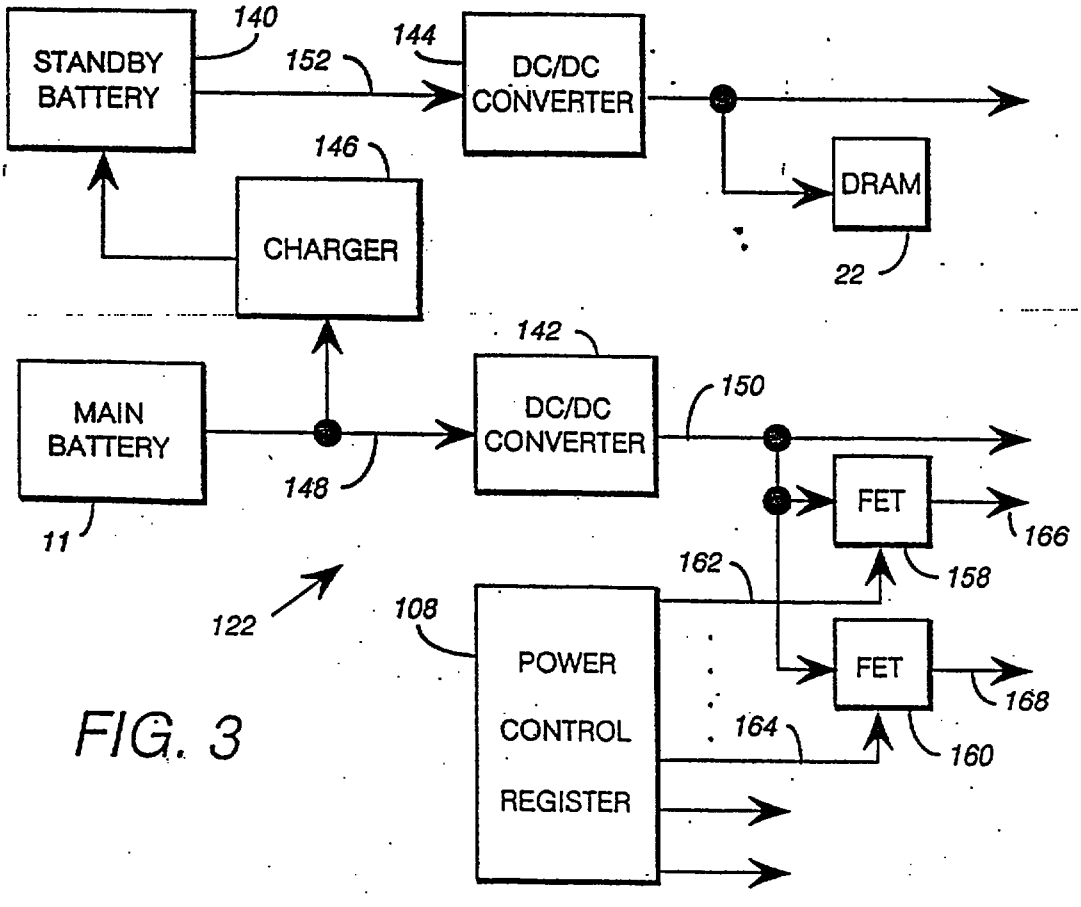

STANDBY BATTERY
140
152
144
DC/DC CONVERTER
146
CHARGER
DRAM
22
142
MAIN BATTERY
148
DC/DC CONVERTER
150
FET
166
11
162
158
122
108
POWER CONTROL REGISTER
FET
168
164
160

FIG. 3

FIG. 4

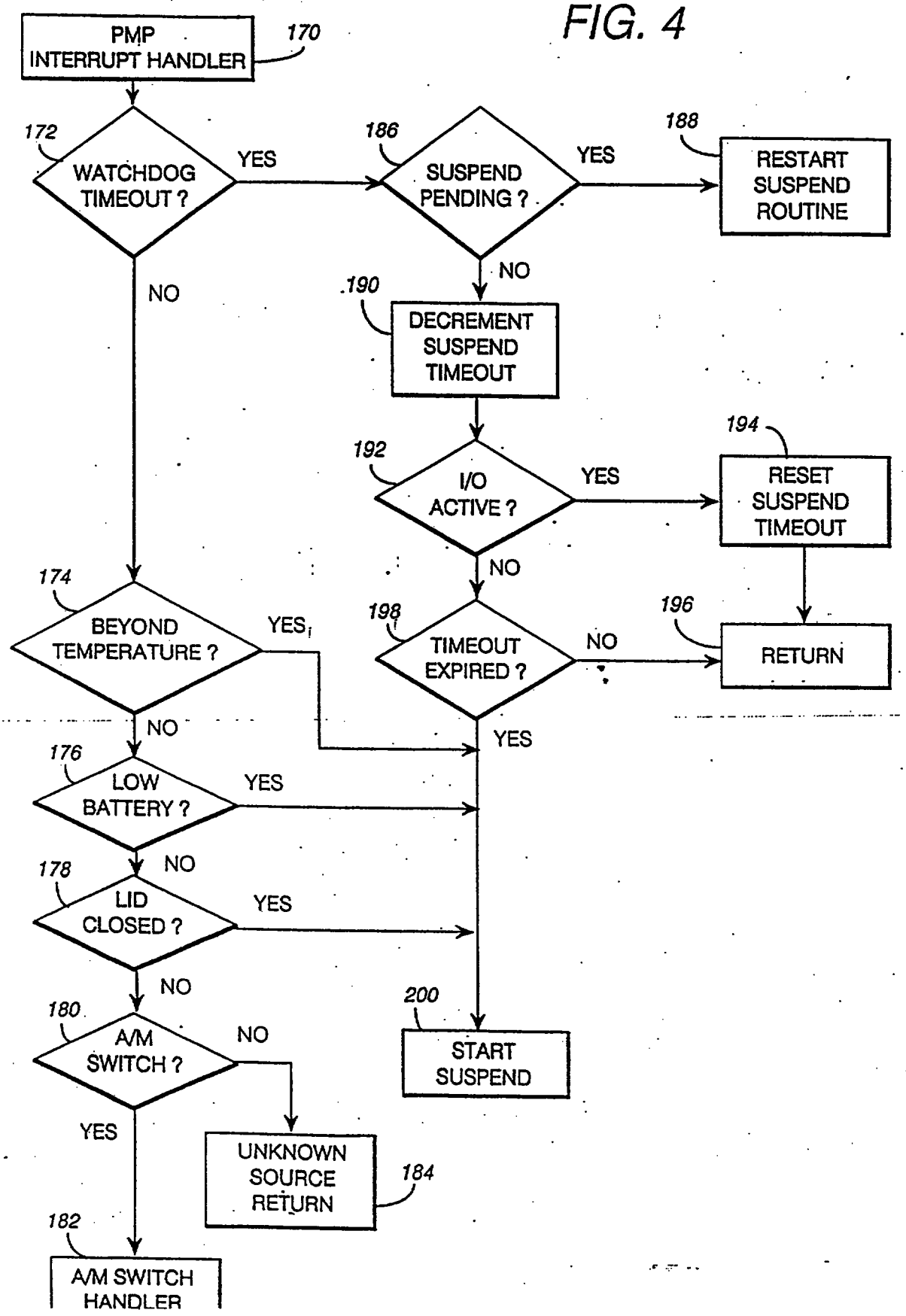
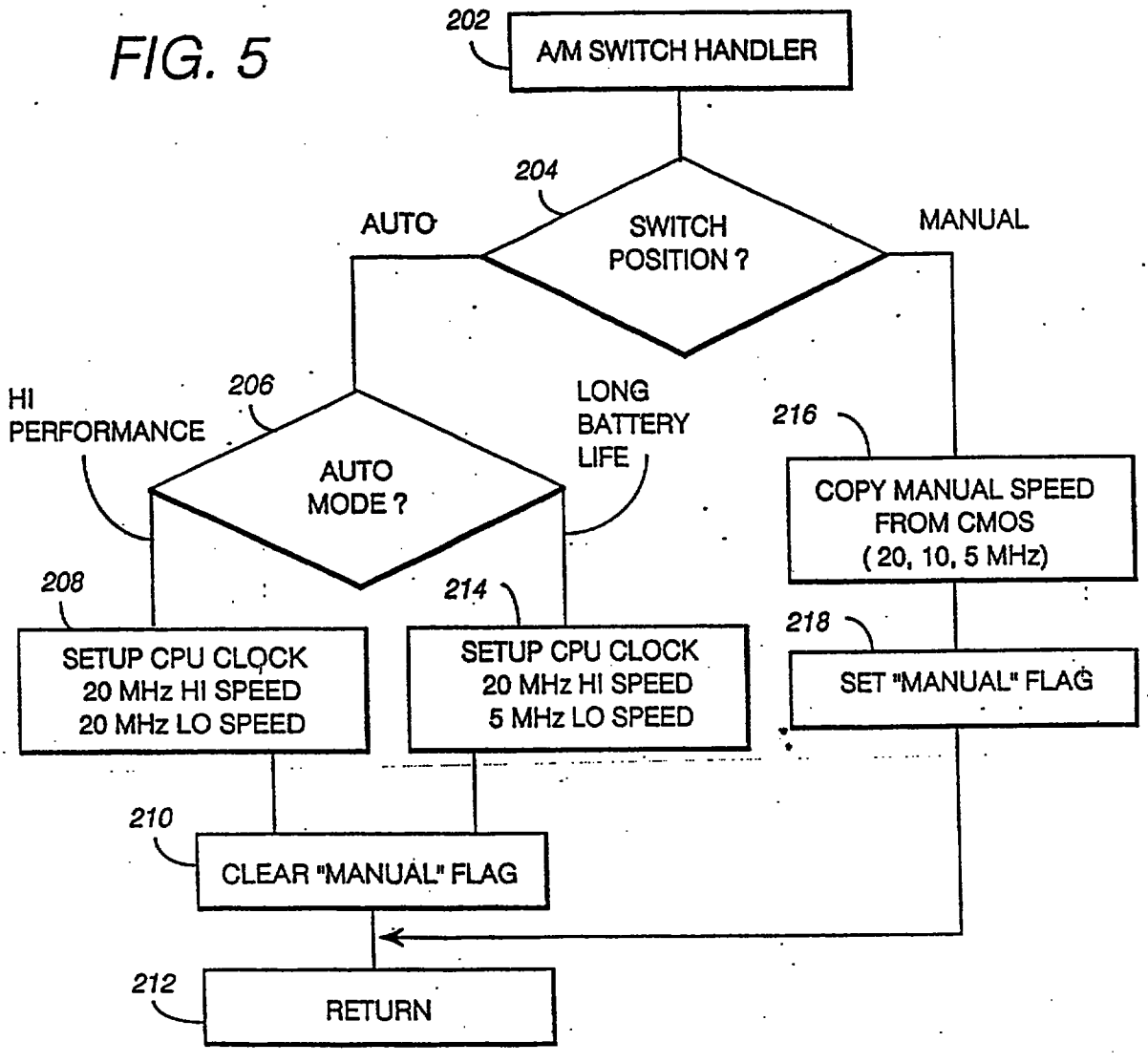

PMP INTERRUPT HANDLER
170
172
WATCHDOG TIMEOUT ?
YES
186
SUSPEND PENDING ?
YES
188
RESTART SUSPEND ROUTINE
NO
NO
190
DECREMENT SUSPEND TIMEOUT
192
I/O ACTIVE ?
YES
194
RESET SUSPEND TIMEOUT
NO
174
BEYOND TEMPERATURE ?
YES
198
TIMEOUT EXPIRED ?
NO
196
RETURN
NO
YES
176
LOW BATTERY ?
YES
NO
178
LID CLOSED ?
YES
NO
200
START SUSPEND
180
A/M SWITCH ?
NO
YES
UNKNOWN SOURCE RETURN
184
182
A/M SWITCH HANDLER

FIG. 5


202
A/M SWITCH HANDLER
204
SWITCH POSITION ?
AUTO
MANUAL
206
AUTO MODE ?
HI PERFORMANCE
LONG BATTERY LIFE
216
COPY MANUAL SPEED FROM CMOS (20, 10, 5 MHz)
208
SETUP CPU CLOCK 20 MHz HI SPEED 20 MHz LO SPEED
214
SETUP CPU CLOCK 20 MHz HI SPEED 5 MHz LO SPEED
218
SET "MANUAL" FLAG
210
CLEAR "MANUAL" FLAG
212
RETURN

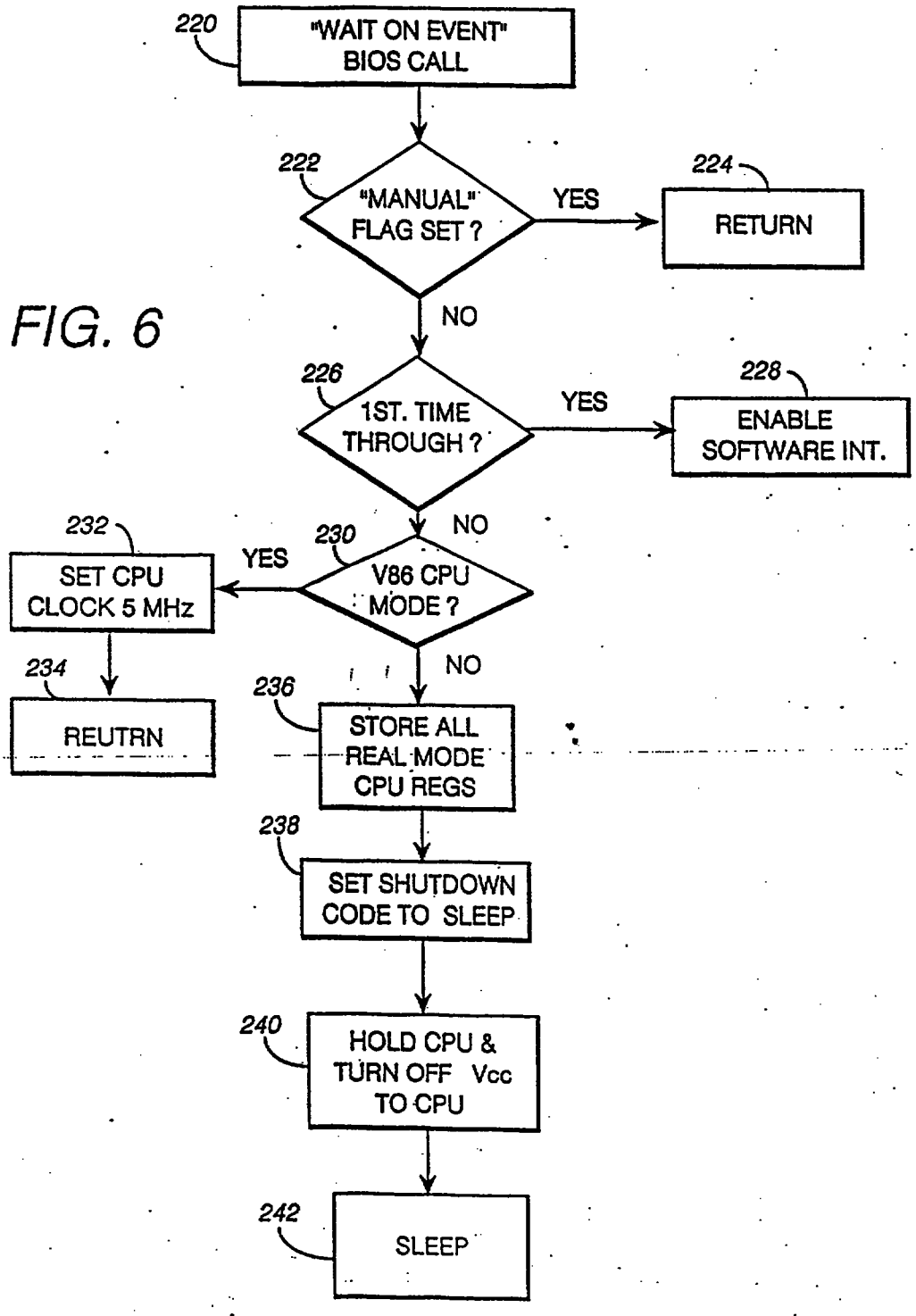

220
"WAIT ON EVENT" BIOS CALL
222
"MANUAL" FLAG SET ?
YES
224
RETURN
NO
226
1ST. TIME THROUGH ?
YES
228
ENABLE SOFTWARE INT.
NO
230
V86 CPU MODE ?
YES
232
SET CPU CLOCK 5 MHz
234
REUTRN
NO
236
STORE ALL REAL MODE CPU REGS
238
SET SHUTDOWN CODE TO SLEEP
240
HOLD CPU & TURN OFF Vcc TO CPU
242
SLEEP

FIG. 6

FIG. 7

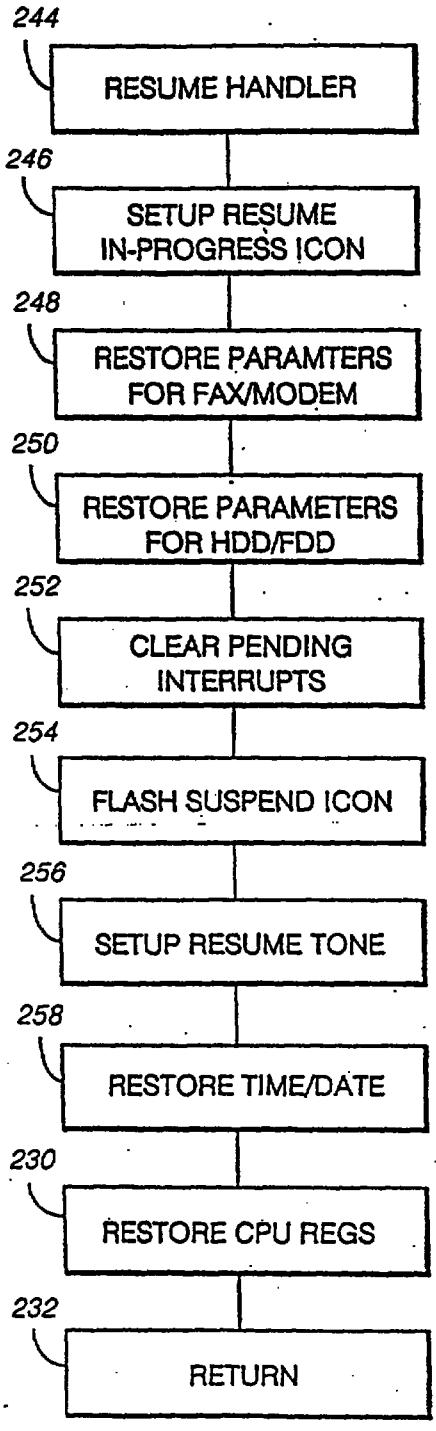

244
RESUME HANDLER
246
SETUP RESUME IN-PROGRESS ICON
248
RESTORE PARAMTERS FOR FAX/MODEM
250
RESTORE PARAMETERS FOR HDD/FDD
252
CLEAR PENDING INTERRUPTS
254
FLASH SUSPEND ICON
256
SETUP RESUME TONE
258
RESTORE TIME/DATE
230
RESTORE CPU REGS
232
RETURN

FIG. 8

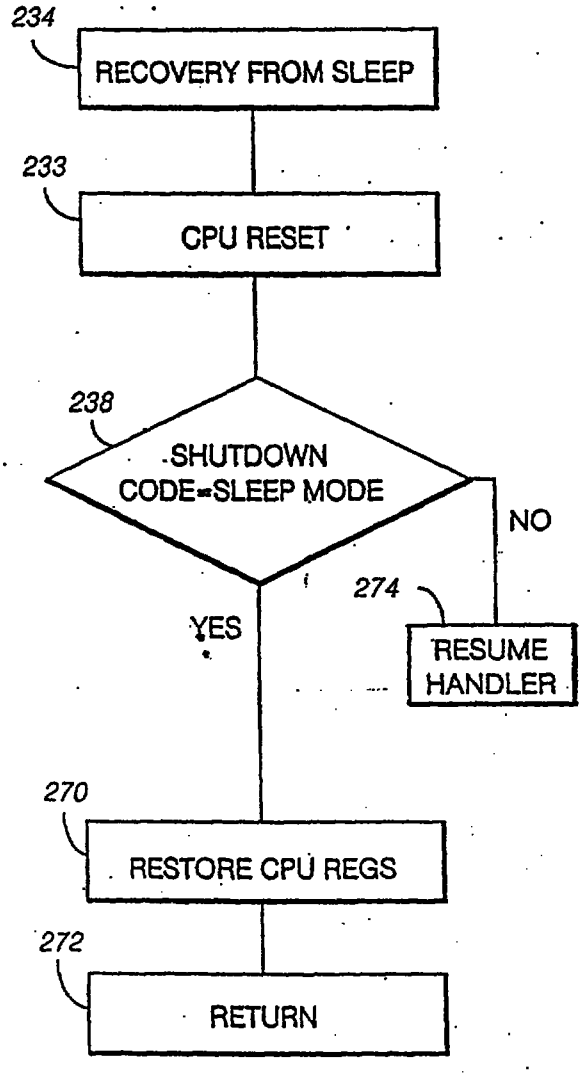
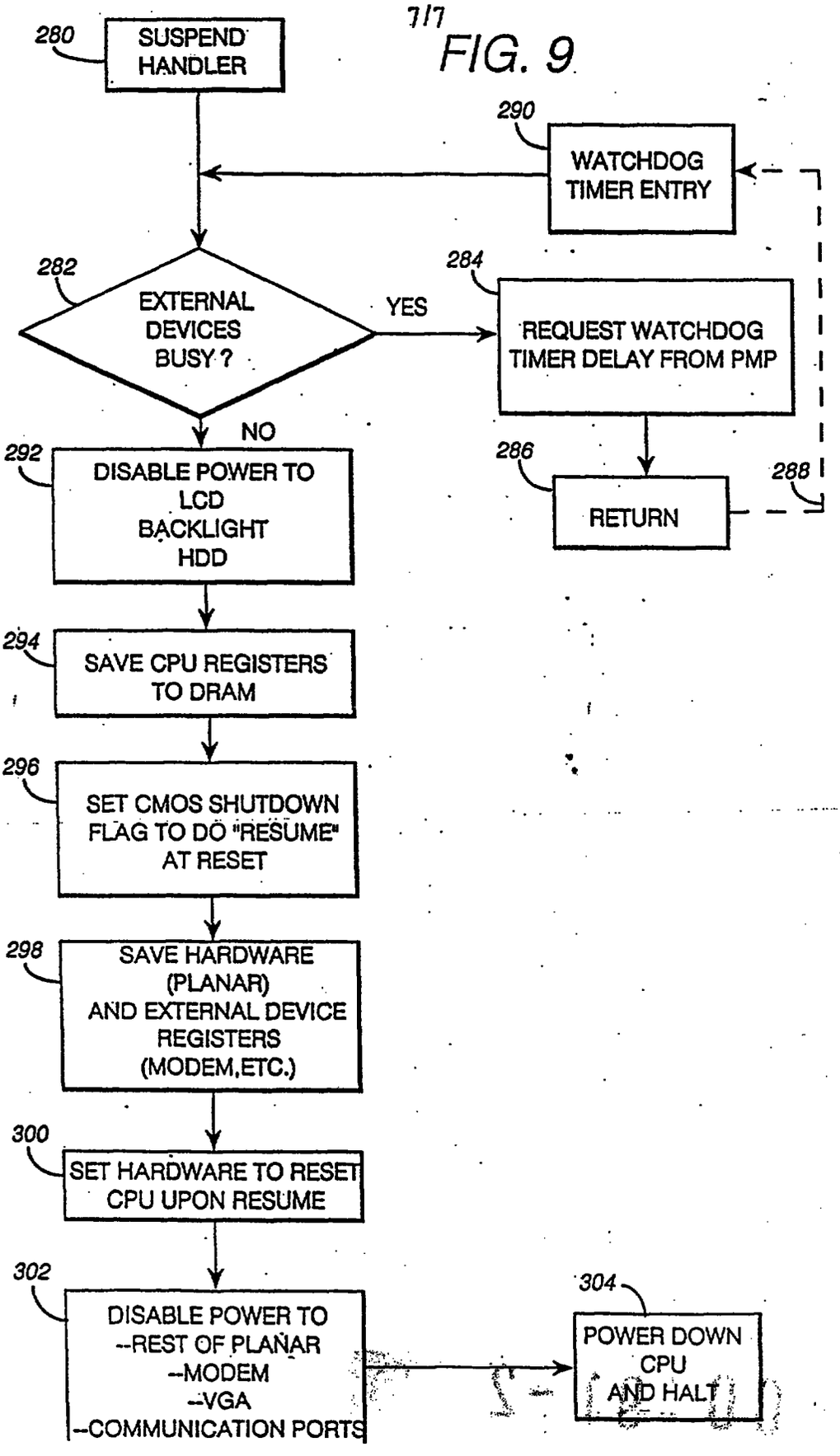

234
RECOVERY FROM SLEEP
233
CPU RESET
238
SHUTDOWN CODE=SLEEP MODE
NO
274
RESUME HANDLER
YES
270
RESTORE CPU REGS
272
RETURN

FIG. 9


280
SUSPEND HANDLER
290
WATCHDOG TIMER ENTRY
282
EXTERNAL DEVICES BUSY ?
YES
284
REQUEST WATCHDOG TIMER DELAY FROM PMP
NO
292
DISABLE POWER TO LCD BACKLIGHT HDD
286
RETURN
288
294
SAVE CPU REGISTERS TO DRAM
296
SET CMOS SHUTDOWN FLAG TO DO "RESUME" AT RESET
298
SAVE HARDWARE (PLANAR) AND EXTERNAL DEVICE REGISTERS (MODEM,ETC.)
300
SET HARDWARE TO RESET CPU UPON RESUME
302
DISABLE POWER TO
--REST OF PLANAR
--MODEM
--VGA
--COMMUNICATION PORTS
304
POWER DOWN CPU AND HALT

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BATTERY OPERATED COMPUTER POWER MANAGEMENT SYSTEM

ABSTRACT

A computer has two processors. A main processor (12) operates under the control of an operating system and provides overall control of the computer for executing application programs. The main processor (12) also assists in power management by executing certain interrupts and controlling a power control register (108) to turn power on and off to various devices. A power management processor (30) monitors ambient temperature and humidity, and battery conditions, and generates interrupts as a result of predetermined changes. Such processor (108) also controls charging of the battery. Logic means are responsive to predetermined conditions to also generate interrupts.

Fig. 1

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REPLACEMENT SHEET
24 MAY 1996

Generally most such computers have very simplistic power management systems. Many provide only low battery warning signals allowing the user to save any volatile data on a disk, before the computer is shut off.

SUMMARY OF THE INVENTION

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is provided in a battery operated computer having a main processor for executing application programs under the control of an operating system; a plurality of I/O devices; and a dynamic random access memory (DRAM) for storing said application programs and said operating system for execution by said main processor; the combination comprising: a power distribution system including a power control register operable under the control of said main processor for controlling power distribution in said computer, said power distribution system being connectable to a replaceable main battery for powering said computer to operate said main processor, said I/O devices, and said DRAM, said power distribution system being further connectable to a standby battery for powering said DRAM when said main battery is removed; said power control register being connected to different lines of said power distribution system and having different bits that are selectively set by said main processor to provide on/off control of power distributed along said lines; first monitoring means including a power management processor (PMP) connected to said power distribution system for monitoring predetermined conditions including power level of said main battery and generating interrupt requests upon the occurrence of predetermined first conditions, said monitoring means being operative to generate a suspend interrupt request immediately prior to said main battery becoming fully discharged; interrupt means connected to said first monitoring means and including an interrupt controller for transmitting an interrupt request signal to said main processor in response to said suspend interrupt request from said first monitoring means; storage

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☑ Description : paged 2 and 2a to paged ....
☑ Claim(s) : paged 1 to paged 11
☐ Drawing(s) : paged ..... to paged .....
☑ Abstract : paged 12 to paged ....

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means connected to said main processor for storing a plurality of interrupt handlers including a suspend-interrupt handler; said main processor being operative in response to said interrupt requests form said interrupt means to selectively execute said interrupt handlers and set said power control register in accordance therewith to thereby control power distribution in said computer, said main processor being operative to execute said suspend interrupt handler immediately prior to said main battery becoming fully discharged to first store CPU information from said main processor in said DRAM and then power down said computer whereby said standby battery retains information in said DRAM when said main battery is removed for replacement; and restoration means responsive to connecting said power distribution system to a source of power, after said main battery has been removed, to power up said computer, restore said CPU information from said DRAM into said main processor, and resume normal operation of said computer.

According to another aspect of the present invention there is provided in a battery operated computer having a main processor for executing application programs under the control of an operating system; a plurality of I/O devices; and a dynamic random access memory (DRAM) for storing said application programs and said operating system for execution by said main processor; the combination comprising: a power distribution system including a power control register operable under the control of said main processor for controlling power distribution in said computer, said power distribution system being connectable to a replaceable main battery for powering said computer to operate said main processor, said I/O devices, and said DRAM, said power distribution system being further connectable to a standby battery for powering said DRAM when said main battery is removed; said power control register being connected to different lines of said power distribution system and having different bits that are selectively set by said main processor to provide on/off control of power distributed along said lines; first monitoring means including a power management processor (PMP) connected to said power distribution system for monitoring predetermined conditions including power

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level of said main battery and generating interrupt requests upon the occurrence of predetermined first conditions, said monitoring means being operative to generate a suspend interrupt request immediately prior to said main battery becoming fully discharged; interrupt means connected to said first monitoring means and including an interrupt controller for transmitting an interrupt request signal to said main processor in response to said suspend interrupt request from said first monitoring means; storage means connected to said main processor for storing a plurality of interrupt handlers including a suspend interrupt handler; a clock speed controller selectively settable to operate said main processor at one of a plurality of predetermined rates; a user actuated first switch for selecting one of said predetermined rates; a non-volatile storage for storing a user selectable energy option for accomplishing either a high performance objective or a long battery life objective; a user actuated second switch selectively settable to a "manual" position and to an "automatic" position; speed control means connected to said clock speed controller, said speed control means being operative when said second switch is in said "manual" position to set said clock speed controller to operate at the rate selected by said first switch, said speed control means being further operative when said second switch is in said "automatic" position to set said clock speed controller in accordance with said energy option and operate said processor at a high rate when said high performance objective is selected and operate said processor when said long battery life objective is selected by switching between a high rate and a low rate dependent on system activity; said main processor being operative in response to said interrupt requests from said interrupt means to selectively execute said interrupt handlers and set said power control register in accordance therewith to thereby control power distribution in said computer, said main processor being operative to execute said suspend handler immediately prior to said main battery becoming fully discharged to first store CPU information from said main processor in said DRAM and then power down said computer whereby said standby battery retains information in said DRAM

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when said main battery is removed for replacement; and restoration means responsive to connecting said power distribution system to a source of power, after said main battery has been removed, to power up said computer, restore said CPU information from said DRAM into said main processor, and resume normal operation of said computer.

DESCRIPTION OF THE PREFERRRED EMBODIMENT(S)

In the drawings:-

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CLAIMS

1. In a battery operated computer having a main processor for executing application programs under the control of an operating system; a plurality of I/O devices; and a dynamic random access memory (DRAM) for storing said application programs and said operating system for execution by said main processor; the combination comprising:

a power distribution system including a power control register operable under the control of said main processor for controlling power distribution in said computer, said power distribution system being connectable to a replaceable main battery for powering said computer to operate said main processor, said I/O devices, and said DRAM, said power distribution system being further connectable to a standby battery for powering said DRAM when said main battery is removed;

said power control register being connected to different lines of said power distribution system and having different bits that are selectively set by said main processor to provide on/off control of power distributed along said lines;

first monitoring means including a power management processor (PMP) connected to said power distribution system for monitoring predetermined conditions including power level of said main battery and generating interrupt requests upon the occurrence of predetermined first conditions, said monitoring means being operative to generate a suspend interrupt request immediately prior to said main battery becoming fully discharged;

interrupt means connected to said first monitoring means and including an interrupt controller for transmitting an interrupt request signal to said main processor in response to said suspend interrupt request from said first monitoring means;

storage means connected to said main processor for storing a plurality of interrupt handlers including a suspend interrupt handler;

said main processor being operative in response to said interrupt requests form said interrupt means to selectively execute said interrupt handlers and set said power control register in accordance therewith to thereby control power distribution in said computer,

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said main processor being operative to execute said suspend interrupt handler immediately prior to said main battery becoming fully discharged to first store CPU information from said main processor in said DRAM and then power down said computer whereby said standby battery retains information in said DRAM when said main battery is removed for replacement;

and restoration means responsive to connecting said power distribution system to a source of power, after said main battery has been removed, to power up said computer, restore said CPU information from said DRAM into said main processor, and resume normal operation of said computer.

2. A computer in accordance with claim 1 wherein said restoration means comprises second monitoring means for monitoring system voltage in said power distribution system, said second monitoring means being operable in response to said system voltage reaching a predetermined level as a result of connecting a charged backup battery to said power distribution system.

3. A computer in accordance with claim 2 wherein:

said logic means is responsive to signals indicative of predetermined conditions for generating resume interrupt requests in response thereto, said predetermined conditions including a lid open, a time of day alarm, and a modem ring;

said interrupt means includes a resume interrupt handler stored in said computer; and

said main processor is further operative to execute said resume handler in response to a resume interrupt request to restore CPU information from said DRAM to said main processor and power up said computer.

4. A computer in accordance with claim 1 wherein:

said PMP generates a low battery signal immediately prior to said main battery becoming fully discharged; and

said first monitoring means comprises logic means connected to said PMP and said interrupt means for translating said low battery signal into said suspend interrupt request,

said logic means being further operable to translate a signal indicative of a computer lid being closed into a second suspend interrupt request, said processor being operative to further execute said suspend handler in response to said logic means generating said second suspend interrupt request.

5. A computer in accordance with claim 1 comprising:

a selectively actuated internal main battery charger connectable to said main battery; and

means for connecting said computer to an ac power source;

said PMP being operable when said computer is connected to said ac power source to monitor said main battery and turn on said charger when said main battery is below a fully charged level.

6. A computer in accordance with claim 1 comprising:

second logic means connected to said interrupt means for generating interrupt requests in response to receipt of signals representing conditions selected from the group of closed/open computer lid, system voltage level, time of day alarm, and modes ring.

7. In a battery operated computer having a main processor for executing application programs under the control of an operating system; a plurality of I/O devices; and a dynamic random access memory (DRAM) for storing said application programs and said operating system for execution by said main processor; the combination comprising:

a power distribution system including a power control register operable under the control of said main processor for controlling power distribution in said computer, said power distribution system being connectable to a replaceable main battery for powering said computer to operate said main processor, said I/O devices, and said DRAM, said power distribution system being further connectable to a standby battery for powering said DRAM when said main battery is removed;

said power control register being connected to different lines of said power distribution system and having different bits that are selectively set by said main processor to provide on/off control of power distributed along said lines;

first monitoring means including a power management processor (PMP) connected to said power distribution system for monitoring predetermined conditions including power level of said main battery and generating interrupt requests upon the occurrence of predetermined first conditions, said monitoring means being operative to generate a suspend interrupt request immediately prior to said main battery becoming fully discharged;

interrupt means connected to said first monitoring means and including an interrupt controller for transmitting an interrupt request signal to said main processor in response to said suspend interrupt request from said first monitoring means;

storage means connected to said main processor for storing a plurality of interrupt handlers including a suspend interrupt handler;

a clock speed controller selectively settable to operate said main processor at one of a plurality of predetermined rates;

a user actuated first switch for selecting one of said predetermined rates;

a non-volatile storage for storing a user selectable energy option for accomplishing either a high performance objective or a long battery life objective;

a user actuated second switch selectively settable to a "manual" position and to an "automatic" position;

speed control means connected to said clock speed controller, said speed control means being operative when said second switch is in said "manual" position to set said clock speed controller to operate at the rate selected by said first switch, said speed control means being further operative when said second switch is in said "automatic" position to set said clock speed controller in accordance with said energy option and operate said processor at a high rate when said high performance objective is selected and operate said processor when said long battery life objective is selected by switching between a high rate and a low rate dependent on system activity;

said main processor being operative in response to said interrupt requests from said interrupt means to selectively execute said interrupt handlers and set said power control

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register in accordance therewith to thereby control power distribution in said computer, said main processor being operative to execute said suspend handler immediately prior to said main battery becoming fully discharged to first store CPU information from said main processor in said DRAM and then power down said computer whereby said standby battery retains information in said DRAM when said main battery is removed for replacement;

and restoration means responsive to connecting said power distribution system to a source of power, after said main battery has been removed, to power up said computer, restore said CPU information from said DRAM into said main processor, and resume normal operation of said computer.

8. A computer in accordance with claim 7 wherein said restoration means comprises second monitoring means for monitoring system voltage in said power distribution system, said restoration means being operable in response to said system voltage reaching a predetermined level as a result of connecting a charged backup battery to said power distribution system.

9. A computer in accordance with claim 8 wherein:

said logic means is responsive to signals indicative of predetermined conditions for generating resume interrupt requests in response thereto, said predetermined conditions including a lid open, a time of day alarm, and a modem ring;

said interrupt means includes a resume interrupt handler stored in said computer; and

said main processor is further operative to execute said resume handler in response to a resume interrupt request to restore CPU information from said DRAM to said main processor and power up said computer.

10. A computer in accordance with claim 7 wherein:

said PMP generates a low battery signal immediately prior to said main battery becoming fully discharged; and

said first monitoring means comprises logic means connected to said PMP and said interrupt means for translating said low battery signal into said suspend interrupt request, said logic means being further operable to translate a signal indicative of a computer lid being closed into a second suspend interrupt request, said processor being operative to further execute said suspend handler in response to said logic means generating said second suspend interrupt request.

11. A computer in accordance with claim 7 comprising:

a selectively actuated internal main battery charger connectable to said main battery; and

means for connecting said computer to an ac power source;

said PMP being operable when said computer is connected to said ac power source to monitor said main battery and turn on said charger when said main battery is below a fully charged level.

12. A computer in accordance with claim 7 comprising:

second logic means connected to said interrupt means for generating interrupt requests in response to receipt of signals representing conditions selected from the group of closed/open computer lid, system voltage level, time of day alarm, and modem ring.

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BATTERY OPERATED COMPUTER POWER MANAGEMENT SYSTEM

ABSTRACT

A computer has two processors. A main processor (12) operates under the control of an operating system and provides overall control of the computer for executing application programs. The main processor (12) also assists in power management by executing certain interrupts and controlling a power control register (108) to turn power on and off to various devices. A power management processor (30) monitors ambient temperature and humidity, and battery conditions, and generates interrupts as a result of predetermined changes. Such processor (108) also controls charging of the battery. Logic means are responsive to predetermined conditions to also generate interrupts.

Fig. 1

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