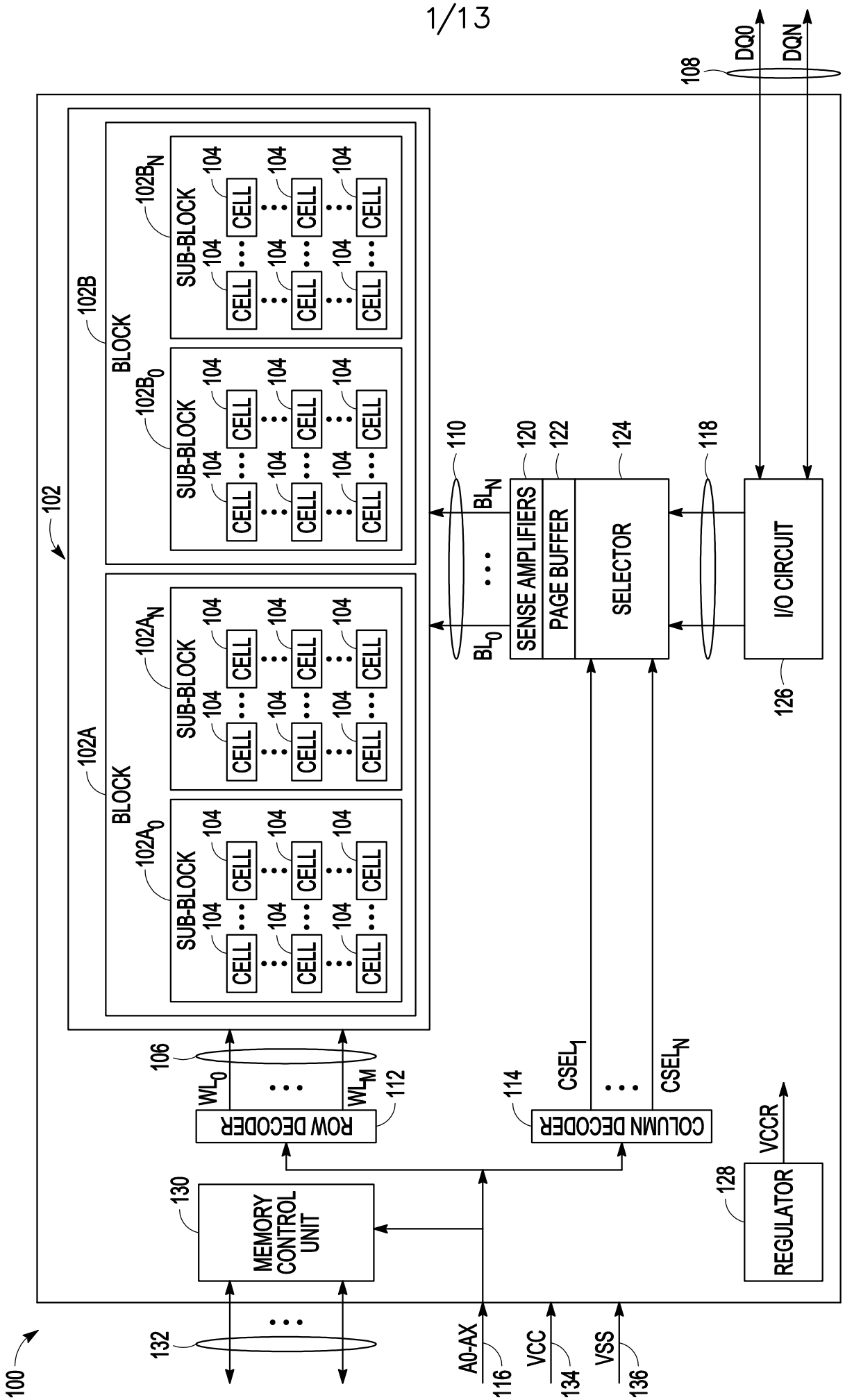

100
102
102A
BLOCK
$102A_0$
$102A_N$
102B
BLOCK
$102B_0$
$102B_N$
SUB-BLOCK
104
CELL
106
$WL_0$
$WL_M$
112
ROW DECODER
110
$BL_0$
$BL_N$
SENSE AMPLIFIERS
120
PAGE BUFFER
122
SELECTOR
124
118
I/O CIRCUIT
126
108
DQ0
DQN
114
$CSEL_1$
$CSEL_N$
COLUMN DECODER
130
MEMORY CONTROL UNIT
128
REGULATOR
VCCR
132
A0-AX
116
VCC
134
VSS
136

FIG. 1

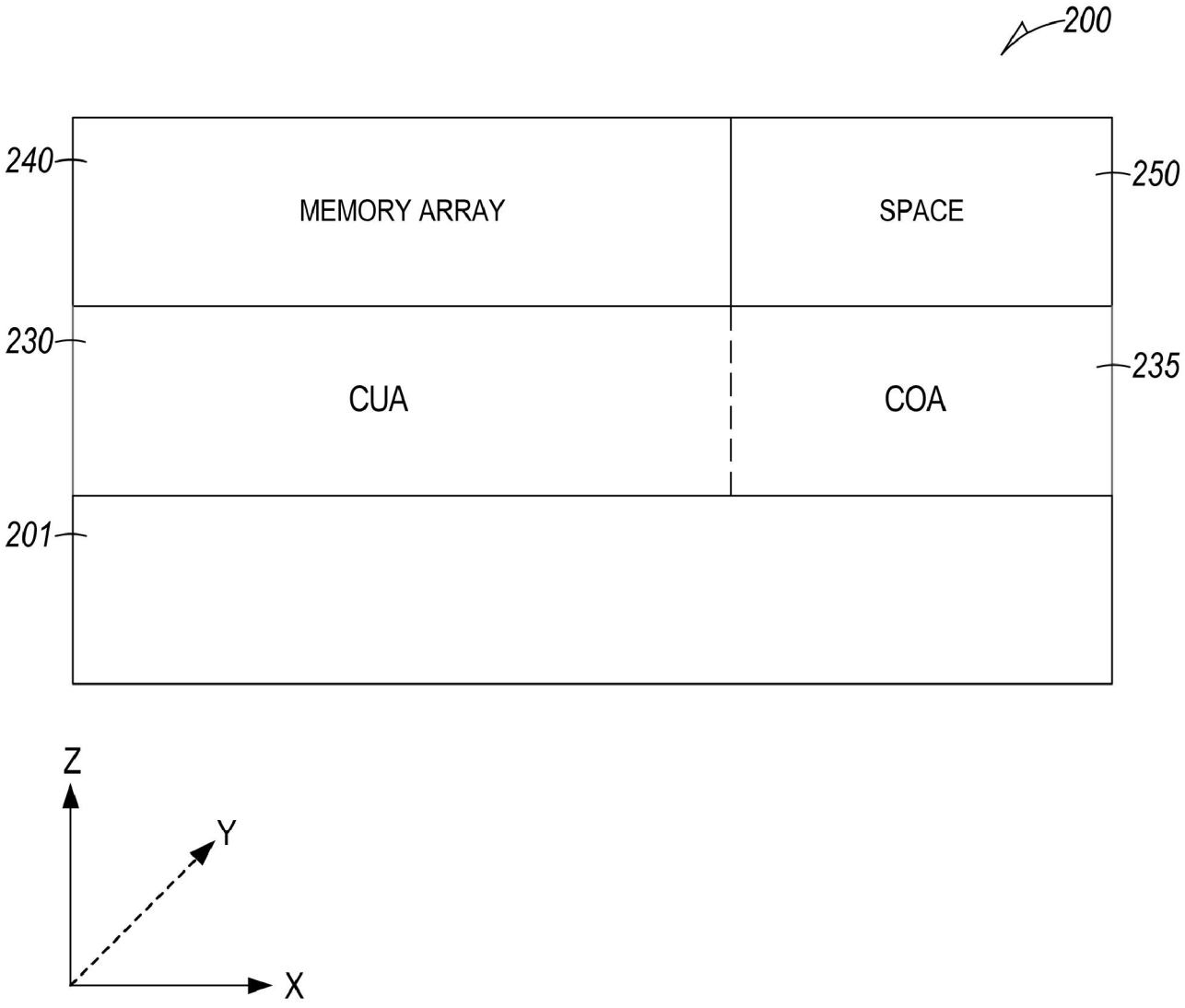



FIG. 2

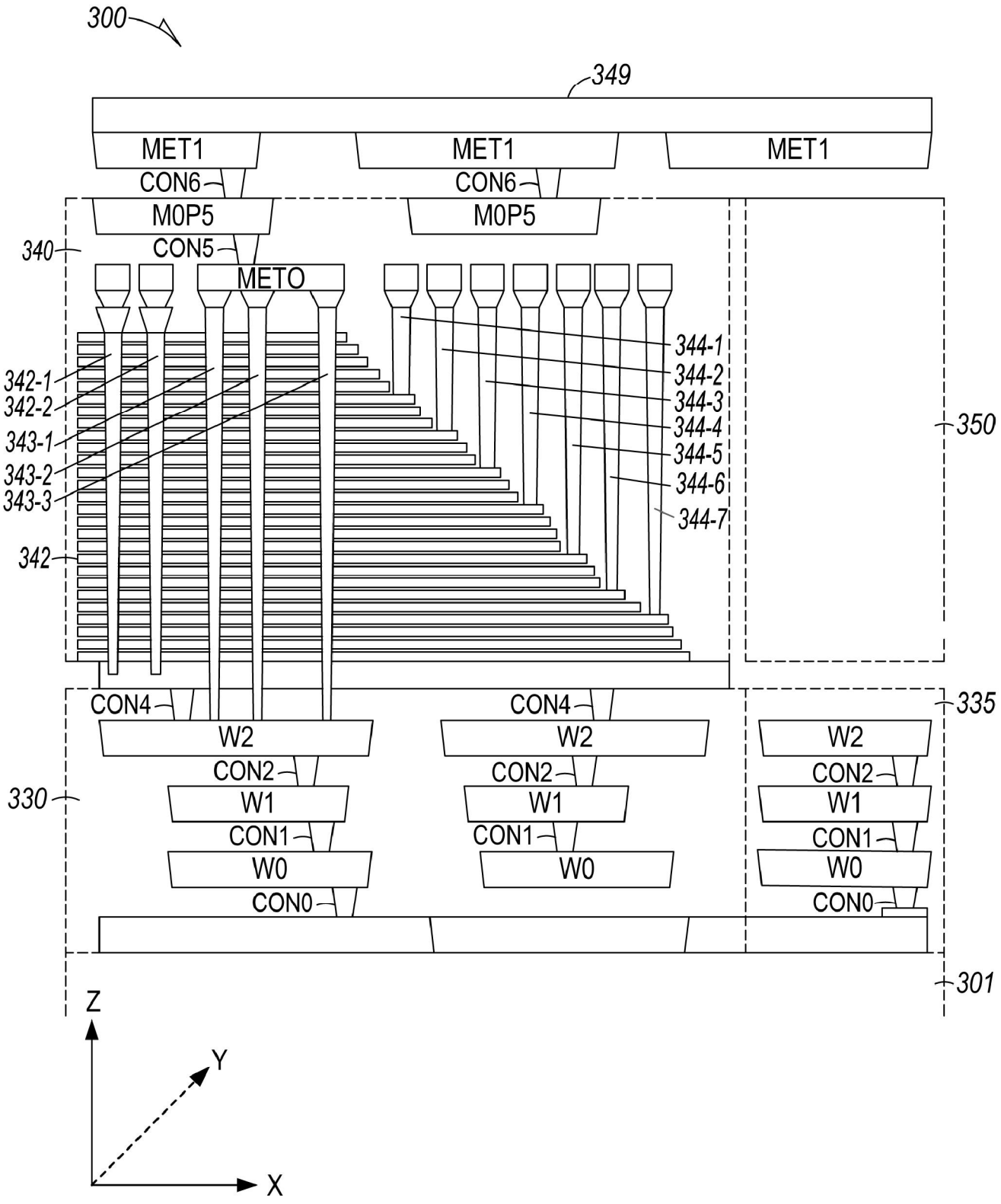

300
349
MET1
MET1
MET1
CON6
CON6
M0P5
M0P5
340
CON5
METO
342-1
342-2
343-1
343-2
343-3
342
344-1
344-2
344-3
344-4
344-5
344-6
344-7
350
CON4
CON4
335
W2
W2
W2
CON2
CON2
CON2
330
W1
W1
W1
CON1
CON1
CON1
W0
W0
W0
CON0
CON0
301
Z
Y
X

FIG. 3

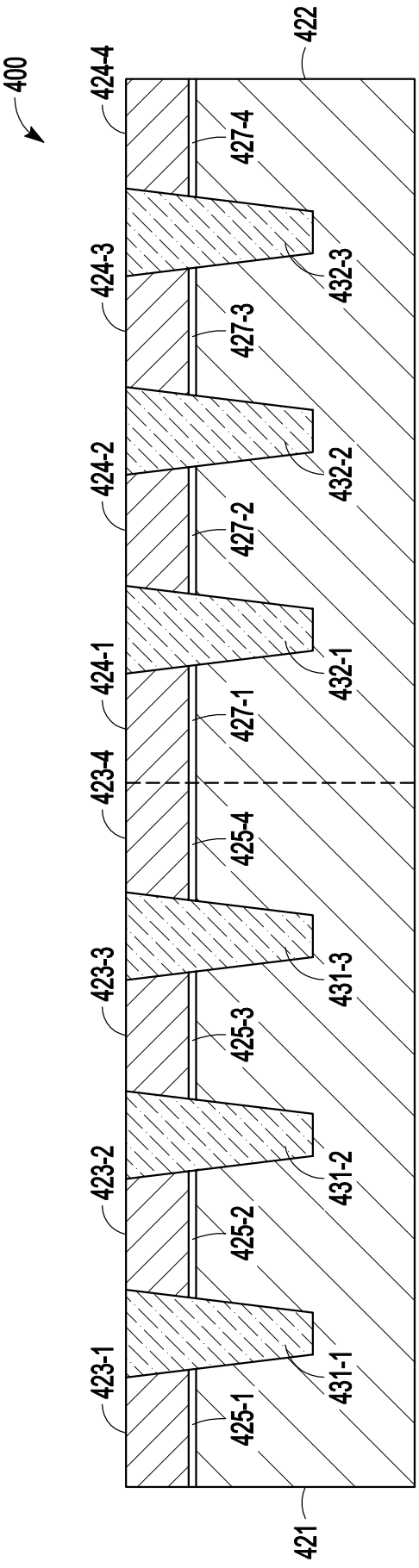

400
422
424-4
427-4
424-3
432-3
427-3
424-2
432-2
427-2
424-1
432-1
427-1
423-4
425-4
423-3
431-3
425-3
423-2
431-2
425-2
423-1
431-1
425-1
421

FIG. 4

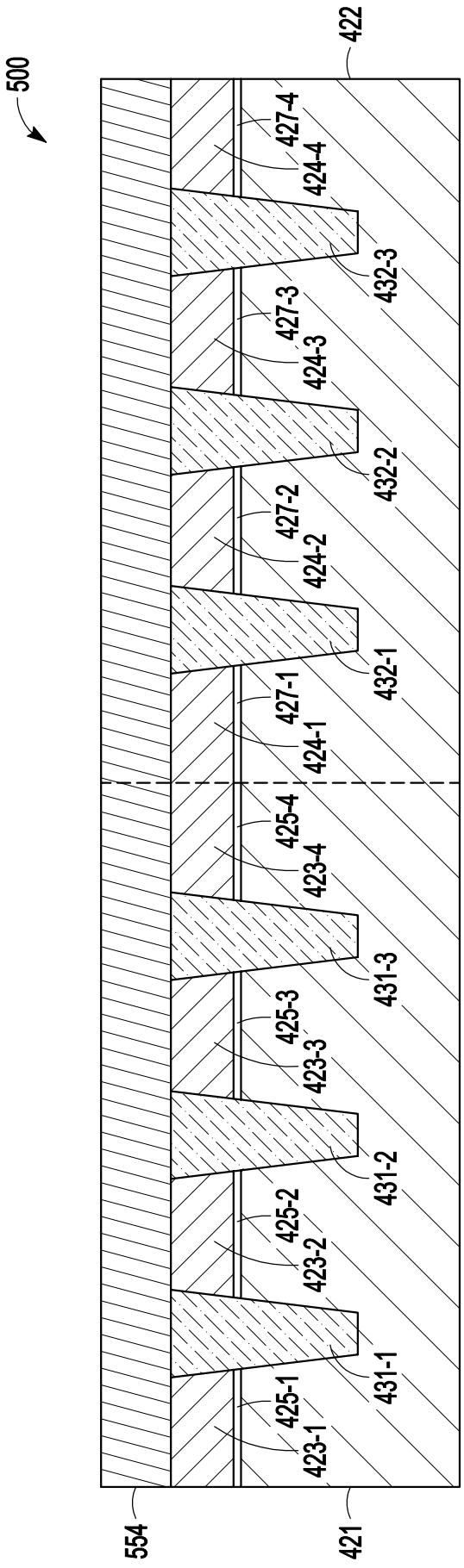

500
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
554
421

FIG. 5

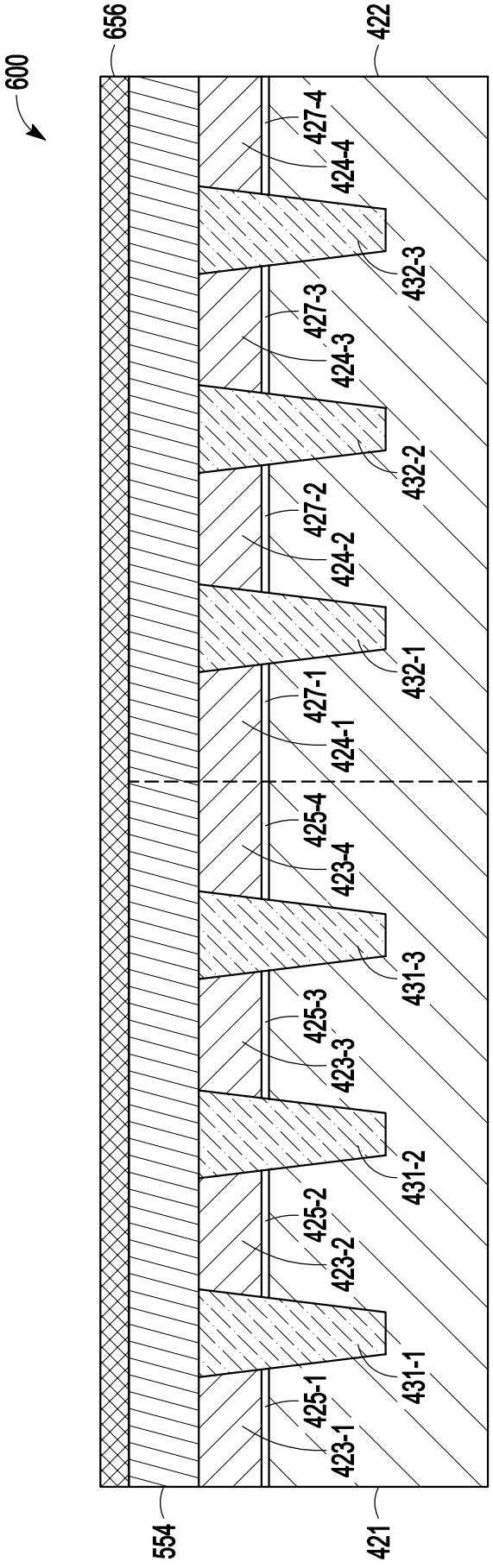

600
656
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
554
421

FIG. 6

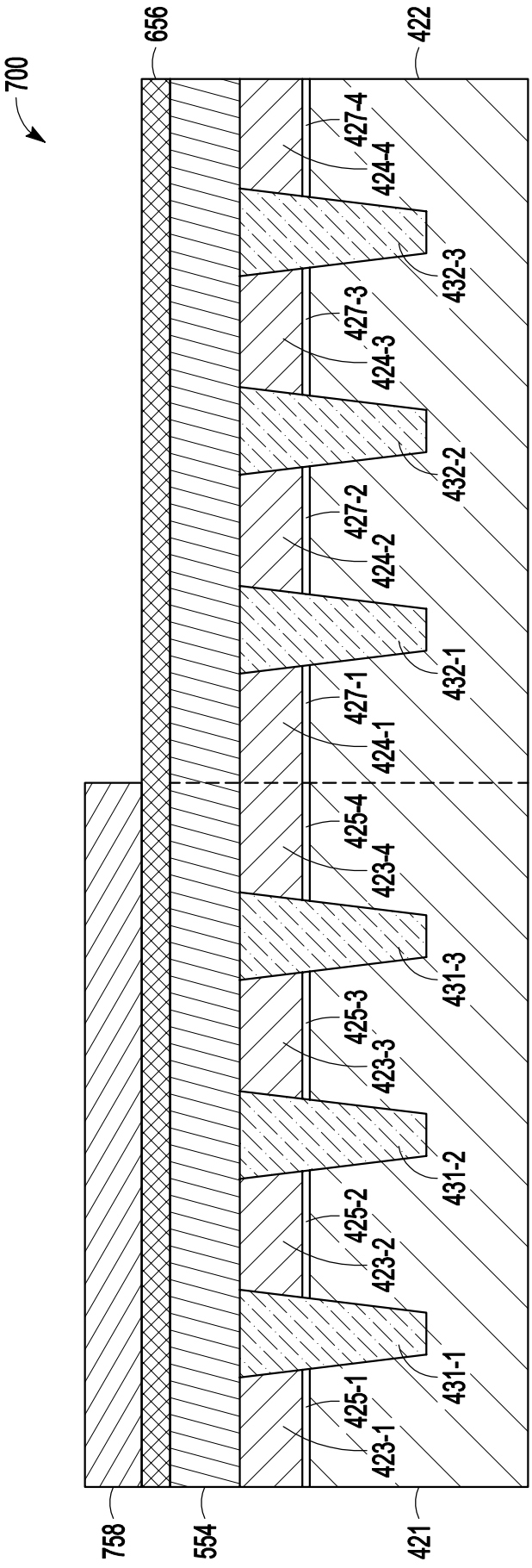

700
656
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
758
554
421

FIG. 7

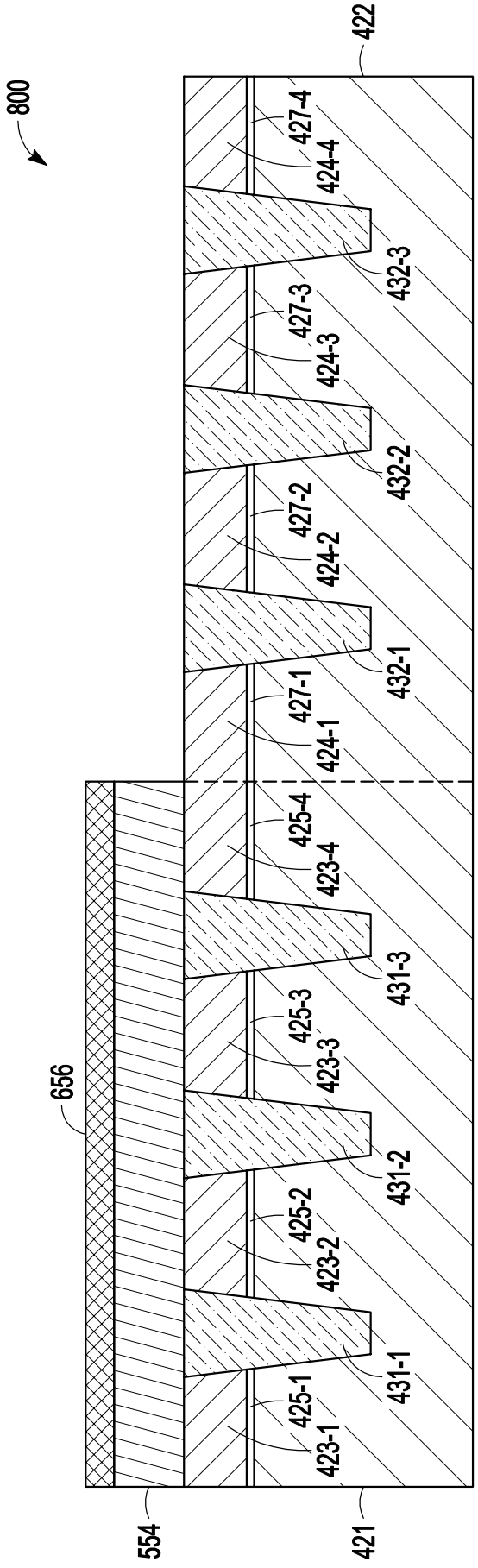

800
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
656
554
421

FIG. 8

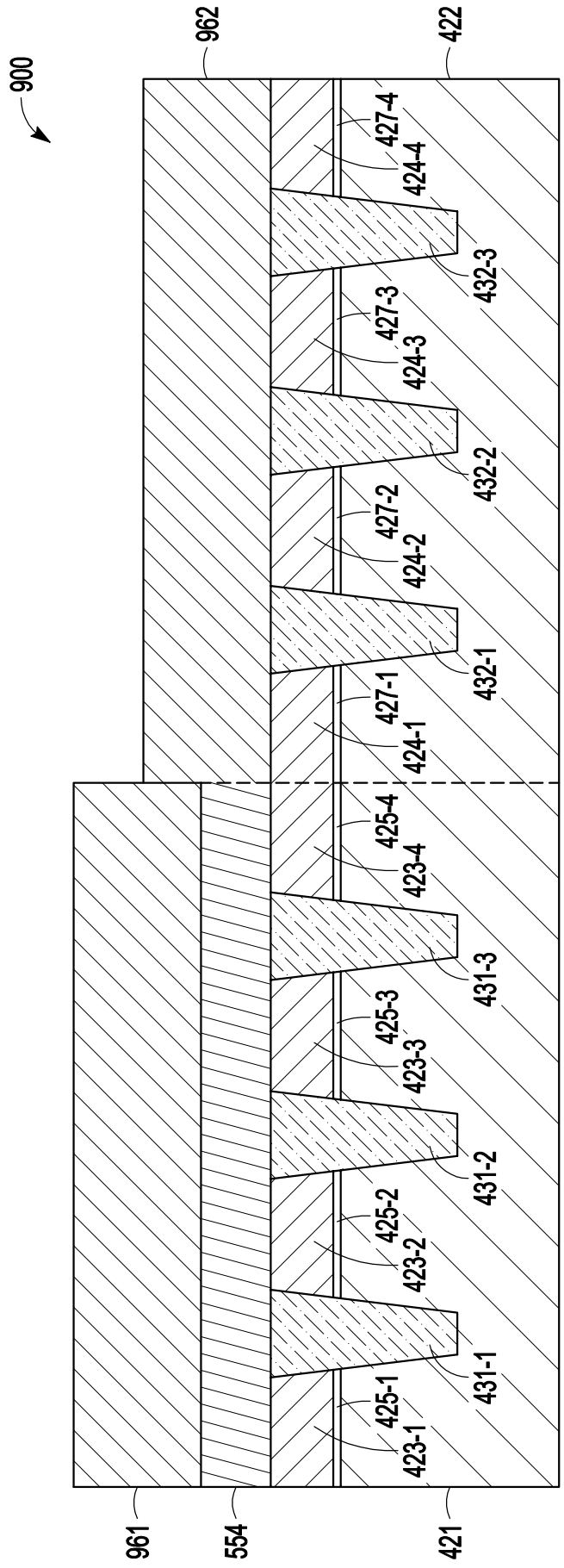

900
962
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
961
554
421

FIG. 9

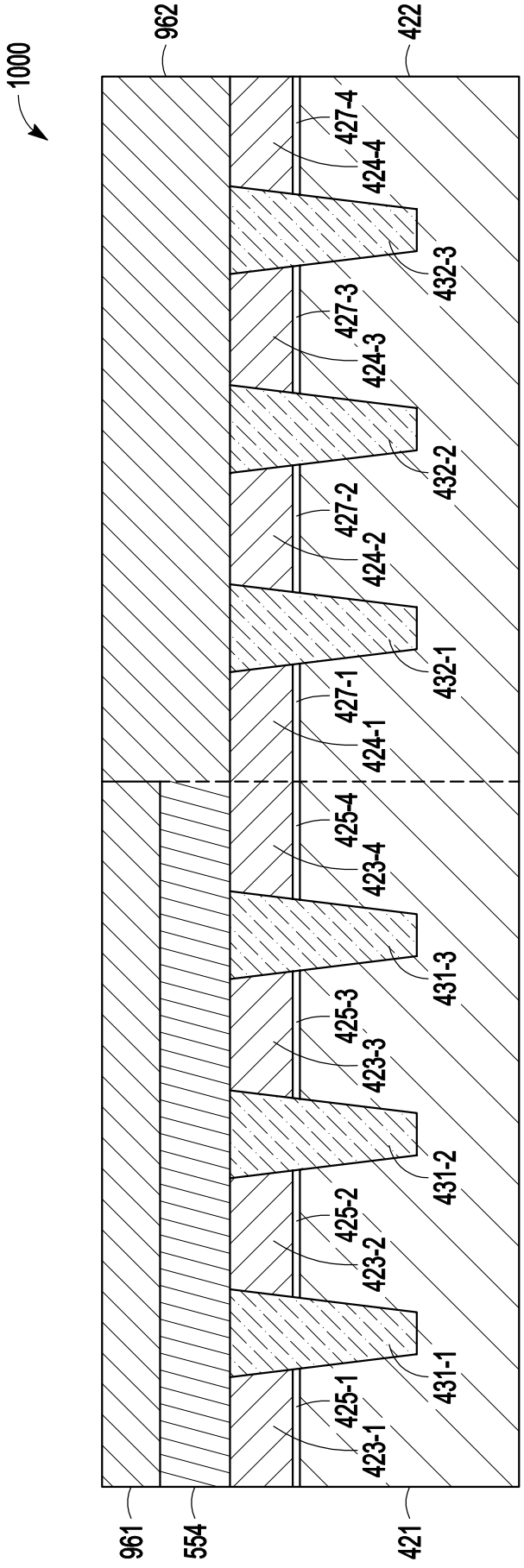

1000
962
422
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
961
554
421

FIG. 10

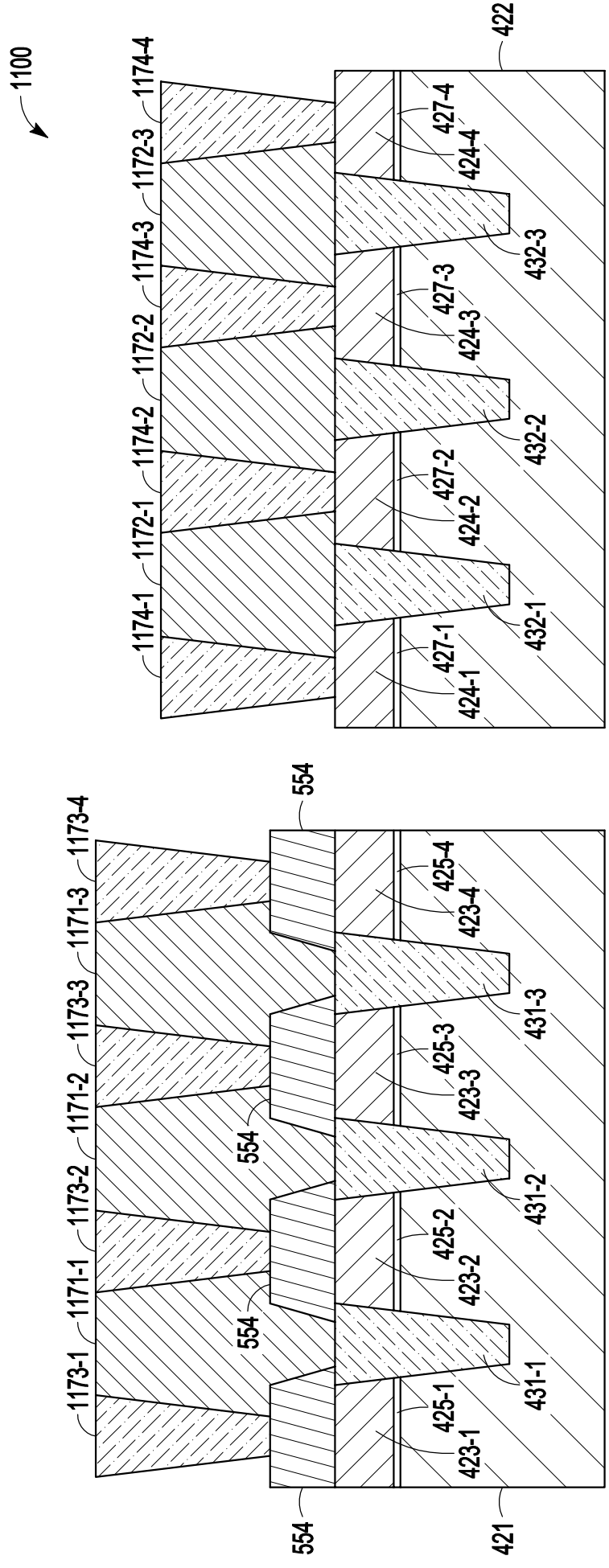

1100
422
1174-4
1172-3
1174-3
1172-2
1174-2
1172-1
1174-1
427-4
424-4
432-3
427-3
424-3
432-2
427-2
424-2
432-1
427-1
424-1
554
1173-4
1171-3
1173-3
1171-2
1173-2
1171-1
1173-1
425-4
423-4
431-3
425-3
423-3
431-2
425-2
423-2
431-1
425-1
423-1
421

FIG. 11

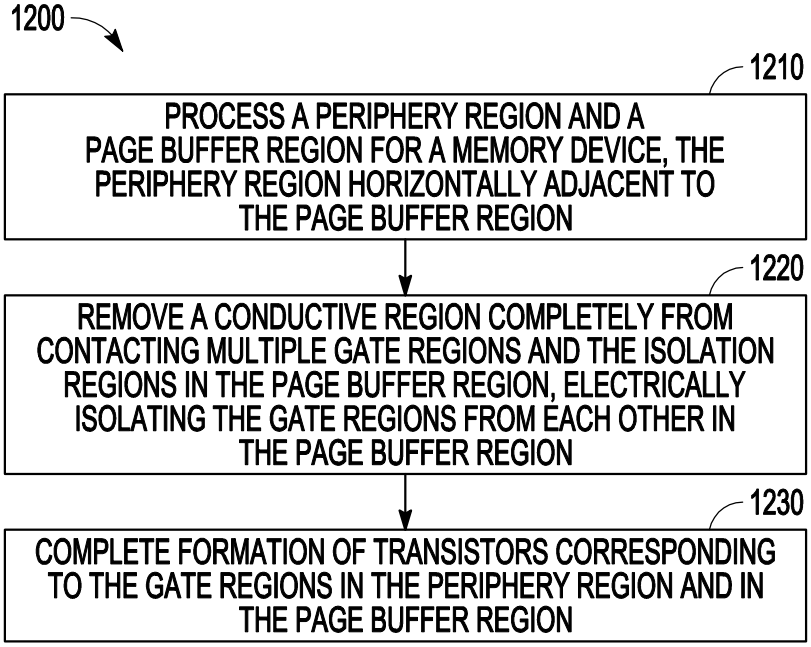

1200
1210
PROCESS A PERIPHERY REGION AND A PAGE BUFFER REGION FOR A MEMORY DEVICE, THE PERIPHERY REGION HORIZONTALLY ADJACENT TO THE PAGE BUFFER REGION
1220
REMOVE A CONDUCTIVE REGION COMPLETELY FROM CONTACTING MULTIPLE GATE REGIONS AND THE ISOLATION REGIONS IN THE PAGE BUFFER REGION, ELECTRICALLY ISOLATING THE GATE REGIONS FROM EACH OTHER IN THE PAGE BUFFER REGION
1230
COMPLETE FORMATION OF TRANSISTORS CORRESPONDING TO THE GATE REGIONS IN THE PERIPHERY REGION AND IN THE PAGE BUFFER REGION

FIG. 12

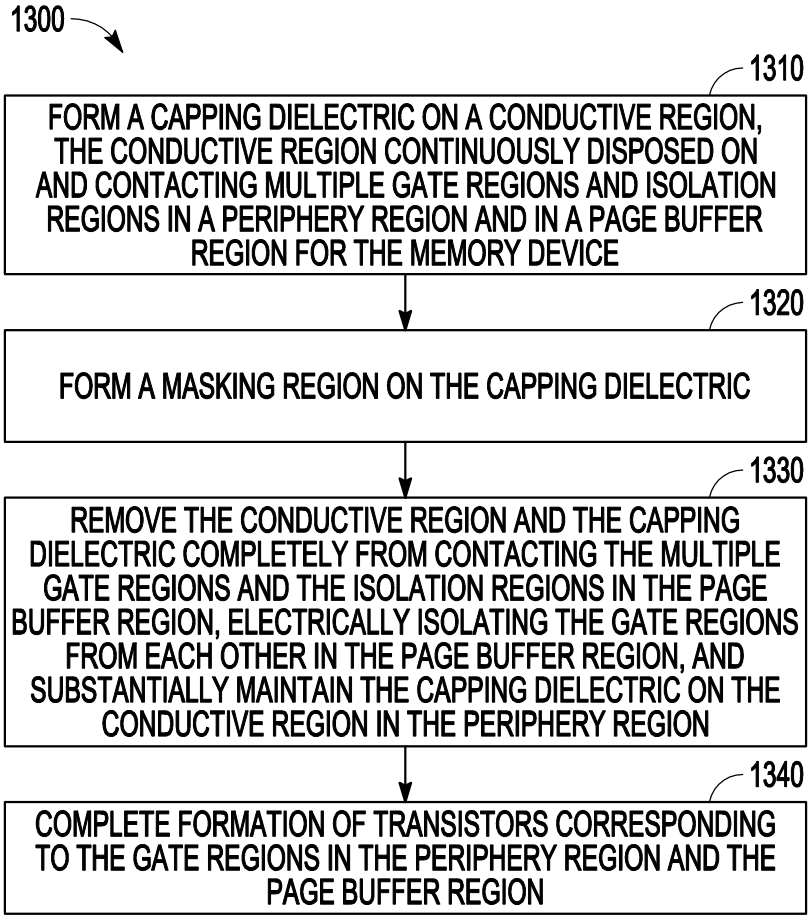

1300
1310
FORM A CAPPING DIELECTRIC ON A CONDUCTIVE REGION, THE CONDUCTIVE REGION CONTINUOUSLY DISPOSED ON AND CONTACTING MULTIPLE GATE REGIONS AND ISOLATION REGIONS IN A PERIPHERY REGION AND IN A PAGE BUFFER REGION FOR THE MEMORY DEVICE
1320
FORM A MASKING REGION ON THE CAPPING DIELECTRIC
1330
REMOVE THE CONDUCTIVE REGION AND THE CAPPING DIELECTRIC COMPLETELY FROM CONTACTING THE MULTIPLE GATE REGIONS AND THE ISOLATION REGIONS IN THE PAGE BUFFER REGION, ELECTRICALLY ISOLATING THE GATE REGIONS FROM EACH OTHER IN THE PAGE BUFFER REGION, AND SUBSTANTIALLY MAINTAIN THE CAPPING DIELECTRIC ON THE CONDUCTIVE REGION IN THE PERIPHERY REGION
1340
COMPLETE FORMATION OF TRANSISTORS CORRESPONDING TO THE GATE REGIONS IN THE PERIPHERY REGION AND THE PAGE BUFFER REGION

FIG. 13

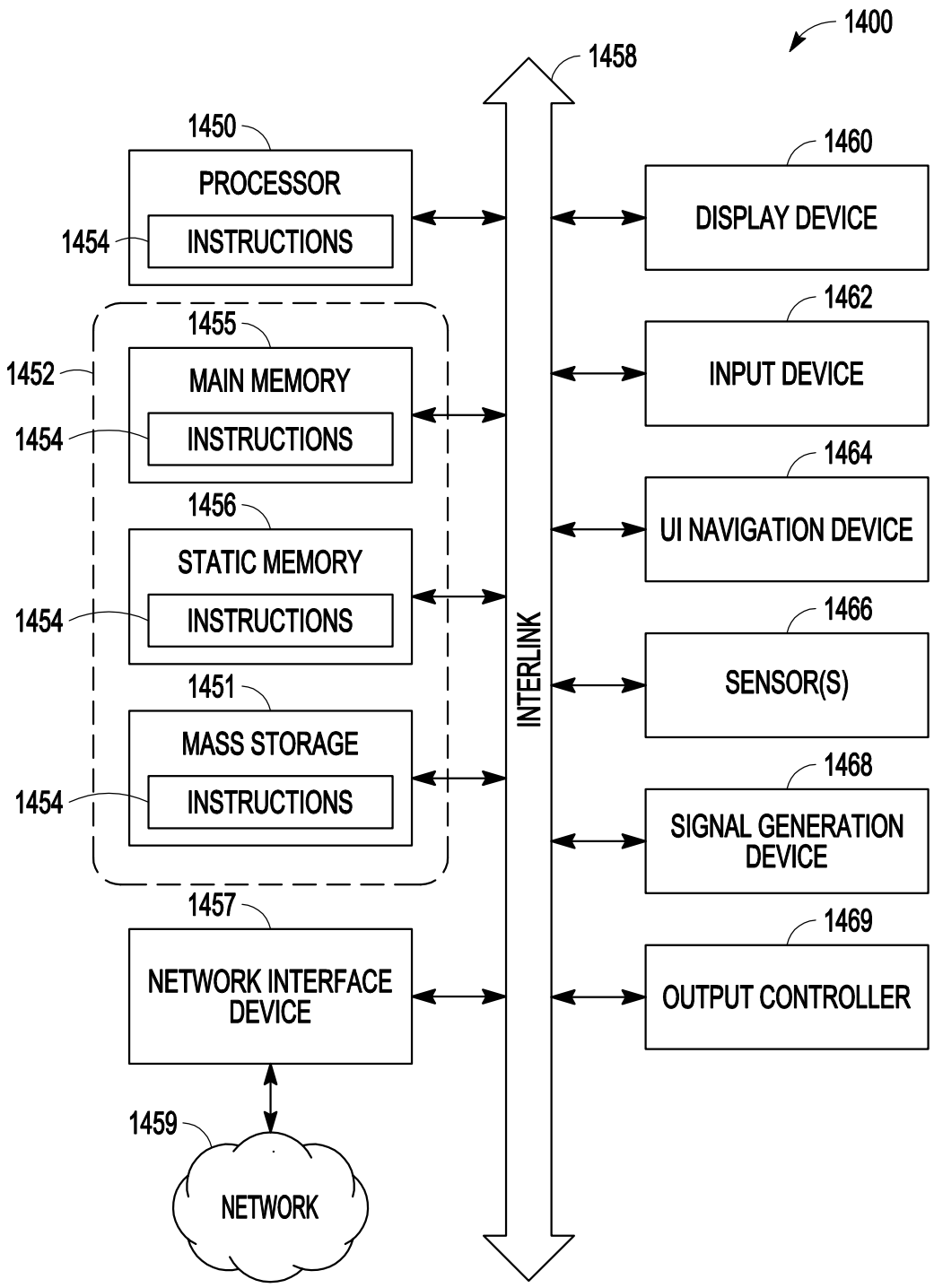

1400
1458
1450
PROCESSOR
1454
INSTRUCTIONS
1455
1452
MAIN MEMORY
1454
INSTRUCTIONS
1456
STATIC MEMORY
1454
INSTRUCTIONS
1451
MASS STORAGE
1454
INSTRUCTIONS
1457
NETWORK INTERFACE DEVICE
1459
NETWORK
INTERLINK
1460
DISPLAY DEVICE
1462
INPUT DEVICE
1464
UI NAVIGATION DEVICE
1466
SENSOR(S)
1468
SIGNAL GENERATION DEVICE
1469
OUTPUT CONTROLLER

FIG. 14