

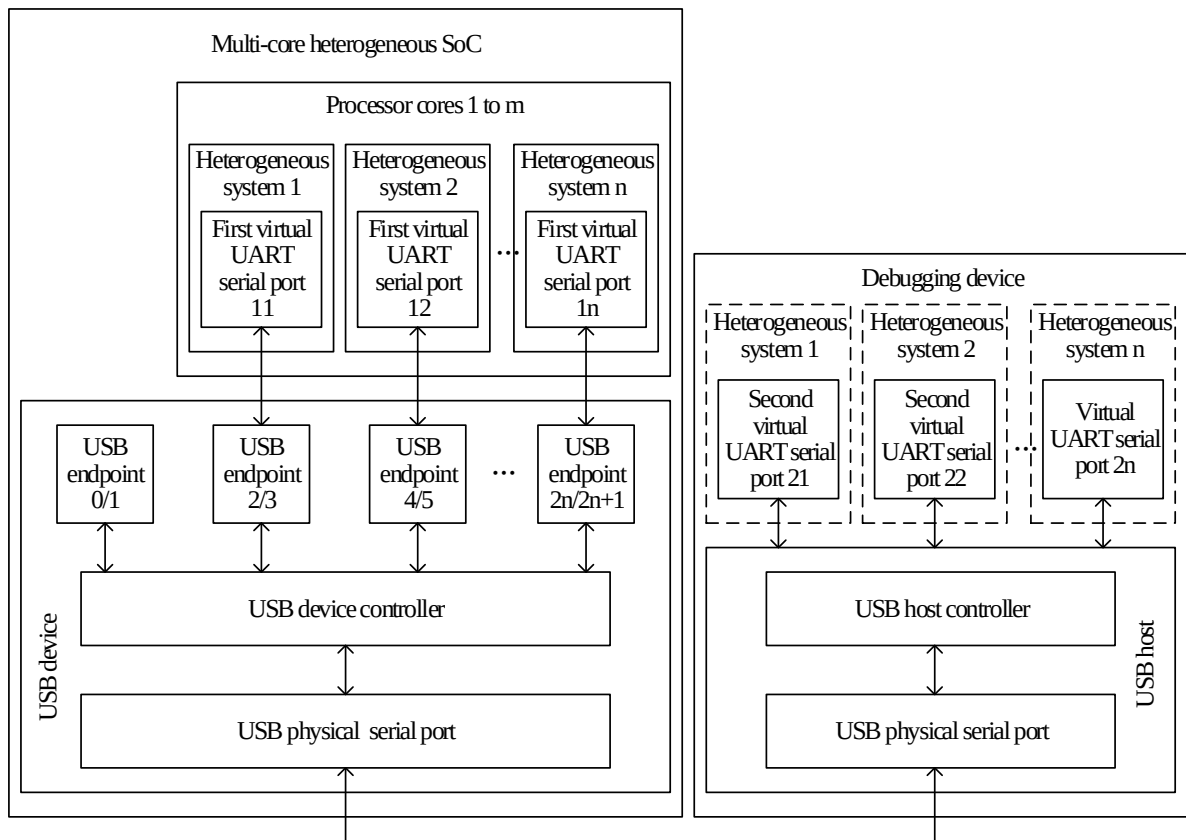


FIG. 1

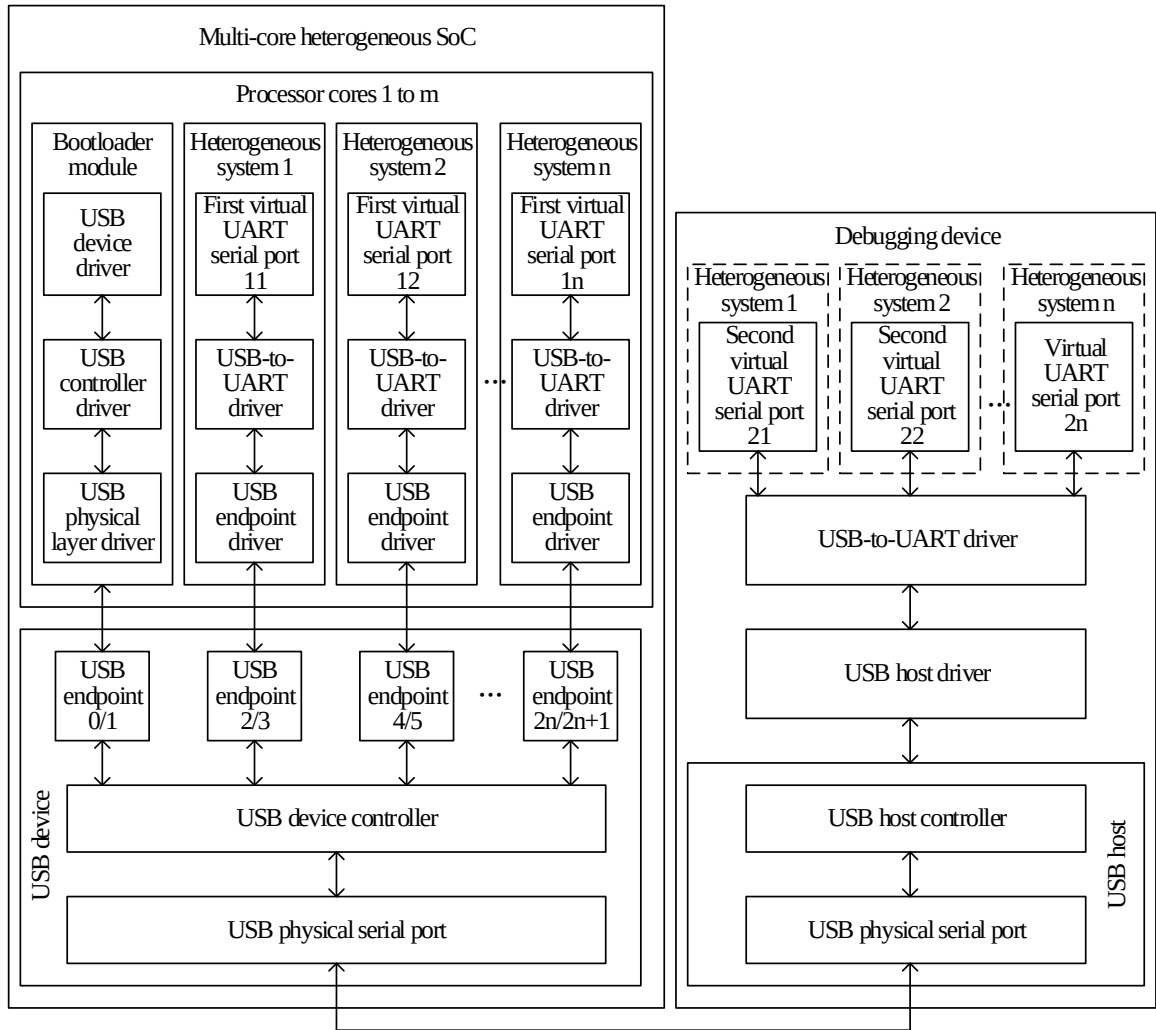


FIG. 2

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Transmitting, by a multi-core heterogeneous SoC, debugging data corresponding to a heterogeneous system with a debugging device through a USB device and a USB host based on a first virtual UART serial port in the heterogeneous system, target USB endpoints that are in the USB device and are bound to the first virtual UART serial port, and a second virtual UART serial port, in the debugging device, that is corresponding to the heterogeneous system and is bound to the target USB endpoints

FIG. 3

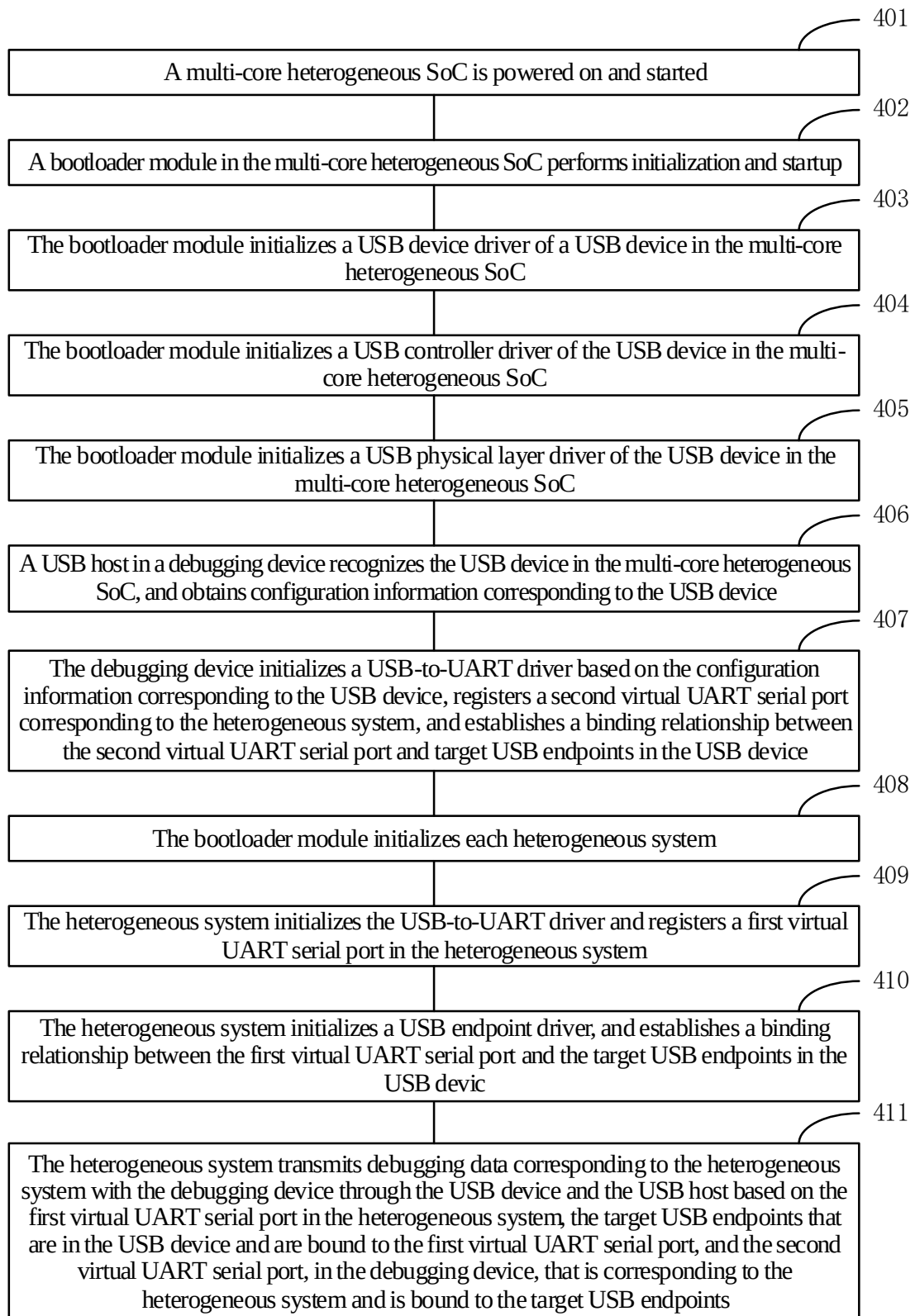


FIG. 4

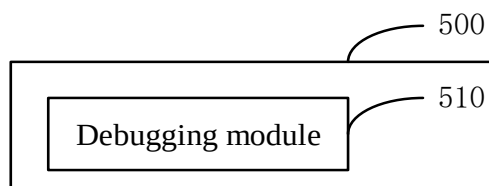


FIG. 5

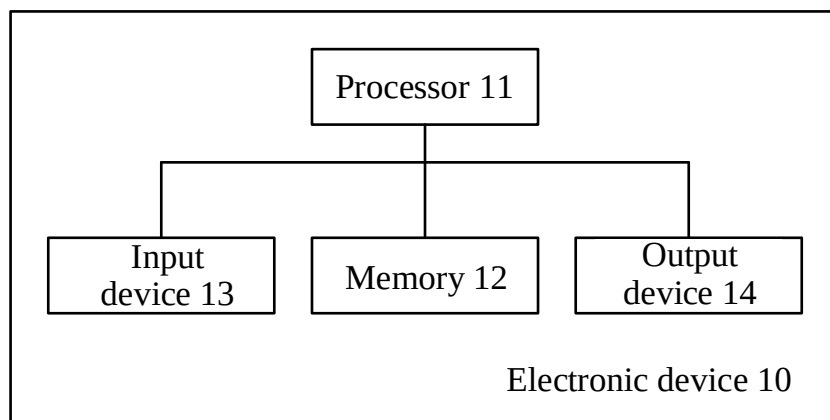


FIG. 6