ABSTRACT

Data Pipeline System and Data Encoding Method

A pipeline structure processes data in a series of stages, each of which has a data input latch (LDIN) and passes it on to the next stage in the pipeline via a data output latch (LDOUT). The stages are preferably connected to two non-overlapping clock phases (PH0, PH1). Adjacent stages are also connected via a validation line (IN_VALID, OUT_VALID) and an acceptance line (IN_ACCEPT, OUT_ACCEPT), and in some embodiments also via an extension bit line (IN_EXTN, OUT_EXTN). Input data is transferred from any stage to the following stage once every complete period of the clock signals only if the acceptance signal from that following stage is in the affirmative state. The extension bit line conveys an extension bit that separates data in the data stream into blocks. Decoding circuitry may also be included in any of the stages so that a stage only manipulates the data that is in blocks in which one or more predetermined bit patterns is decoded at the start of the block.

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