technologies.

[0008] Therefore, it would be desirable to provide a system and method that overcomes the above identified problems, and others.

SUMMARY

[0009] According to an embodiment, a flip flop circuit has a first stage and a second stage. The first stage and the second stage each have interleaved filters. The interleaved filter of the first stage comprises: a first stage delay circuit; and a first stage output buffer having a first input coupled to an input of the flip flop circuit and a second input coupled to an output of the first stage delay circuit.

[0010] According to another embodiment, a flip flop circuit has a first stage. The first stage has a first stage interleaved filter having a first stage interleaved filter input and a first stage interleaved filter output; and a first stage feedback inverter coupled to ~~a~~ the first stage interleaved filter input and to ~~a~~ the first stage interleaved filter output. The flip flop circuit has a second stage. The second stage has a second stage interleaved filter having a second stage interleaved filter input and a second stage interleaved filter

output; and a second stage feedback inverter coupled to ~~a~~ the second stage interleaved filter input and to ~~a~~ the second stage interleaved filter output. A switching device is coupled between the first stage and the second stage. The first stage interleaved filter comprises: a first stage delay circuit, wherein the first stage delay circuit is a selectable delay; and a first stage output buffer coupled to the first stage delay circuit, wherein the first stage output buffer comprises a plurality of transistors, wherein the plurality of transistors are interleaved.

[0011] According to yet another embodiment, a multi-stage flip flop circuit has a first stage interleaved filter coupled to an input of the multi-stage flip flop. A first stage feedback inverter is coupled to the input of the multi-stage flip flop and to a first stage interleaved filter output. A

second stage interleaved filter is coupled to the first stage interleaved filter output. A second stage feedback inverter is coupled to the first stage interleaved filter output and to a second stage interleaved filter output. A switching device is coupled between the first stage and the second stage. The first stage interleaved filter has a delay circuit and the second stage interleaved filter has a selectable delay circuit.

[0012] Further, the disclosure comprises embodiments according to the following clauses:

[0013] Clause 1. A flip flop circuit, comprising: a first stage; and a second stage, wherein the first stage and the second stage each have interleaved filters.

[0014] Clause 2. The flip flop circuit in accordance with Clause 1, wherein the interleaved filter of the first stage comprises: a first stage delay circuit; and a first stage output buffer having a first input coupled to an input of the flip flop circuit and a second input coupled to an output of the first stage delay circuit.

[0015] Clause 3. The flip flop circuit in accordance with Clause 2, further comprising a first stage feedback inverter coupled between an output of the first stage output buffer and the input of the flip flop.

[0016] Clause 4. The flip flop circuit in accordance with Clause 2, wherein the first stage delay circuit has a fixed

delay.

[0017] Clause 5. The flip flop circuit in accordance with

What is claimed is:

1. A flip flop circuit, comprising:

a first stage; and

a second stage,

wherein the first stage and the second stage each have interleaved filters.

2. The flip flop circuit in accordance with Claim 1, wherein the interleaved filter of the first stage comprises:

a first stage delay circuit; and

a first stage output buffer having a first input coupled to an input of the flip flop circuit and a second input coupled to an output of the first stage delay circuit.

3. The flip flop circuit in accordance with Claim 2, further comprising a first stage feedback inverter coupled between an output of the first stage output buffer and the input of the flip flop.

4. The flip flop circuit in accordance with Claim 2, wherein the first stage delay circuit has a fixed delay.

5. The flip flop circuit in accordance with Claim 2, wherein the first stage delay circuit has a selectable delay.

6. The flip flop circuit in accordance with Claim 1, wherein the interleaved filter of the second stage comprises:

a second stage delay circuit; and

a second stage output buffer having a first input coupled to an input of the second stage and a second input coupled to an output of the second stage delay circuit.

7. The flip flop circuit in accordance with Claim 6, further comprising a second stage feedback inverter coupled between an output of the second stage output buffer and the input of the second stage.

8. The flip flop circuit in accordance with Claim 6, wherein the second stage delay circuit has a fixed delay.

9. The flip flop circuit in accordance with Claim 6, wherein the second stage delay circuit has a selectable delay.

10. A flip flop circuit comprising:

a first stage comprising:

a first stage interleaved filter having a first stage interleaved filter input and a first stage interleaved filter output; and

a first stage feedback inverter coupled to the first stage interleaved filter input and to the first stage interleaved filter output;

a second stage comprising:

a second stage interleaved filter having a second stage interleaved filter input and a second stage interleaved filter output; and

a second stage feedback inverter coupled to the second stage interleaved filter input and to the second stage interleaved filter output; and

a switching device coupled between the first stage and the second stage.

11. The flip flop circuit in accordance with Claim 10, wherein the first stage interleaved filter comprises:

a first stage delay circuit; and

a first stage output buffer coupled to the first stage delay circuit, wherein the first stage output buffer comprises a plurality of transistors, wherein the plurality of transistors are interleaved.

12. The flip flop circuit in accordance with Claim 11, wherein the first stage delay circuit has a fixed delay.

13. The flip flop circuit in accordance with Claim 11, wherein the first stage delay circuit has a selectable delay.

14. The flip flop circuit in accordance with Claim 10, wherein the second stage interleaved filter comprises:

a second stage delay circuit; and

a second stage output buffer coupled to the second stage delay circuit, wherein the second stage output buffer comprises a plurality of transistors, wherein the plurality of transistors are interleaved.

15. The flip flop circuit in accordance with Claim 14, wherein the second stage delay circuit has a fixed delay.

16. The flip flop circuit in accordance with Claim 14, wherein the second stage delay circuit has a selectable delay.

17. A multi-stage flip flop circuit comprising:

a first stage interleaved filter coupled to an input of the multi-stage flip flop;

a first stage feedback inverter coupled to the input of the multi-stage flip flop and to a first stage interleaved filter output;

a second stage interleaved filter coupled to the first

stage interleaved filter output;

a second stage feedback inverter coupled to the first stage interleaved filter output and to a second stage interleaved filter output; and

a switching device coupled between the first stage and the second stage.

18. The multi-stage flip flop circuit in accordance with Claim 17, wherein the first stage interleaved filter and the second stage interleaved filter each have a fixed delay circuit.

19. The multi-stage flip flop circuit in accordance with Claim 17, wherein the first stage interleaved filter and the second stage interleaved filter each have a selectable delay.

20. The multi-stage flip flop circuit in accordance with Claim 17, wherein the first stage interleaved filter has a fixed delay circuit and the second stage interleaved filter has a selectable delay circuit.

What is claimed is:

1. A flip flop circuit, comprising:

a first stage; and

a second stage,

wherein the first stage and the second stage each have interleaved filters, wherein the interleaved filter of the first stage comprises:

a first stage delay circuit; and

a first stage output buffer having a first input coupled to an input of the flip flop circuit and a second input coupled to an output of the first stage delay circuit.

2. The flip flop circuit in accordance with claim 1, further comprising a first stage feedback inverter coupled between an output of the first stage output buffer and the input of the flip flop.

3. The flip flop circuit in accordance with claim 1, wherein the first stage delay circuit has a fixed delay.

4. The flip flop circuit in accordance with claim 1, wherein the first stage delay circuit has a selectable delay.

5. The flip flop circuit in accordance with claim 1, wherein the interleaved filter of the second stage comprises:

a second stage delay circuit; and

a second stage output buffer having a first input coupled to an input of the second stage and a second input coupled to an output of the second stage delay circuit.

6. The flip flop circuit in accordance with claim 5, further comprising a second stage feedback inverter coupled between an output of the second stage output buffer and the input of the second stage.

7. The flip flop circuit in accordance with claim 5, wherein the second stage delay circuit has a fixed delay.

8. The flip flop circuit in accordance with claim 5, wherein the second stage delay circuit has a selectable delay.

9. A flip flop circuit comprising:

a first stage comprising:

a first stage interleaved filter having a first stage interleaved filter input and a first stage interleaved filter output; and

a first stage feedback inverter coupled to the first stage interleaved filter input and to the first stage interleaved filter output;

a second stage comprising:

a second stage interleaved filter having a second stage interleaved filter input and a second stage interleaved filter output; and

a second stage feedback inverter coupled to the second stage interleaved filter input and to the second stage interleaved filter output; and

a switching device coupled between the first stage and the second stage;

wherein the first stage interleaved filter comprises:

a first stage delay circuit, wherein the first stage delay circuit is a selectable delay; and

a first stage output buffer coupled to the first stage delay circuit, wherein the first stage output buffer comprises a plurality of transistors, wherein the plurality of transistors are interleaved.

10. The flip flop circuit in accordance with claim 9, wherein the second stage interleaved filter comprises:

a second stage delay circuit; and

a second stage output buffer coupled to the second stage delay circuit, wherein the second stage output buffer comprises a plurality of transistors, wherein the plurality of transistors are interleaved.

11. The flip flop circuit in accordance with claim 10, wherein the second stage delay circuit has a fixed delay.

12. The flip flop circuit in accordance with claim 10, wherein the second stage delay circuit has a selectable delay.

13. A multi-stage flip flop circuit comprising:

a first stage interleaved filter coupled to an input of the multi-stage flip flop;

a first stage feedback inverter coupled to the input of the multi-stage flip flop and to a first stage interleaved filter output;

a second stage interleaved filter coupled to the first stage interleaved filter output;

a second stage feedback inverter coupled to the first stage interleaved filter output and to a second stage interleaved filter output; and

a switching device coupled between the first stage and the second stage;

wherein the first stage interleaved filter has a delay circuit and the second stage interleaved filter has a selectable delay circuit.

14. The multi-stage flip flop circuit in accordance with claim 13, wherein the first stage interleaved filter delay circuit is a selectable delay circuit.

15. The multi-stage flip flop circuit in accordance with claim 13, wherein the first stage interleaved filter delay circuit is a fixed delay circuit.