WHAT IS CLAIMED IS:

1. A decoder, the decoder comprising circuitry configured to: receive a bitstream including a coded picture, the coded picture including a first region comprising a first plurality of coding units and a second region comprising a second plurality of coding units, the first plurality of coding units having a common motion model characterizable with common motion parameters, the common motion model being one of translational motion, 4-parameter affine motion, and 6-parameter affine motion;

construct, for each of the coding units in the first plurality of coding units, a motion vector candidate list, each motion vector candidate list depending on the common motion model and comprising one or more candidate motion vectors to substantially implement the common motion parameters for each coding unit in the first plurality of coding units;

decode the first plurality of coding units of the first region using the common motion model and the one or more motion vectors of the motion vector candidate lists, whereby common motion is reconstructed in the first region;

ascertain, from the bitstream, individually determined motion vectors for each coding unit of the second plurality of coding units, adjacent coding units in the second plurality of coding units having different individually determined motion vectors, the individually determined motion vectors being translational motion vectors or control point motion vectors for 4-parameter or 6-parameter affine motion; and

decode the second plurality of coding units of the second region using the individually determined motion vectors, whereby local motion in the second region is reconstructed.

2. The decoder of claim 1, wherein the first plurality of coding units comprises a coding tree unit.

3. The decoder of claim 1, wherein the common motion model is signaled by a header of the bitstream, the header including a sequence parameter set.