FIG. 1

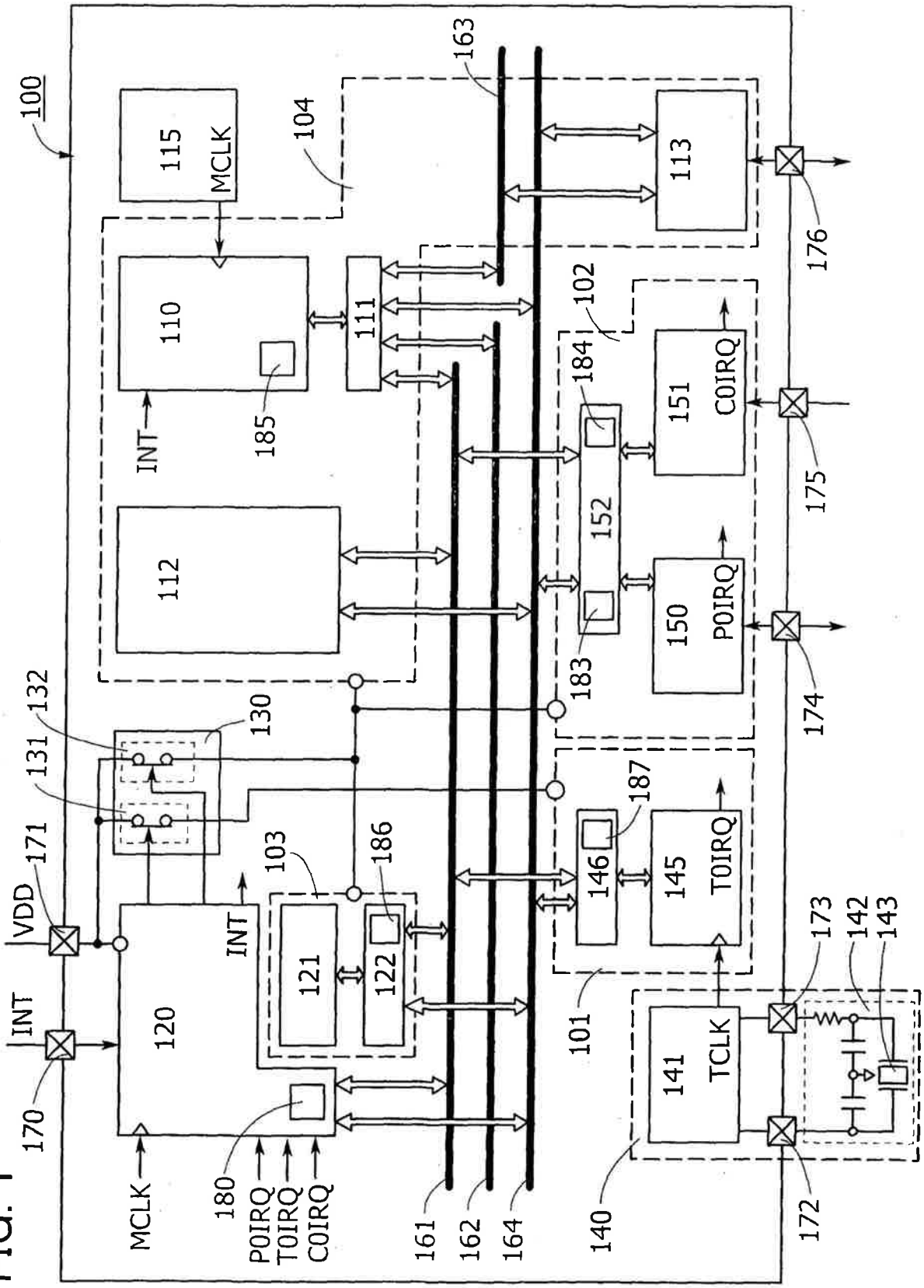

100
115
MCLK
104
163
113
176
110
111
102
184
151
COIRQ
175
185
INT
112
152
183
150
POIRQ
174
132
130
131
187
171
VDD
103
186
146
145
TOIRQ
INT
121
122
173
142
143
101
INT
120
141
TCLK
170
140
172
MCLK
180
POIRQ
TOIRQ
COIRQ
161
162
164

FIG. 2

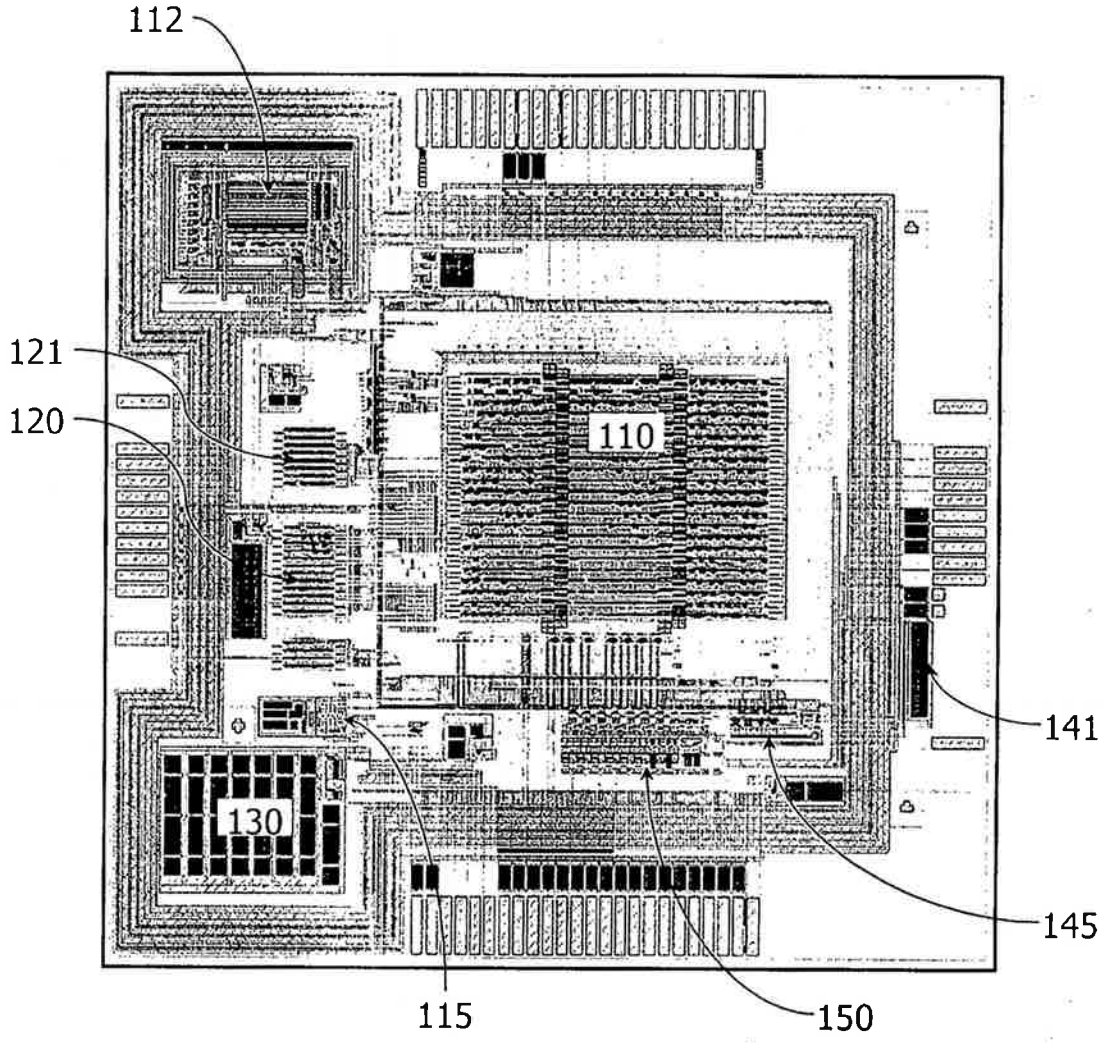


FIG. 3

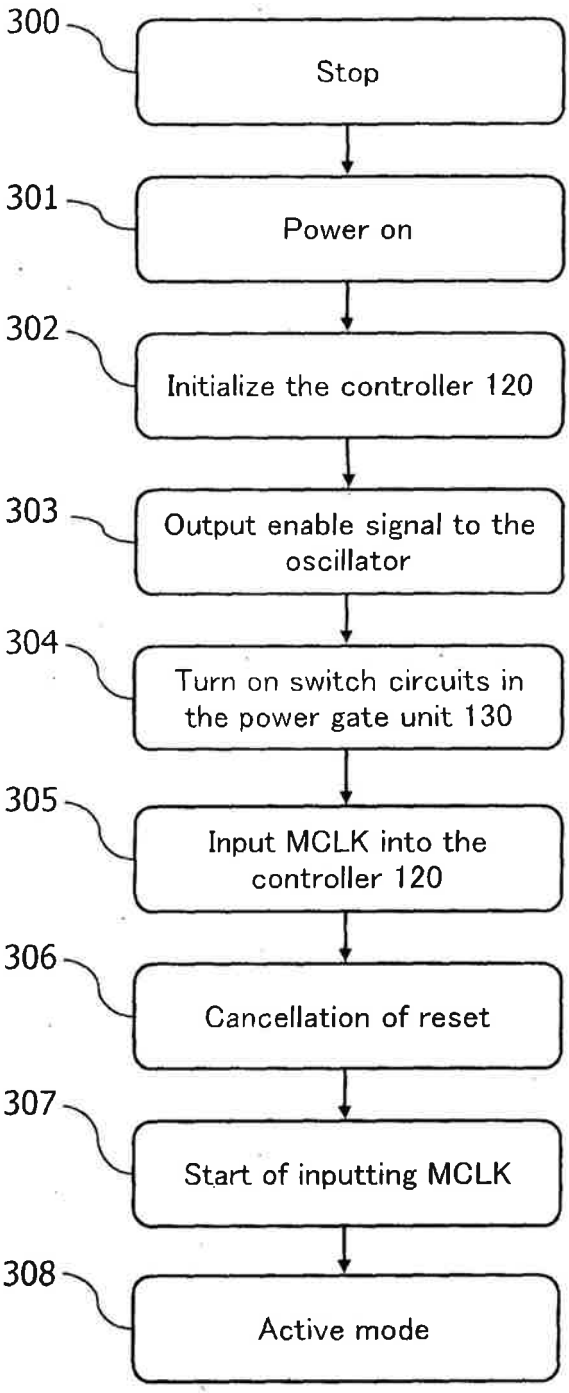

300
Stop
301
Power on
302
Initialize the controller 120
303
Output enable signal to the oscillator
304
Turn on switch circuits in the power gate unit 130
305
Input MCLK into the controller 120
306
Cancellation of reset
307
Start of inputting MCLK
308
Active mode

FIG. 4

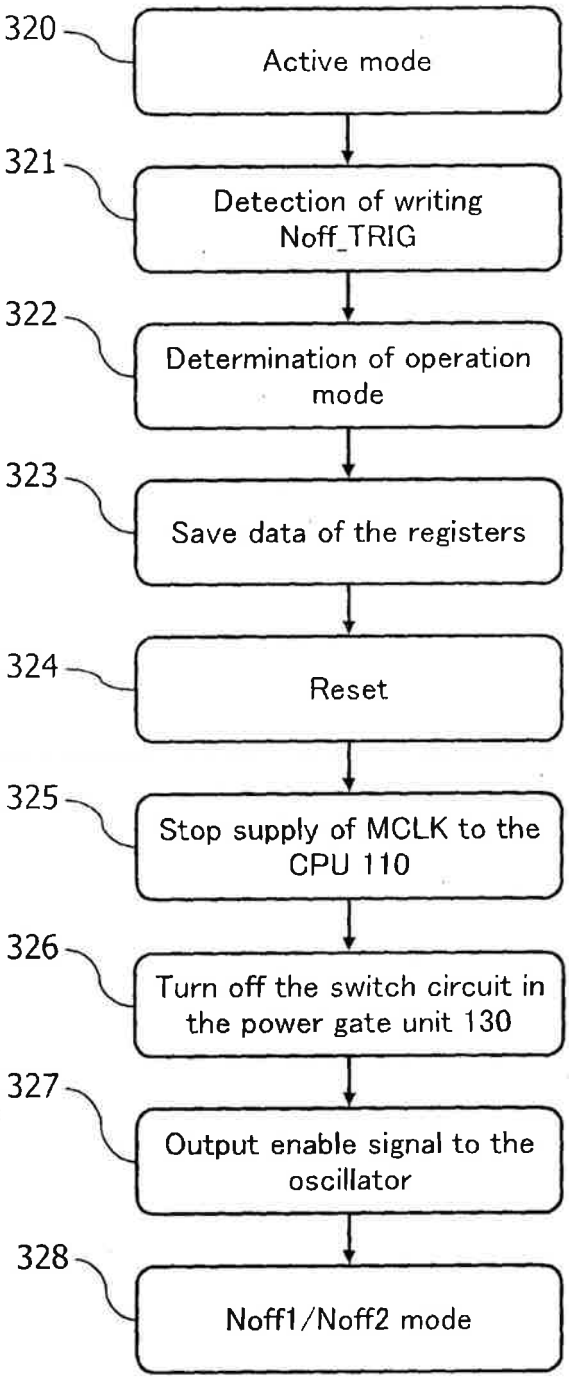

320
Active mode
321
Detection of writing Noff_TRIG
322
Determination of operation mode
323
Save data of the registers
324
Reset
325
Stop supply of MCLK to the CPU 110
326
Turn off the switch circuit in the power gate unit 130
327
Output enable signal to the oscillator
328
Noff1/Noff2 mode

FIG. 5

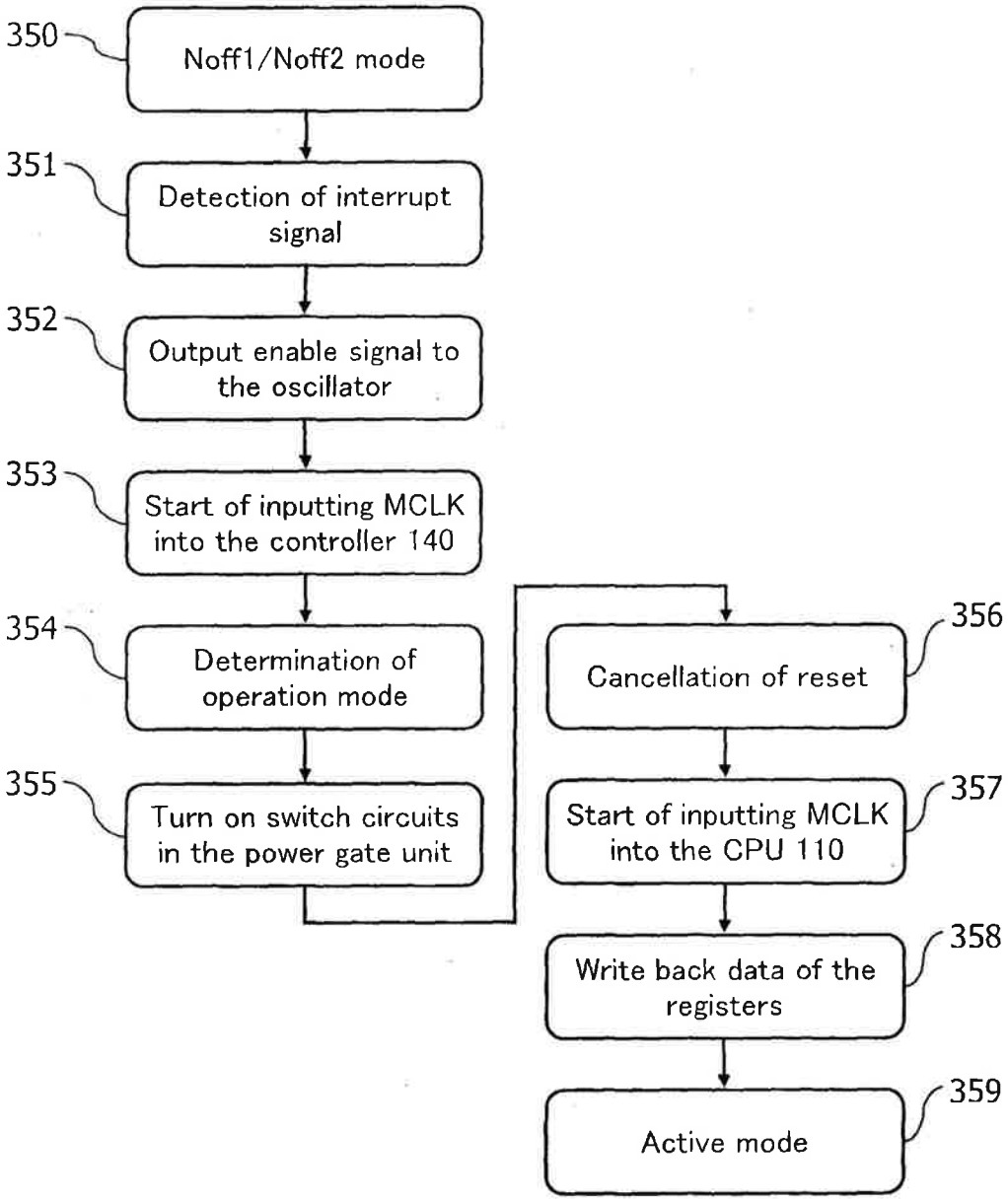

350
Noff1/Noff2 mode
351
Detection of interrupt signal
352
Output enable signal to the oscillator
353
Start of inputting MCLK into the controller 140
354
Determination of operation mode
355
Turn on switch circuits in the power gate unit
356
Cancellation of reset
357
Start of inputting MCLK into the CPU 110
358
Write back data of the registers
359
Active mode

FIG. 6

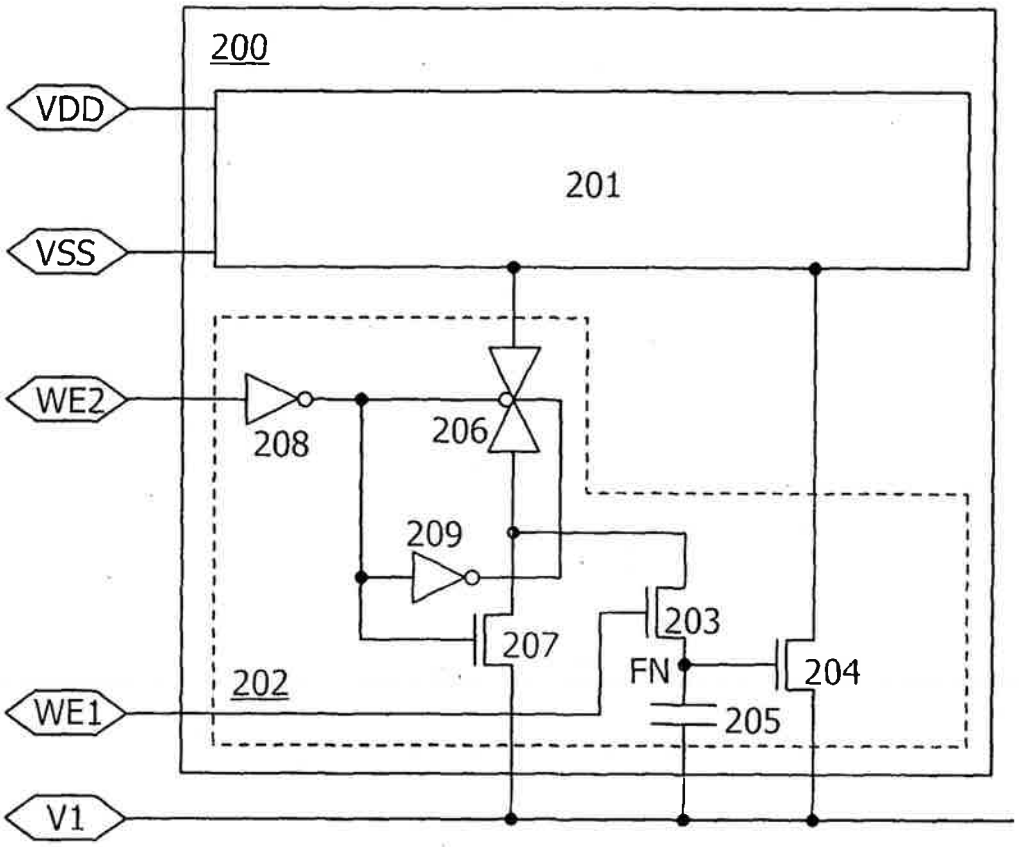


FIG. 7

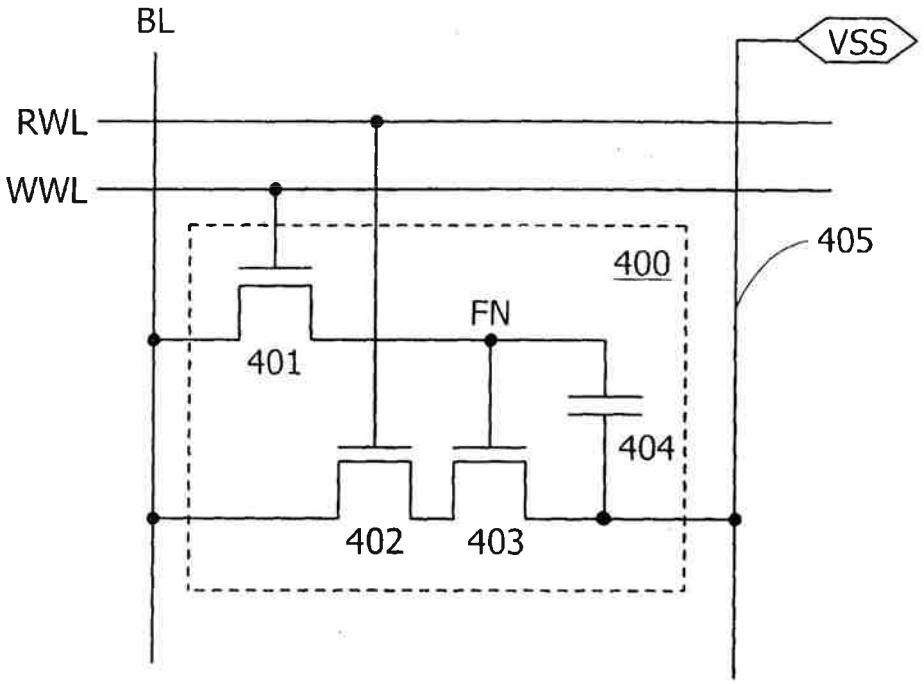


FIG. 8

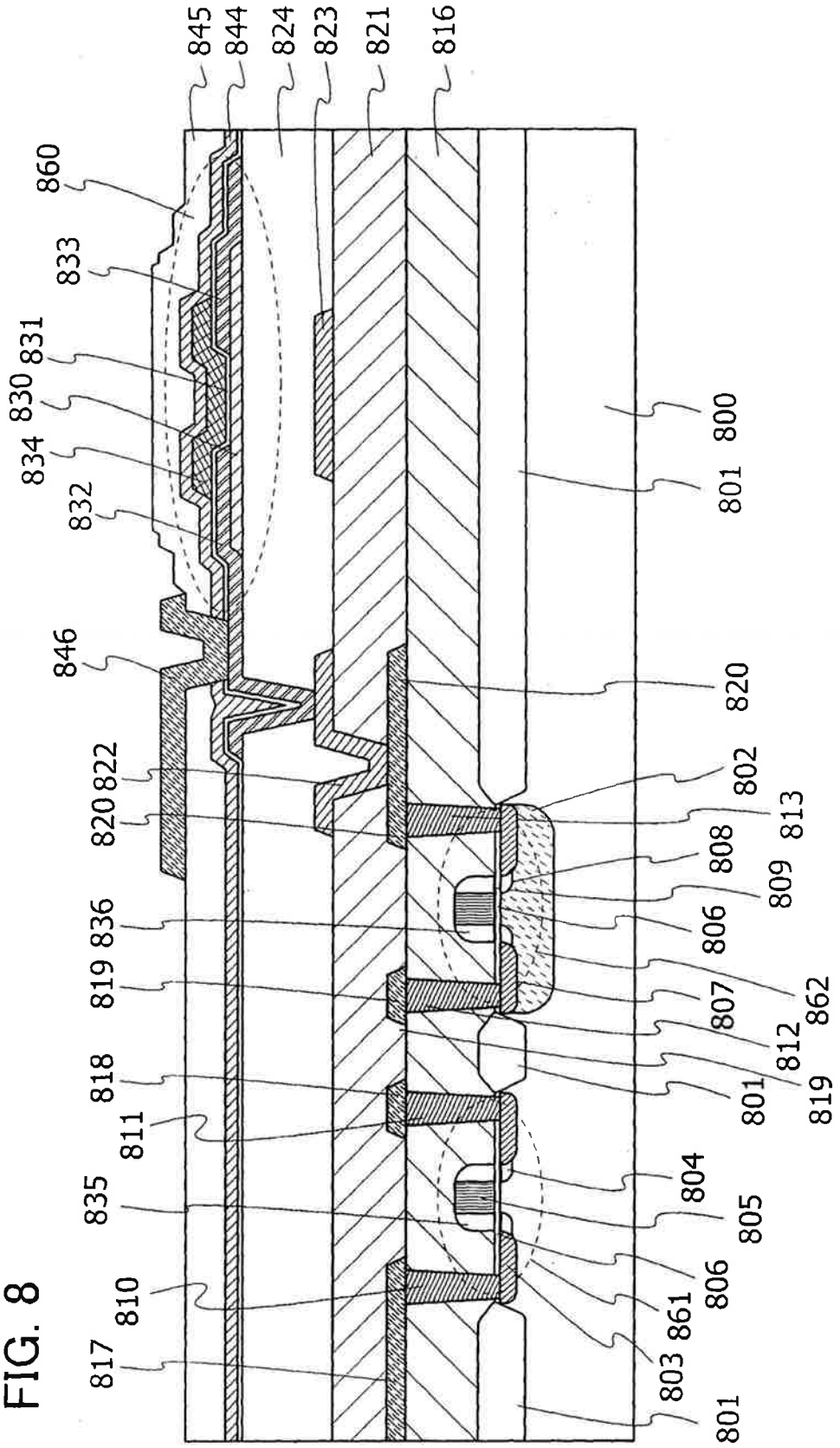

845
844
824
823
821
816
860
833
831
830
834
832
846
822
820
836
819
818
811
835
810
817
800
801
820
802
813
808
809
806
807
862
812
819
801
804
805
806
861
803
801

FIG. 9

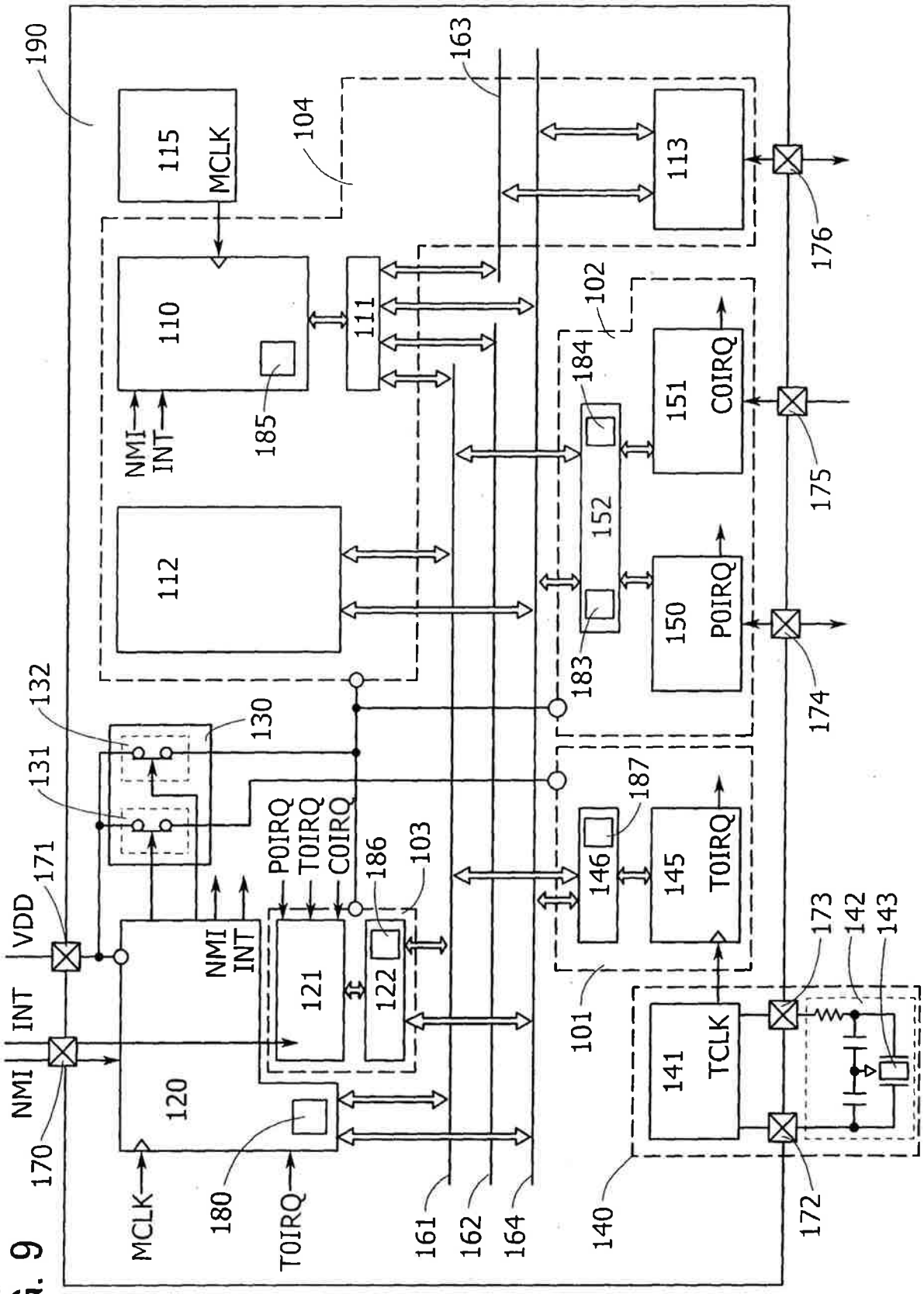

190
115
MCLK
104
163
113
176
110
111
102
184
151
COIRQ
175
NMI
INT
185
112
152
183
150
POIRQ
174
132
130
131
171
VDD
POIRQ
TOIRQ
COIRQ
186
103
187
146
145
TOIRQ
173
142
143
INT
NMI
INT
121
122
101
141
TCLK
NMI
170
120
MCLK
180
TOIRQ
161
162
164
140
172

FIG. 10

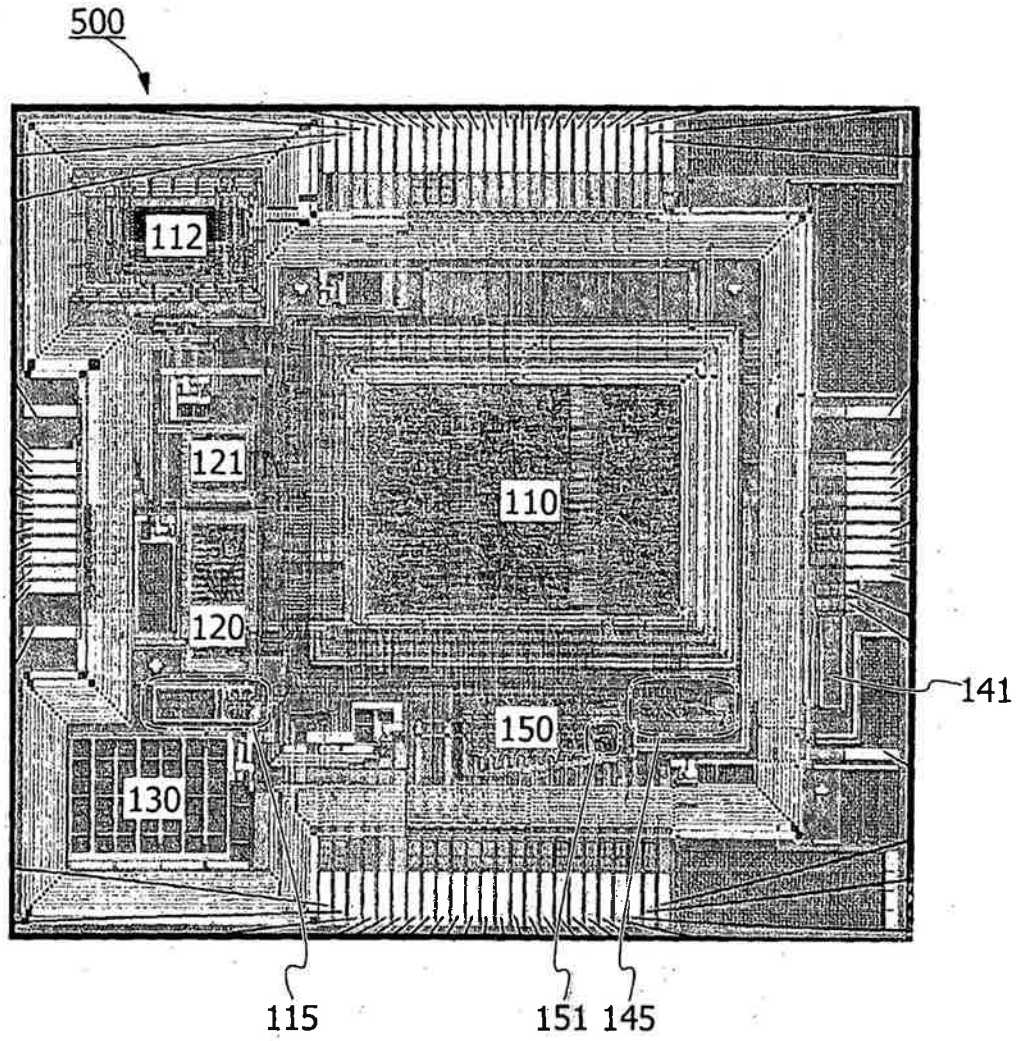


FIG. 11

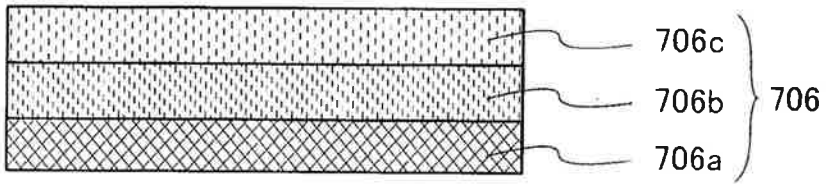


FIG. 12A

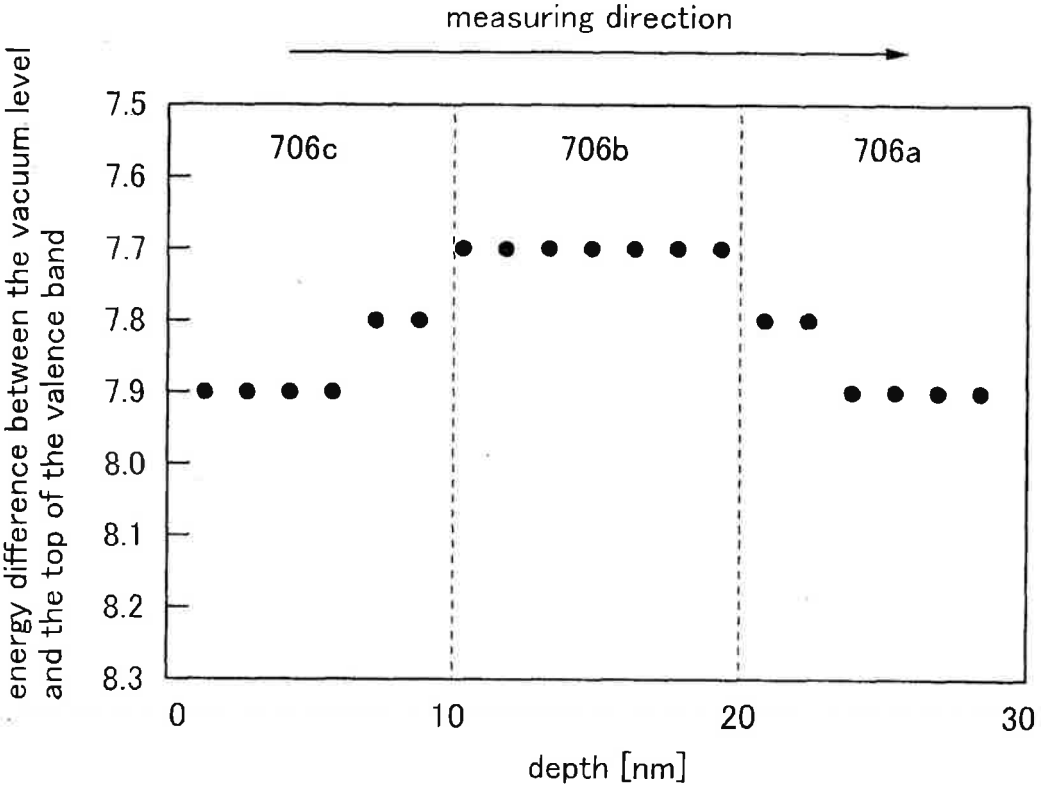


FIG. 12B

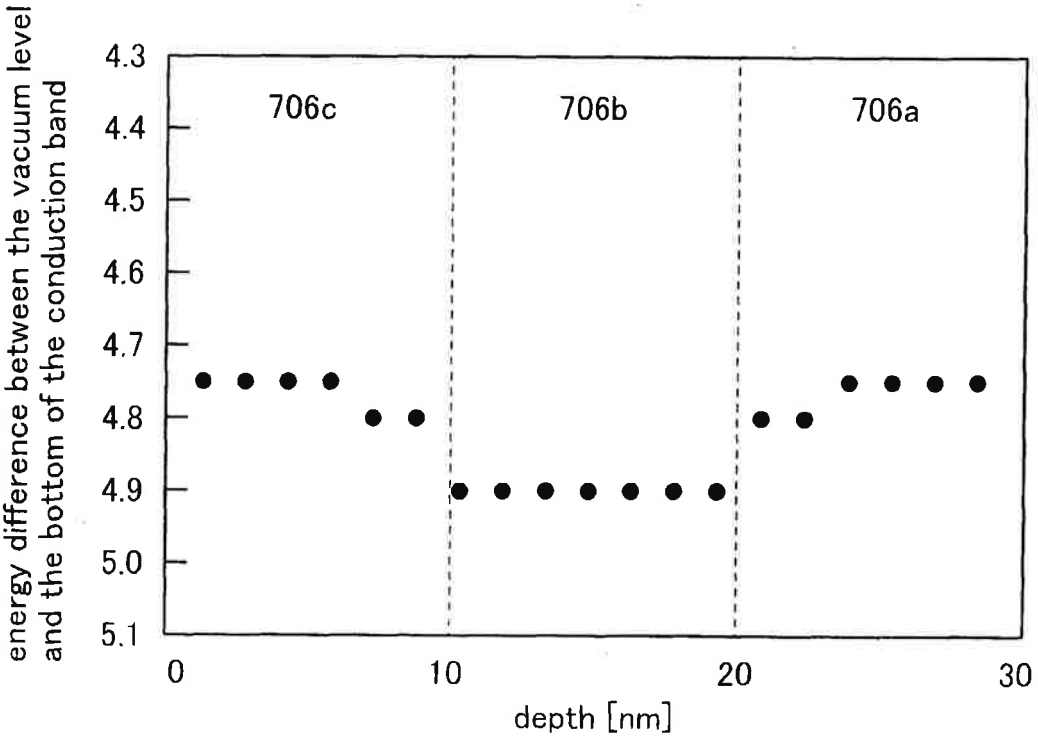


FIG. 13A

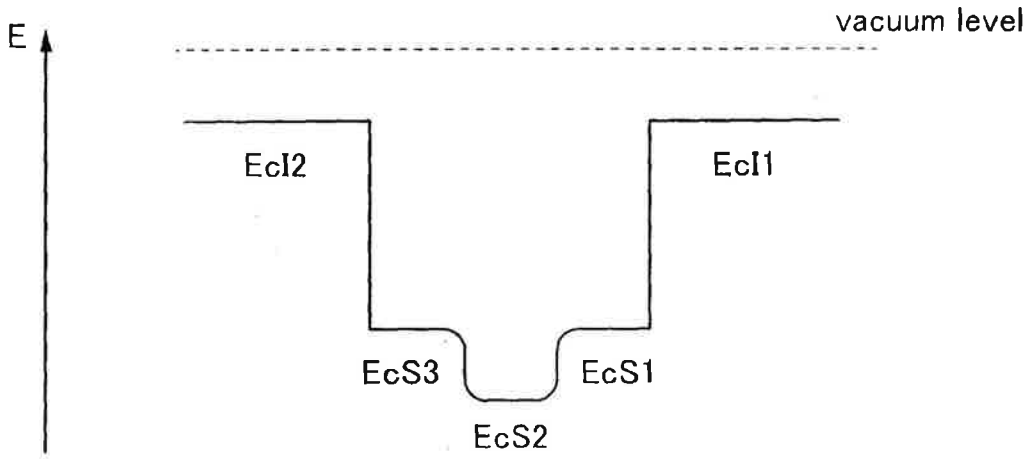


FIG. 13B

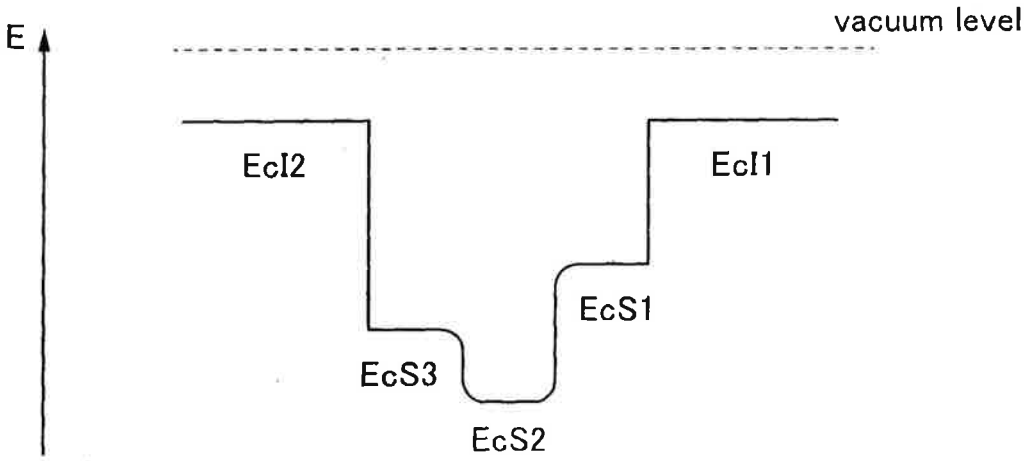


FIG. 14

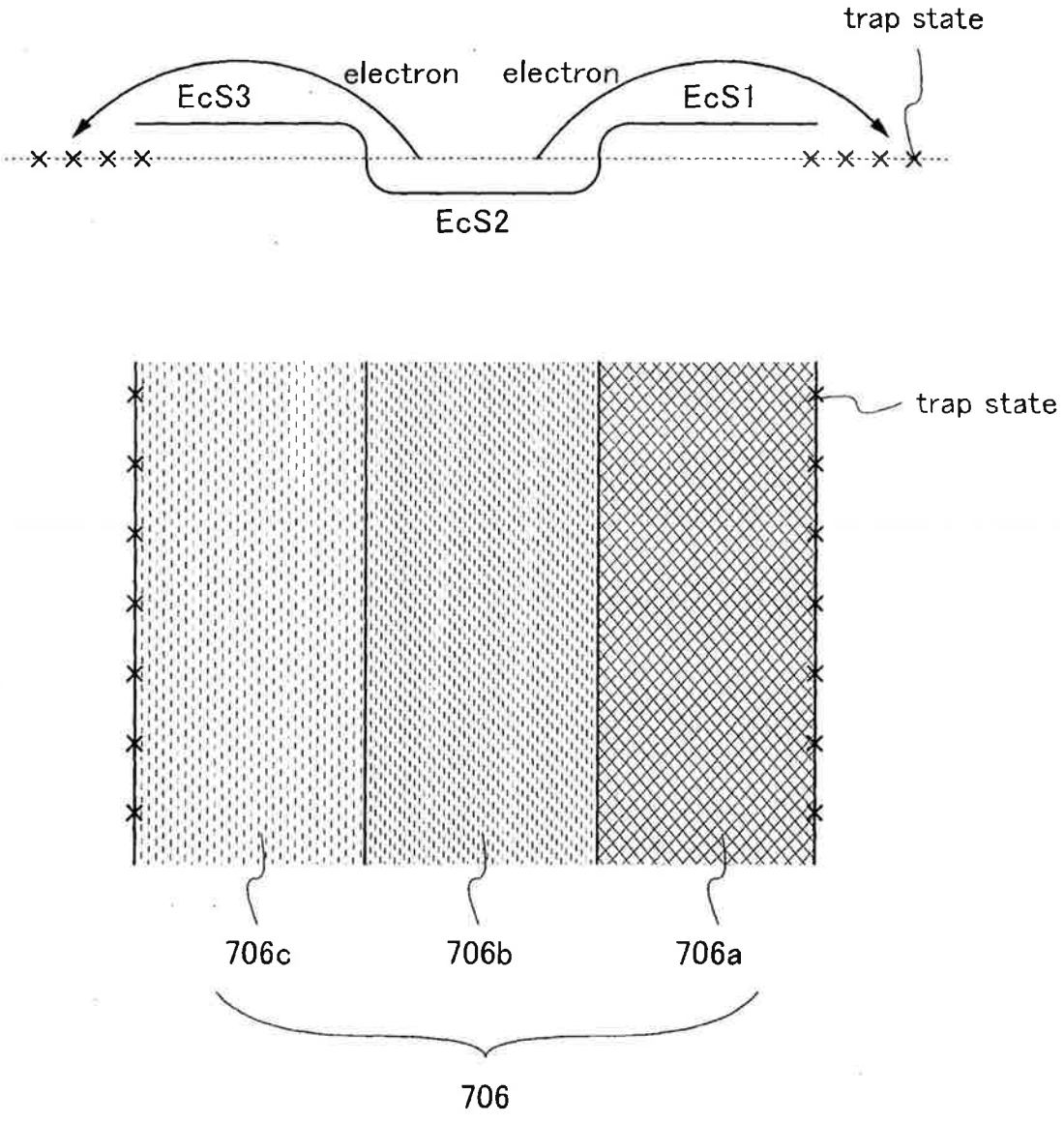

trap state
electron
electron
EcS3
EcS1
EcS2
trap state
706c
706b
706a
706

FIG. 15A

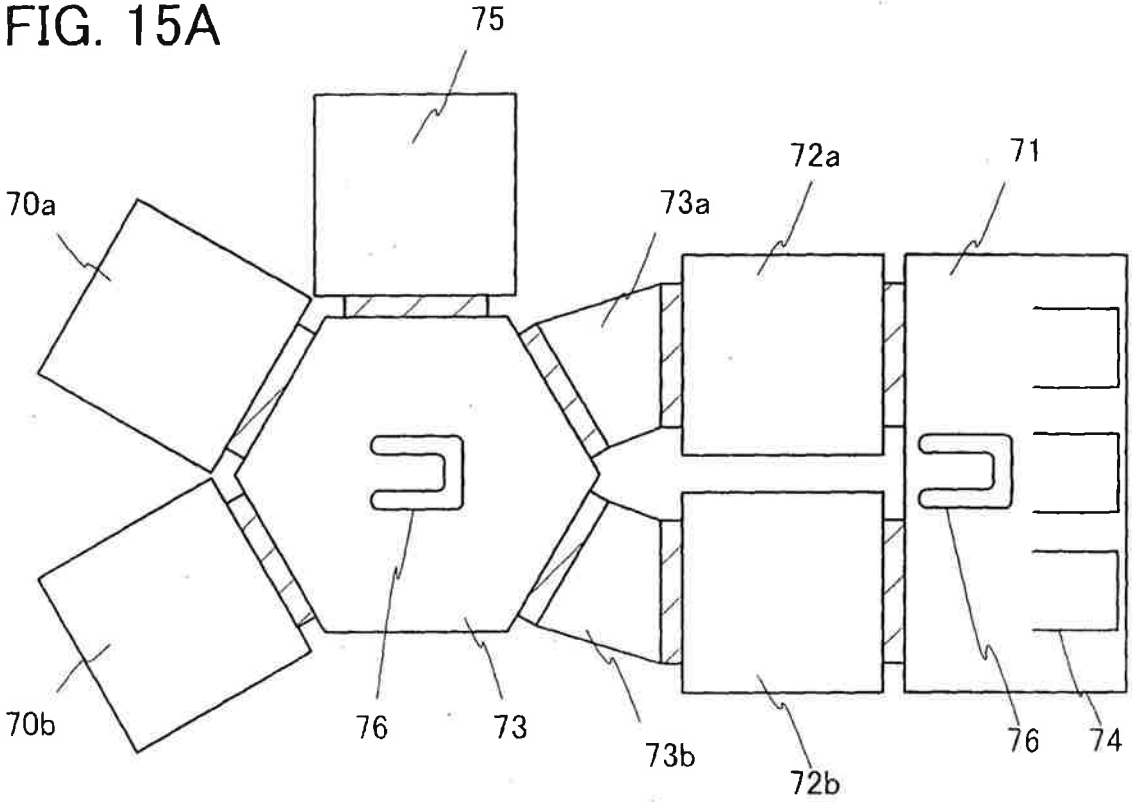


FIG. 15B

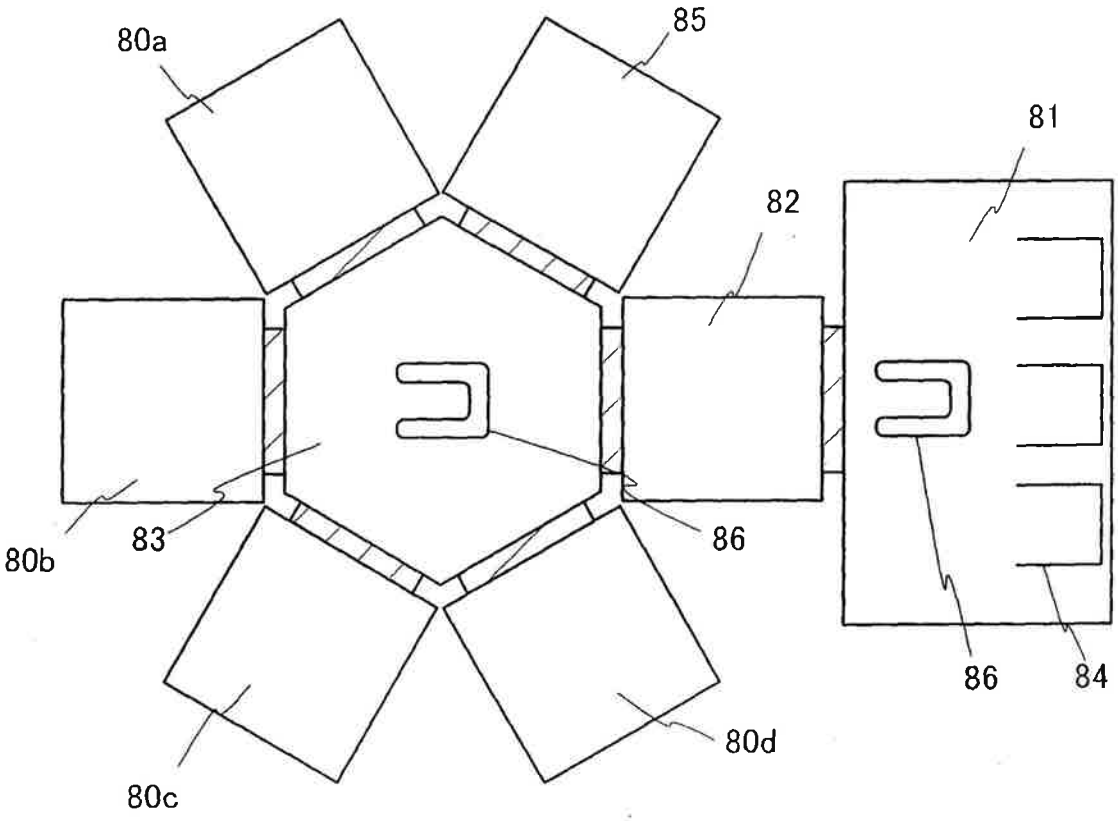


FIG. 16A

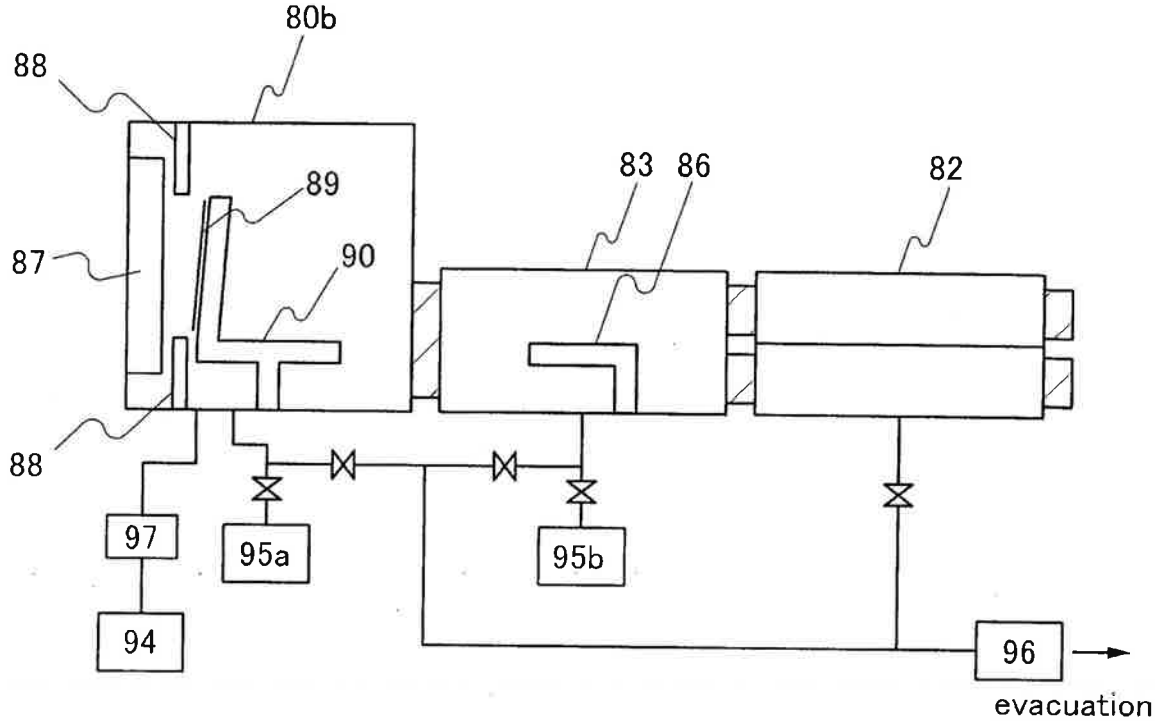


FIG. 16B

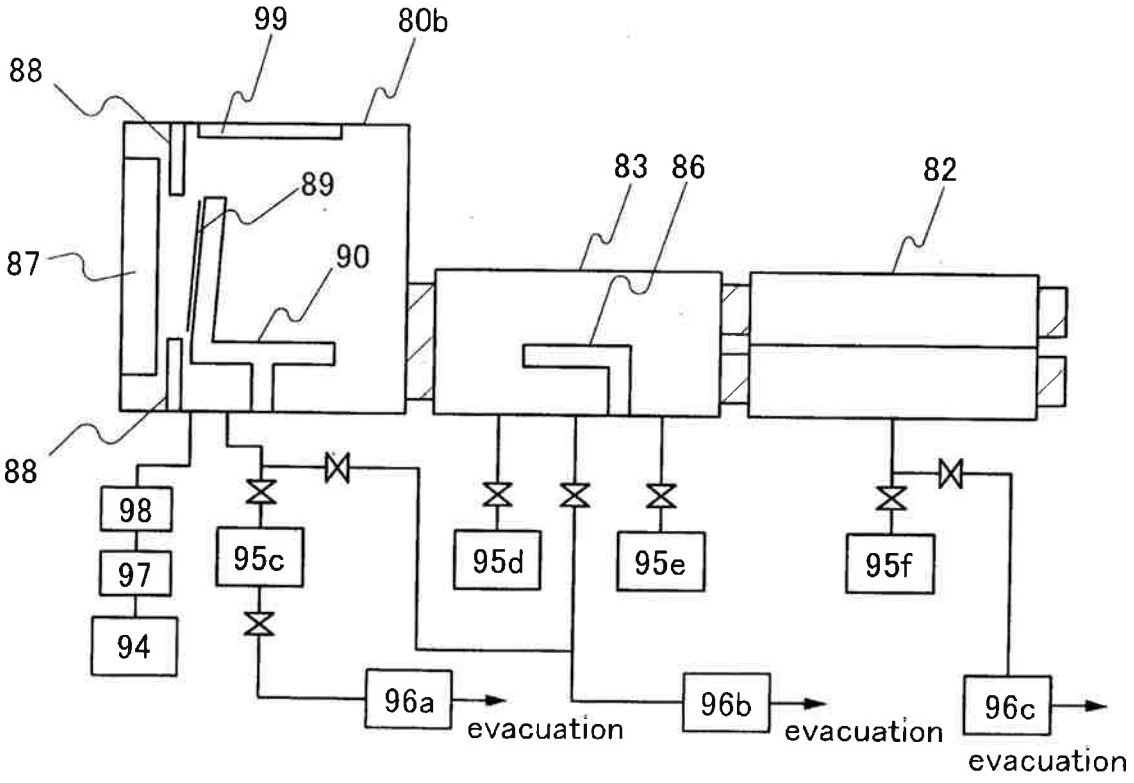


FIG. 17

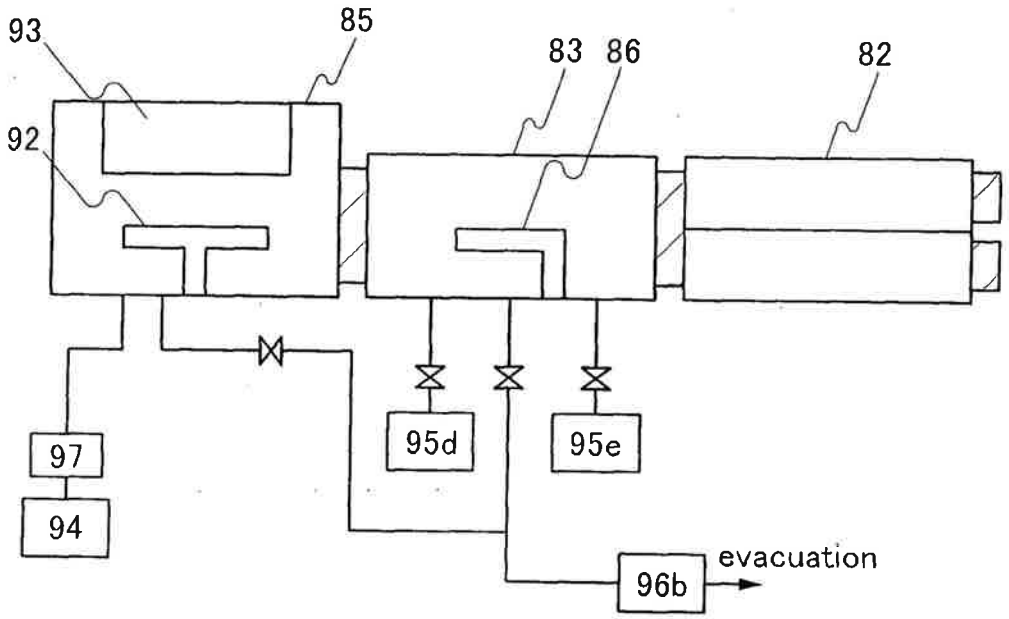


FIG. 18A

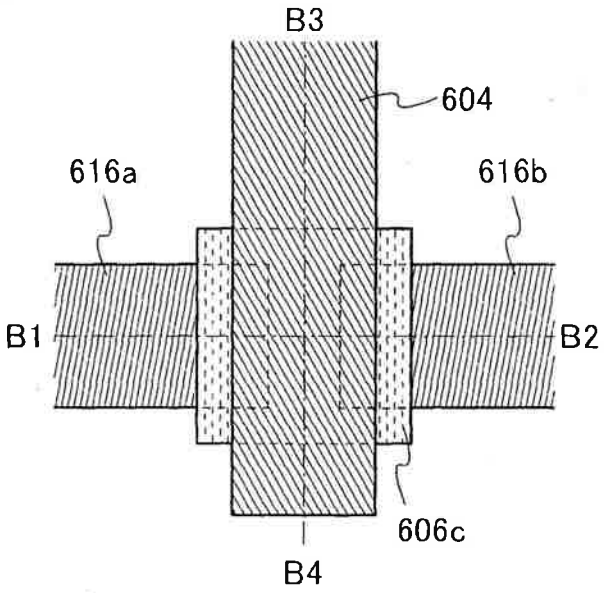


FIG. 18C

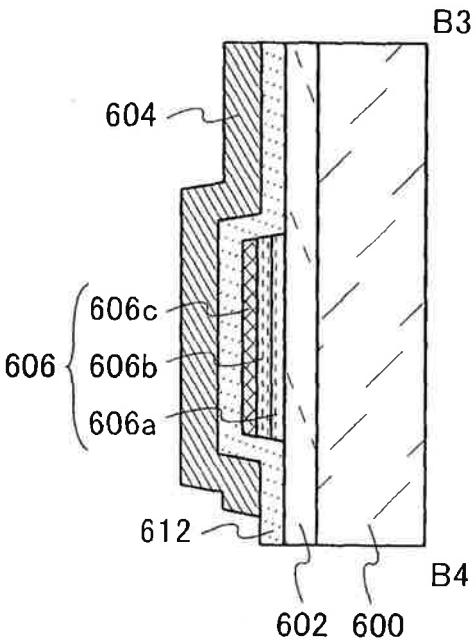


FIG. 18B

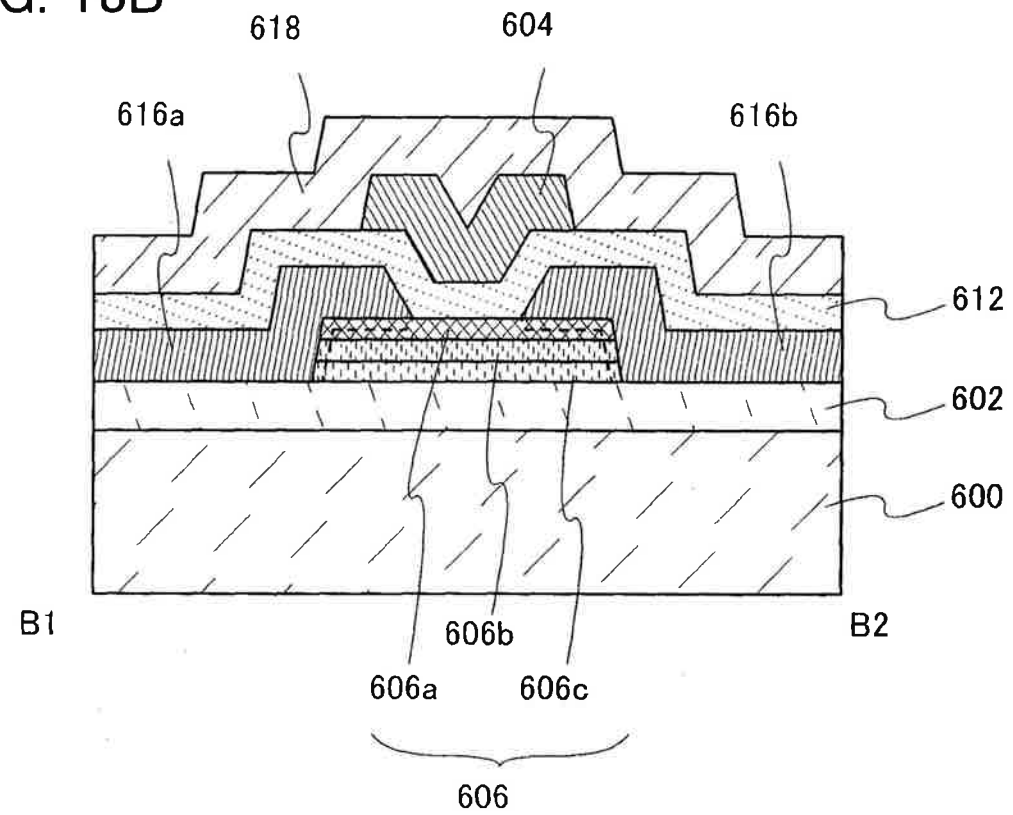


FIG. 19A

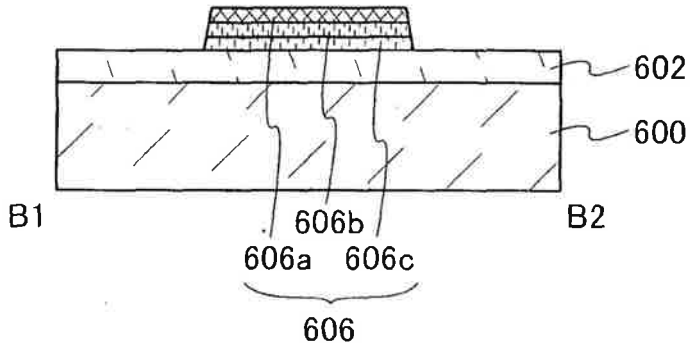


FIG. 19B

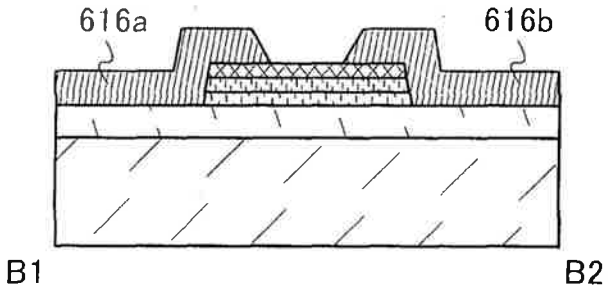


FIG. 19C

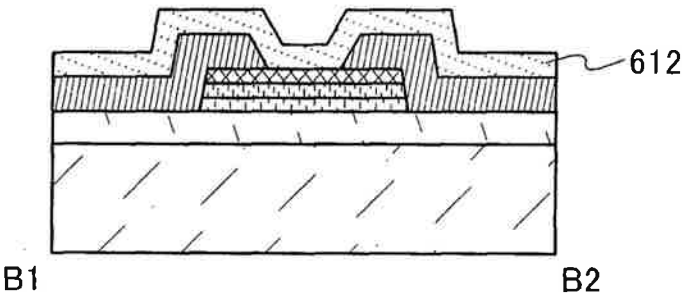


FIG. 20A

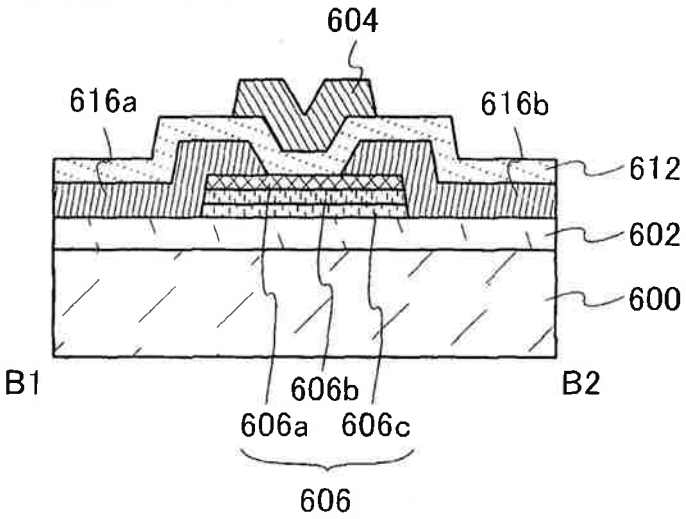


FIG. 20B

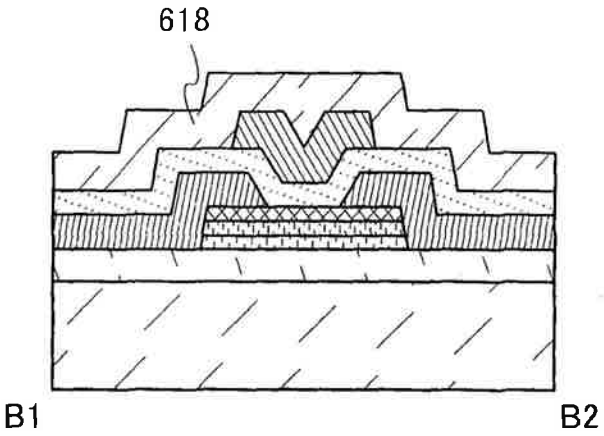


FIG. 21A

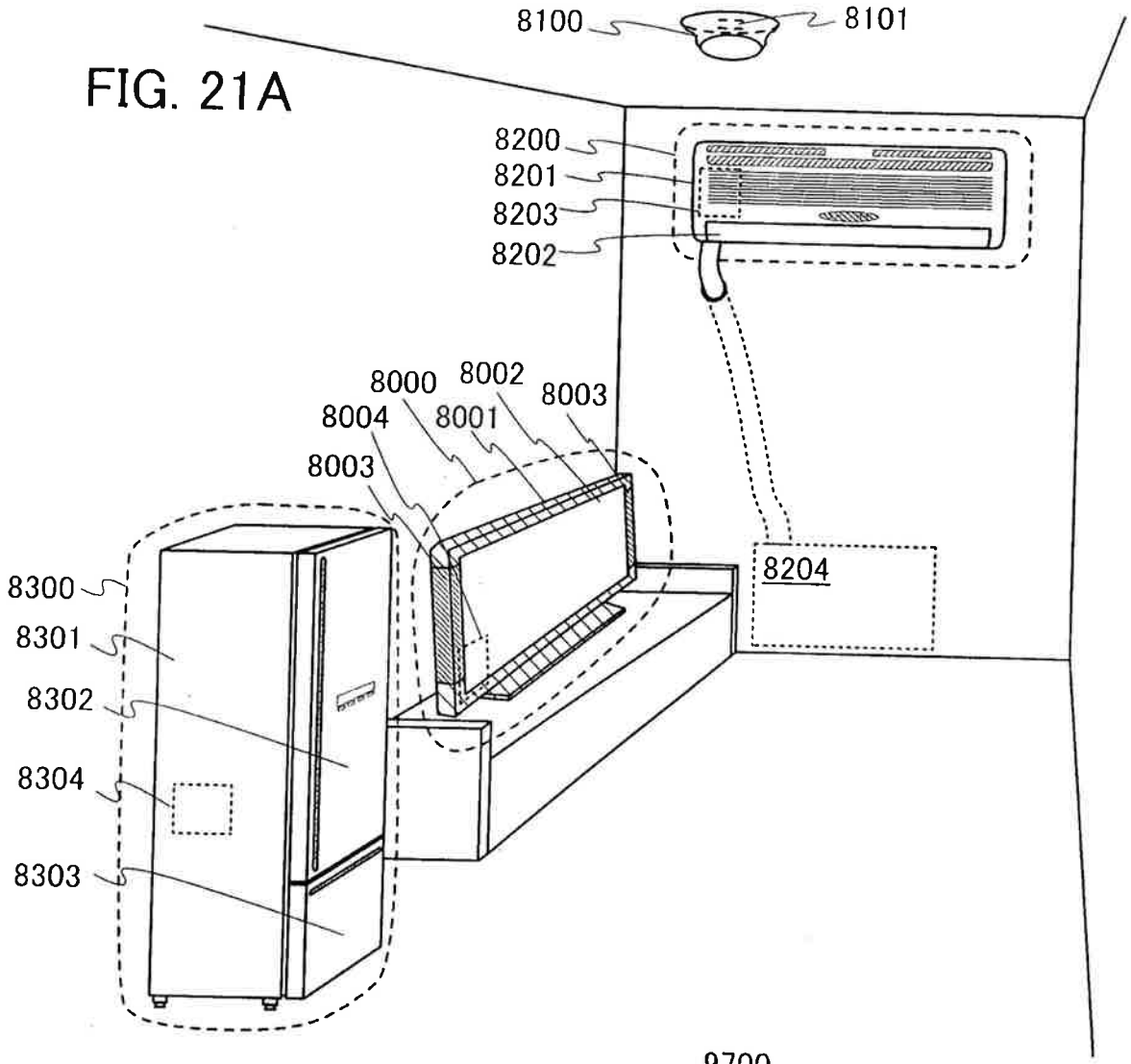


FIG. 21B

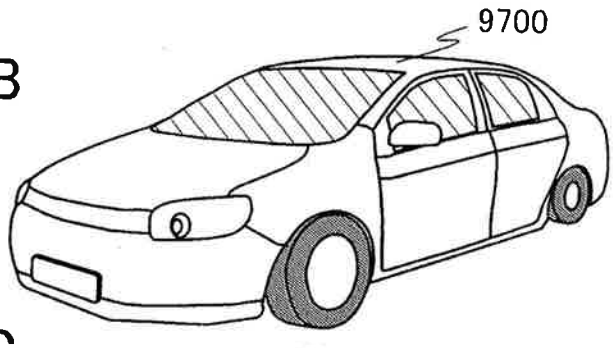


FIG. 21C

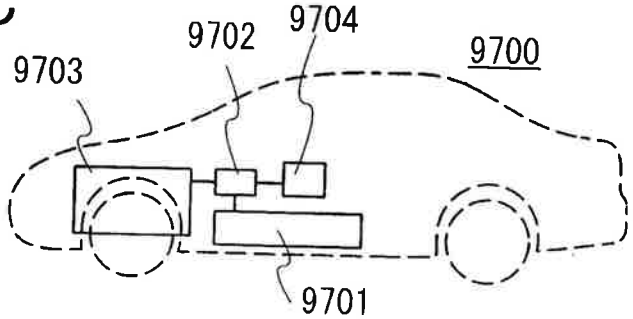
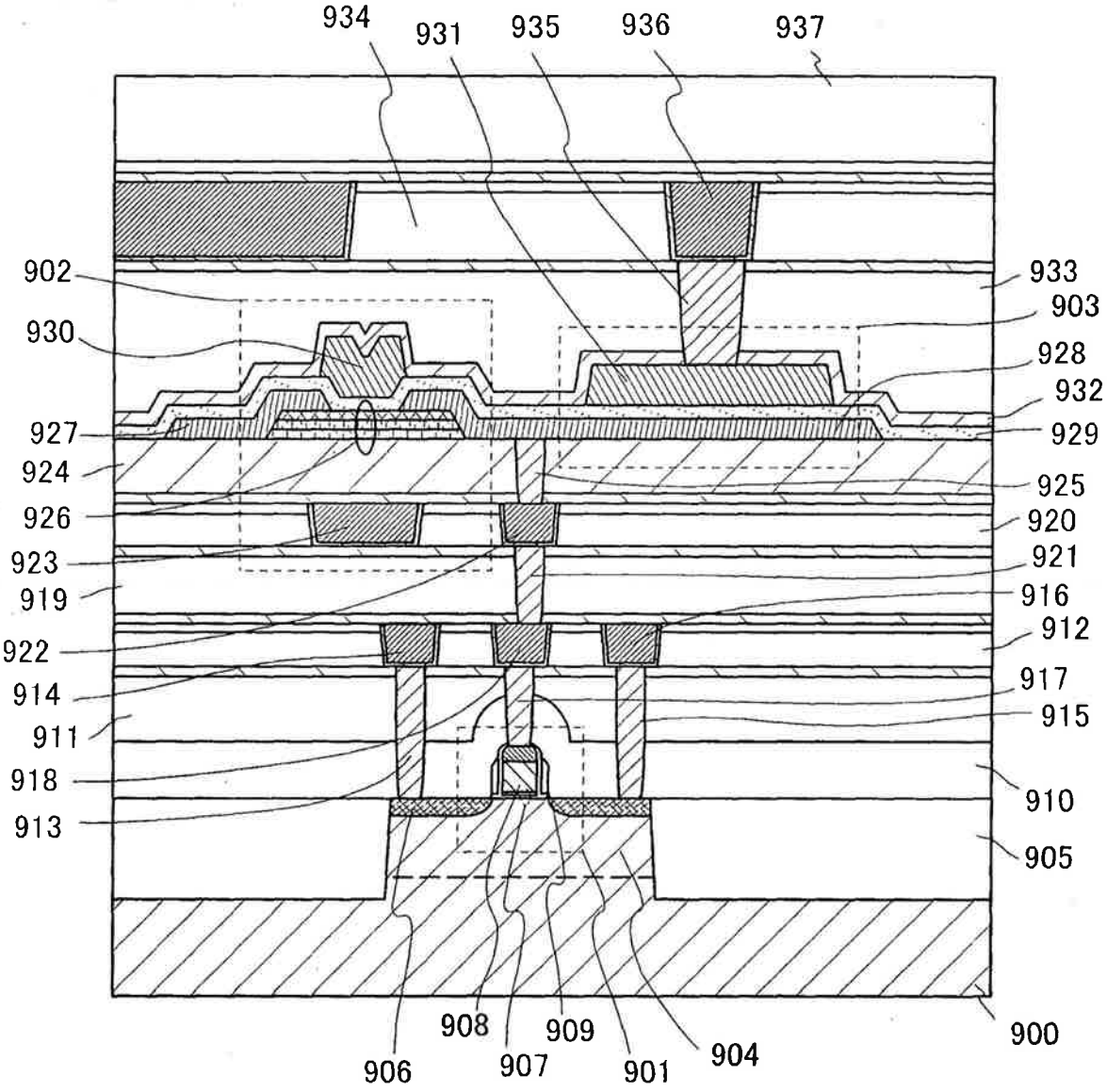


FIG. 22


934
931
935
936
937
902
930
927
924
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922
914
911
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907
901
904

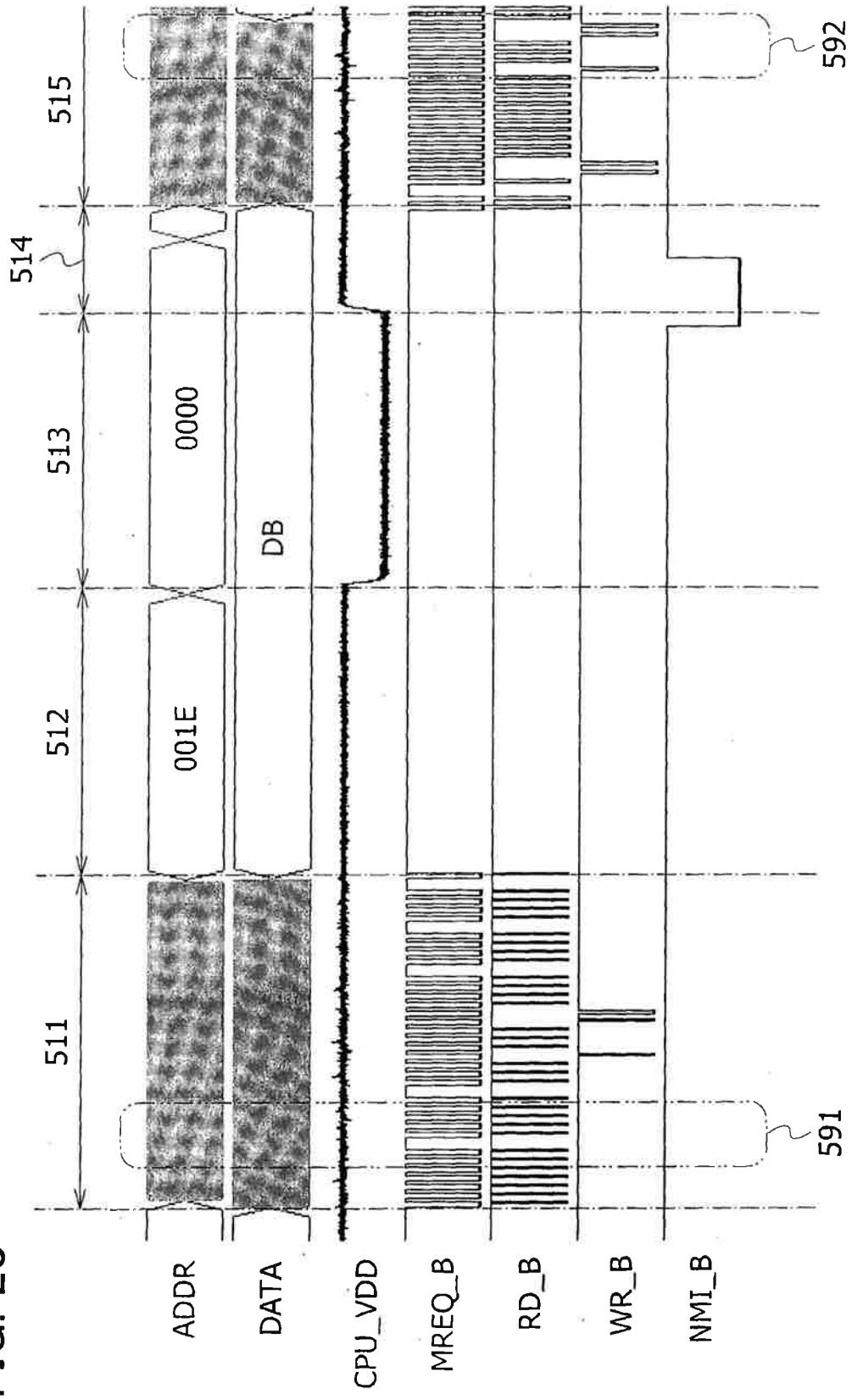

511
512
513
514
515
001E
0000
DB
591
592
ADDR
DATA
CPU_VDD
MREQ_B
RD_B
WR_B
NMI_B

FIG. 23

FIG. 24A

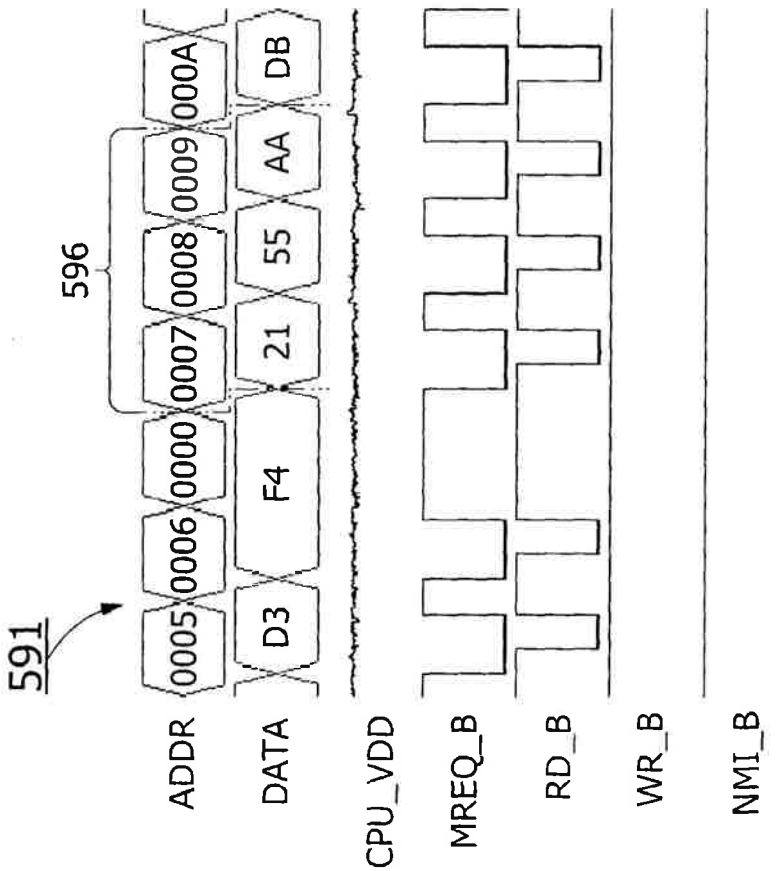


FIG. 24B

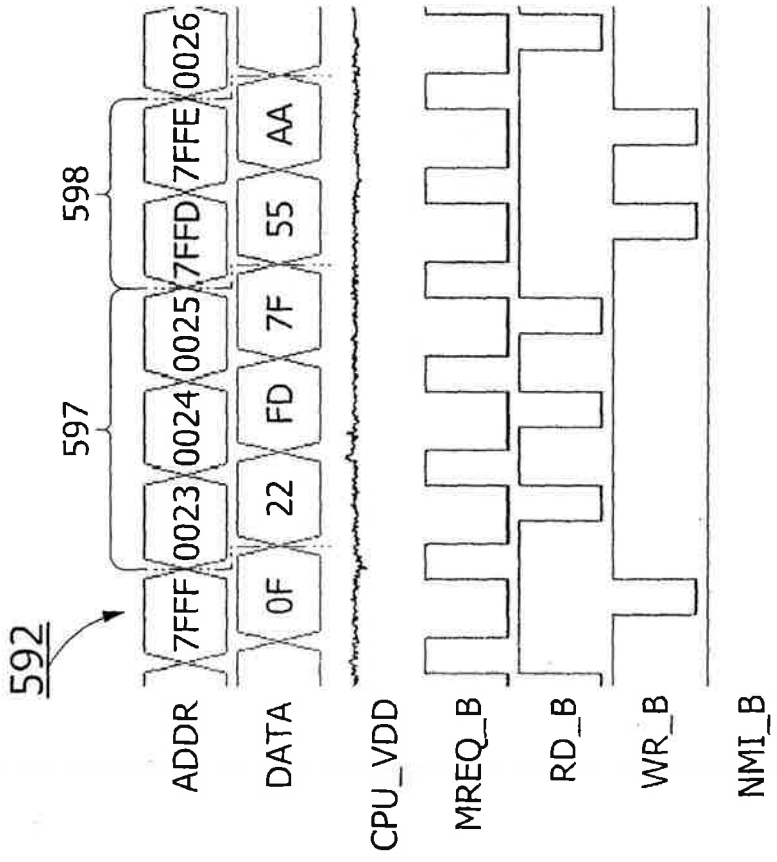
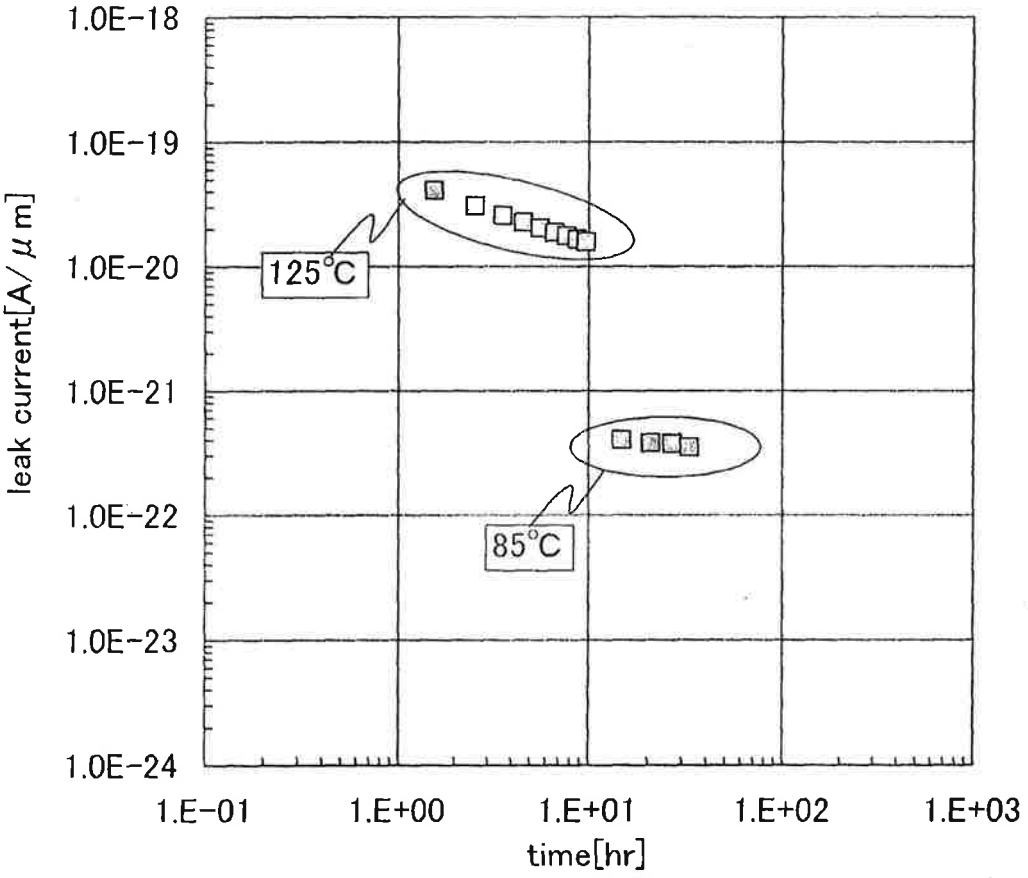


FIG. 25


1.0E-18
1.0E-19
1.0E-20
1.0E-21
1.0E-22
1.0E-23
1.0E-24
leak current[A/μm]
125°C
85°C
1.E-01
1.E+00
1.E+01
1.E+02
1.E+03
time[hr]