Description

The present invention relates to a method of manufacturing optical semiconductor structures,. It finds particular application in the field of the manufacture of opto-electronic devices such as semiconductor lasers, and.

A known family of opto-electronic devices has the following central structure : a substrate of semiconductor material having a mesa thereon, with burying layers on either side of the mesa. Such a device is described by O Mikami et al in "1.5 μm GaInAsP/Inp Buried Heterostructure Lasers Fabricated by Hybrid Combination of Liquid - and Vapour-Phase Epitaxy", Electronics Letters, 18 (5) (4.3.82) pages 237-239. The word "mesa" in this context is used to describe an upstanding stripe having steep sides and a flat top.

The devices of the family include a p-n junction across which current flows (the conventional current from p to n) and a waveguide region to which light is confined. The waveguide region may comprise an "active layer" in which electrons and holes combine with the production of photons by radiative recombination. Such an active layer has to relate suitably in band gap and refractive index to the other semiconductor regions of the structure in order to achieve a suitable degree of "confinement" of these processes to the active layer. The layers of material to either side of the waveguide region and in contact with the opposite faces of the waveguide region are known as "confinement layers".

A major field of application of semiconductor optical devices is in optical fibre communications systems. In general, the devices are constructed out of materials whose elemental components are selected from Groups III and V of the Periodic Table. Silica optical fibres as produced in recent years have loss minima at 1.3 μm and 1.55 μm approximately, the latter minimum being the lower. Accordingly, there is an especial need for devices operating in the range from 1.1 to 1.65 μm, especially from 1.3 to 1.6 μm. (These wavelengths, like all the wavelengths herein except where the context indicates otherwise, are in vacuo wavelengths). Semiconductor lasers operating in this region of the infrared usually comprise regions of indium phosphide, InP, and of quaternary materials indium gallium arsenide phosphides, $In_xGa_{1-x}As_yP_{1-y}$. By suitable choices of x and y it is possible to lattice-match the various regions while varying the band gaps of the materials. (Band gaps can be determined experimentally by, for example, photoluminescence). Additionally, both indium phosphide and the quaternary materials can be doped to be p - or n-type as desired.

Describing a selected device of the known family, a semiconductor laser, with its mesa uppermost, it has an active layer within the mesa. Electrical contacts are provided to the mesa and on the furthermost face of the substrate from the mesa. The "confinement" required is provided optically in a vertical direction, by changes in refractive index of the semiconductor material, and both optically and electrically in a horizontal direction by the burying layers. The burying layers act to cause any current flowing between the contacts to flow preferentially through the mesa and therefore through the active layer. In one form, the burying layers may present non-conducting semiconductor junctions to current flow between the contacts in use of the device.

Good electrical confinement is provided if the semiconductor layers between the contacts constitute a p-n junction and the burying layers in combination with the substrate constitute an n-p-n junction when taken in the same direction. In use the burying layers and substrate then comprise a reverse biased semiconductor junction in both directions. Alternatively the burying layers and substrate could present multiple reverse biased semiconductor junctions in one or both directions.

In another form, the burying layers may comprise "semi-insulating "materials such as Fe doped InP. These materials have a relatively high resistivity compared to for instance undoped InP. Burying layers in this form have advantages in that they substantially completely oppose current flow and show low capacitance effects. Low capacitance effects tend to increase device speed.

In the past devices of this type have been fabricated by means of liquid phase epitaxy (LPE). However there are problems associated with these techniques such as solutal convection within the melts, inaccurate thickness control of the burying layers and meltback of the mesas during fabrication. These have lead in particular to lack of uniformity over large areas and the techniques do not lend themselves easily to large scale production.

In the disclosure by O Mikami et al, a method for manufacturing a device with resistive burying layers is described. The layers which will constitute the mesa, comprising InP and quaternary layers, are grown on a semiconductor wafer by LPE, the mesa being produced by chemical etching on either side of a Si_3N_4 masking stripe. The burying layers, of high-resistivity InP, are then grown by vapour phase exitaxy (VPE) to either side of the mesa. The Si_3N_4 stripe remains during the VPE growth stage, preventing growth on the upper surface of the mesa itself, and is only subsequently removed.

The characteristics of two lasers produced by O Mikami et al are claimed to be as follows:-

1

(i) active layer thickness 0.2μm
(ii) active layer width 4μm
(iii) pulsed threshold current about 85 mA

2

(i) active layer thickness 0.2μm
(ii) active layer width 10μm
(iii) pulsed threshold current about 800mA to 500mA
(iv) single longitudinal mode output at wavelenth 1.525μm

The Mikami LPE-VPE hybrid technique solves the problem of meltback of the mesas during fabrication but still suffers from disadvantages. It retains an LPE growth step and therefore still does not lend itself to large scale production, a significant leakage current has been observed in the burying layers and the Si_3N_4 stripe shows a tendency to be bridged by the burying layers when the width of the stripe is reduced.

An alternative growth technique, metal organic vapour phase epitaxy (MOVPE), has been found promising for large scale device production. It offers a highly desirable combination of features : atomic scale interface abruptness, precise compositional control, and uniformity of thickness and composition over a large area.

Unfortunately it has not been found possible merely to replace the LPE and VPE growth steps of the Mikami technique with MOVPE growth steps. If this were possible, a structure having the better current confinement of reverse biased junction burying layers would be produced, with a concomitant, higher potential output power. Although MOVPE could be used to grow the layers of the mesa, the successful growth of the burying layers in the Mikami technique depends on the growth characteristics of VPE. The chemical etching step of the Mikami technique produces a mesa of a characteristic cross section. If MOVPE is used to try and grow burying layers on such a mesa, instead of laterally extending burying layers, upstanding "ears" of InP have been found to develop, the lateral surfaces of the mesa not being continuously covered.

A method of fabricating buried mesa structure lasers using only low pressure "metalorganic chemical vapour deposition" (LP-MOCVD) epitaxial growth steps is outlined in the following paper : "Very Low Threshold Buried Ridge Structure Lasers Emitting at 1.3 μm Grown by Low Pressure Metalorganic Chemical Vapour Deposition" by M Razeghi et al, Applied Physics Letters, 46 (2) (15.1.85) pages 131-133. (MOCVD is an alternative term for MOVPE.) The method comprises the steps of growing onto an InP substrate, an n-doped InP confinement layer, an undoped GaInAsP active layer, and a p-doped InP layer for avoiding the formation of defects near the active layer during etching. Etching using a mask, the active layer is reduced to a mesa. After removing the mask, the mesa is covered by a p-doped InP layer and a p-doped GaInAs cap layer.

All the growth steps of the above method are performed by low pressure MOVPE and hence large scale production should be facilitated. Further it is particularly convenient since only one growth technique must be employed. However, the devices produced either rely on a built-in potential difference between the large area p-n homo-junctions to each side of the active region and the p-n heterojunction through the relatively small area active region itself or involve a more complicated fabrication process. Although a lowest measured threshold current of 11 mA using continuous wave operation has been quoted, the values given for measurements relating to 269 devices were variable in the range from 17.9 mA to 50.0 mA inclusive. 44.6% of these devices had a threshold current of more than 45 mA. Further, an optical power emission of only up to 15 mW is quoted.

In EP-A-0038085 there is described an InGaAsP/InP buried heterostructure laser diode in which the active layer is contained in a mesa structure. A blocking layer of InP is grown by LPE up the sides of the mesa. A further InP layer, a current confining layer, is grown by LPE on the blocking layer. During the growth of these two layers the top of the mesa is covered in silica and, provided that the mesa is 4 microns or less in width, use of LPE results in no overgrowth of the mesa. The upper semiconductor surface of the mesa consists of an InGaAsP waveguiding layer and not InP. All epitaxial growth involves the use of LPE. There is no suggestion that the method could or should be adapted to permit the use of other growth technologies or of how any such adaptation could be effected.

Razeghi et al in Appl. Phys. Lett. 46, 2, 1985, pp131-133 detail the production of buried ridge structure lasers of GaInAsP/InP grown by MOCVD (MOVPE). The simple device structure enables a simple two-stage growth process to be used with excellent reproducibility and homogeneity, with high processing yields. External quantum efficiency of 60% with a cw threshold current of 11mA were achieved. The fabriction process involves sequential growth of an n-doped InP confinement layer, a GaInAsP active layer and a p-doped InP overlayer. Next a photolithographic mask was used in an etch step to define a 2micron ridge in the top InP layer and the active layer. After removing the resist mask, the ridge was covered with a p-doped InP confinement layer and a p-doped GaInAs cap layer. Localisation of the current is achieved by the built-in potential difference between the p-n InP homo-

junction on each side of the active region and the p-n InP - GaInAsP heterojunction of the active region. Thus it is clear that the InP confinement layer, which is grown by MOVPE , is formed not just beside the ridge but also on top of and over the ridge. This of course is quite distinct from the growth characteristics which are achieved and relied upon in the present invention.

Razeghi et al state that their structure embodies a simpler fabrication process as compared to conventional buried lasers because reverse p-n junctions, properly placed near the active layer, are not required to block the current leaks outside the buried stripe.

It is an object of the present invention to provide a method of manufacturing an optical semiconductor structure. This object is solved by the method according to claim 1. Hereinafter, structures and devices may be described in terms, such as "uppermost", which imply a specific orientation of the structure or device. The use of such terms is for convenience of description only and should not be taken to limit any structure or device to a specific orientation.

It is important for growth of the burying layers by MOVPE that the lateral surfaces of the mesa are not substantially re-entrant. In particular it is preferable that the uppermost layer of the mesa should not contribute (III) A planes to the lateral surfaces. There should not be an overhang of any part of either of the lateral surfaces equal to more than 10% of the width of the uppermost surface of the mesa. More preferably any overhang should not be equal to more than 5% of the width of the uppermost surface of the mesa or there should be no overhang, the mesa being vertically sided or even tapered towards its uppermost surface.

By using a method according to an embodiment of the present invention, the silica stripe can be produced so as to be self aligned, and centrally placed on the mesa.

Preferably the silica stripe is substantially equal in width to the width of the uppermost surface of the mesa. This facilitates growth of the burying layers. For instances, the width of the stripe should not be more than 0.4μm greater or less than the width of the uppermost surface of the mesa.

In certain cases it can be difficult to achieve a stripe of growth suppressing material. It has been found that a method of enhancing the growth suppressing properties of the surface of certain materials, such as silica, is to subject that surface to a temperature which lies in the range from 600°c to 700°c inclusive for a period of at least one minute in the present of PH_3. It may be found preferable to increase that period to more than three or even more than five minutes.

Alternative methods of carrying out steps ii) and iii) of Claim 1 are set out in the dependent claims.

A particularly important application of the present invention is in the production of lasers which will operate in a single transverse mode. These lasers are of major importance in optical communication systems. Such lasers can be produced from semiconductor structures made by the method of the present invention in which the uppermost surface of the mesa is restricted to being not more than 5 um wide.

A single transverse mode semiconductor laser, and methods for making it, according to embodiments of the present invention will now be described, by way of example only, with reference to the accompanying Figures in which:

Figure 1 shows a double heterostructure wafer for use in making the laser;

Figures 2a to 2f show stages in production of an initial semiconductor structure from the wafer of Figure 1;

Figures 3a to 3f show stages in an alternative method of producing the initial semiconductor structure from the wafer of Figure 1;

Figure 4 shows a semiconductor structure which comprises the initial semiconductor structure after burying layers have been grown;

Figure 5 shows the structure of Figure 4 overgrown with a covering layer;

Figure 6 shows the completed laser;

Figure 7 shows a graph of output power in mW plotted against bias current for a completed laser;

Figure 8 shows the pulse response of a completed laser to current pulse modulation; and

Figure 9 shows a histogram of threshold currents measured for a plurality of lasers.

Each of Figures 1 to 6 above shows only a portion of the wafer and stages in the production of only a single laser using that portion of wafer.

Figures 1 to 6 are not drawn to scale. They represent cross sections in each case but cross hatching is omitted for the purpose of clarity.

Referring to Figure 6, a completed laser comprises a layered mesa 3,4,5 on a substrate 2. The mesa 3,4,5 has sidewalls which caper towards its uppermost surface 15. The sidewalls are buried by burying layers 8, 9 whose uppermost surfaces 17 extend upwards and away from the uppermost surface 15 of the mesa to form a flared groove.

Referring to Figure 1, the first stage in production of the laser is to produce a double heterostructure wafer 1. The base layer 2 is a 200 μm (100) orientated S doped InP layer with the doping level n approximately equal to 8×10^{18} cm^{-3}. Onto the base layer are grown the following three layers 3, 4, 5 : a 0.5 μm S doped InP layer 3, n approxi-

mately equal to 2 x 10^{18} cm^{-3}; a 0.14 μm undoped GaInAsP layer 4; and a 0.3 μm Cd doped InP layer 5, p approximately equal to 5 x 10^{17} cm^{-3}. The GaInAsP layer 4 has a bandgap equivalent of 1.52 μm as determined by photoluminescence. The layers 3, 4, 5 are lattice matched, being grown by MOVPE under normal growth conditions.

Referring to Figure 2a, a fifth layer 6 of SiO_2 is next deposited. This layer is grown by chemical vapour deposition (CVD), from a mixture of SiH_4 and O_2 as the active gas, to a thickness of between 100 nm and 300 nm. Growth is carried out at a temperature of 450 °C.

Referring to Figure 2b, Waycoat W43 negative photoresist material is used to form a mask 7 comprising a stripe 5 μm wide which extends in the ⟨110⟩ direction with respect to the wafer 1. The mask 7 is exposed and developed in the normal manner then baked at 150 °C for 45 secs to prevent the resist from lifting during the next step.

Referring to Figure 2c, the SiO_2 (silica) is etched using the mask 7 by Countdown "silox etch". Etching is isotropic and therefore the photoresist mask 7 is undercut with a 1 : 1 undercut to depth ratio. By periodic observation with a microscope, the extent of silica remaining under the mask 7, which is transparent, can be determined and etching is continued until a stripe 16 of silica 1 μm wide remains. Only the silica is etched by this etchant, the layer below it not being affected. Immediately after etching the sample is stored in a desiccator at 10 °c for at least half a day to remove occluded water from beneath the undercut resist. If this is not done, and water remains, the edges of the resist may not be uniform after the next processing stage.

Referring to figure 2d, in order to seal the 1 μm silica stripe 16, the sample is heated at 150 °C for 5 mins. This causes the stripe of the photoresist mask 7 to soften and flow to the extent that the undercut portions drop onto the semiconductor surface, sealing in the SiO_2 stripe 16 and restoring the effective mask width to approximately 5 μm.

Referring to Figure 2e, the next stage is to etch a mesa, using the reflowed photoresist as a mask 7'. The quaternary layer of the wafer substrate forms an active layer in the mesa. It can be desirable that the sides of the mesa should be smooth. If this is so, subsequent growth reliability and reproducibility can be enhanced. Further, smooth sides can lead to improved performance in a completed laser. In order to obtain smooth sides of the mesa, an etchant which will etch the different layers 2, 3, 4, 5 of the double heterostructure wafer, including the active layer, at substantially equal rates should be used. In the present method a 0.2% solution of bromine in methanol at 20 °C is used but other etchants could be used, such as a solution of bromine in acetic acid. This produces a mesa having only a relatively slight shoulder at the level of the active layer 4.

Again, the extent to which the photoresist mask 7' is undercut during etching can be monitored using a microscope. Etching is continued until the uppermost surface 15 of the mesa is in the range from 1.2 μm to 1.5 μm wide. This dimension range is desirable for correct operation of the completed laser.

The dimensions given for the stripe 16 of SiO_2 and the mesa may of course be varied but preferably, for the purpose of reliability, the stripe 16 of SiO_2 should be not more than 0.4μm different in width to the uppermost surface 15 of the mesa.

The use of the resist mask 7' in etching the mesa is thought to produce a tapered mesa because the mask 7' does not adhere strongly to the material of the wafer, in contrast to silica masks. The latter tend to produce mesas with strongly reentrant lateral surfaces. Resist materials other than the photoresist material specified above may also be found satisfactory. However it must be possible to reflow the material of the resist mask 7 so as to seal the silica stripe 16, by heat or otherwise.

Referring to Figure 2f, after etching of the mesa the photoresist mask 7' is removed. Removal is carried out using Indust-Ri-Chem Lab resist strip J100 and methanol and the silica stripe 16 is left intact. This sample is then cleaned using H_2SO_4, rinsed in deionised water and blown dry. The sample at this stage represents the initial semiconductor structure onto which the burying layers are grown, and can be described as a substrate having a mesa thereon, a stripe 16 of silica being centrally positioned on the mesa.

Referring to Figures 3a to 3f, in an alternative method of making the initial semiconductor structure, again a double heterostructure wafer 1 as shown in Figure 1 is the starting point. However in this second method the first step is to oxidise the uppermost surface of the wafer to degrade a subsequent interface with silica growth-suppressing material.

To oxidise the surface, a mixture of nitrogen and oxygen is flowed over the wafer 1 for a few minutes, generally less than ten minutes. A mixture of approximately one part O_2 to five parts N_2 is appropriate but the flow time and mixture proportions are inter-dependent and the combination must generally be determined by experiment. It may be found for instance that considerably lower proportions of O_2 can be effective. Referring to Figure 3a, 0.27 μm of silica 6 is then deposited immediately onto the oxidised uppermost surface of the wafer 1 without disturbing the sample.

Referring to Figure 3b, Waycoat negative photoresist material is again used to form a mask 7 comprising a stripe which extends in the ⟨110⟩ direction with respect to the wafer 1. The stripe in this case is less than 5μm wide, being for intance from 4 to 4.5μm wide where a mesa of depth 1.5μm is intended. The mask is then baked as before, prior to etching the silica layer 6.

Referring to Figure 3c, the silica layer 6 is etched using the resist mask 7, to create a double layered mask 16, 7.

Referring to Figure 3d, the mesa is then etched using 0.2% Br/MeOH as before. Etching is carried out for a pre-selected time period so as to achieve the required depth. The result is a mesa supporting the double layered mask 16, 7, the mask overhanging the lateral surfaces of the mesa.

Because the overhanging silica can cause difficulty in later stages of the laser fabrication, it is removed. Firstly the sample is rebaked so as to seal the resist mask 7 to the silica stripe 16 but without any significant change in profile of the resist mask 7. Then the sample is placed in buffered HF for a time sufficient to etch away the overhanging silica from beneath where the silica is exposed.

Referring to Figure 3e, the result of etching the overhanging silica as above is to reduce the silica stripe 16 to a width slightly less than that of the uppermost surface 15 of the mesa. The side surfaces of the stripe 16 slope outwards towards the resist mask 7. This sloping characteristic is a result of the rebaking step which seals the resist mask 7 to the silica stripe 16, and is advantageous when burying layers are subsequently grown.

Referring to Figure 3f, after etching of the overhanging silica, the resist mask 7 is again removed using Indust-Ri-Chem lab resist strip J100 and methanol. This leaves a mesa with a stripe 16 of silica on top, the uppermost surface 15 of the mesa being exposed over a narrow distance at each edge.

Under different conditions, such as where a relatively shallow mesa is etched, the silica stripe 16 may not overhang the mesa to any great extent and may not require the etching step above to remove overhanging material. It has been found that adequately grown burying layers 8, 9 can be achieved even when the silica stripe 16 overhangs the mesa edges slightly. That is, the silica stripe 16 does not cause voids to develop adjacent the mesa as the burying layers 8, 9 are grown. In practice it is preferable that the width of the silica stripe 16 should be not more than 0.4μm wider or narrower than the width of the uppermost surface 15 of the mesa.

Although both methods described above for making an initial semiconductor structure, with reference to Figures 2a to 2f and 3a to 3f respectively, result in a tapered mesa, it is only necessary that the mesa should have substantially non re-entrant sidewalls. For instance there should not be an overhang of any part of either of the lateral surfaces equal to more than 10% of the width of the uppermost surface 15 of the mesa. Preferably any overhang should not be equal to move than 5% of the width of the uppermost surface 15 of the mesa. If the sidewalls of the mesa overhang to too great an extent then satisfactory burying layers cannot be grown subsequently by MOVPE.

Referring to Figure 4, the burying layers 8, 9 are grown in two stages onto the initial semiconductor structure : a 0.4 μm, Cd doped InP layer 8, p approximately equal to 5×10^{17} cm^{-3}; and a 0.8 μm, S doped InP layer 9, n approximately equal to 1×10^{17} cm^{-3}. Growth conditions again are generally as is normal for MOVPE growth but before growth starts, the sample is heated to 650 • C for 5 mins in the presence of PH_3. This treatment acts to enhance the action of the silica as a MOVPE growth-suppressing material even at stripe widths as low as 1 μm or so.

It should be noted that the period for which the sample must be heated in the presence of PH_3 will vary according to the conditions applied. For instance, if the concentration of PH_3 is increased, the period may be reduced to three minutes or even to only one minute.

The resultant layers 8, 9 as can be seen in Figure 4, are grown so that the first layer 8 reaches the height of the mesa and the second layer 9 grows onto the exposed portions of the uppermost surface 15 of the mesa, adjacent to the SiO_2 stripe 16. Importantly however, because of the presence of the PH_3 treated silica stripe 16, the second layer 9 does not cover the mesa, developing an outwardly inclined facet 17 on each side of the stripe 16, thus leaving the stripe 16 exposed at the bottom of a V-shaped groove.

Although it is possible that the silica stripe 16 does not entirely prevent all growth on its surface during formation of the burying layers 8, 9, it should do so to the extent that the second burying layer 9 forms the flared groove, allowing sufficient access to the silica stripe 16 for its subsequent removal.

Referring to Figure 5, when the burying layers 8, 9 are complete the silica stripe 16 is removed and two further epitaxial layers, the covering layers 10, 11, are grown. The silica stripe 16 is removed in a 40% aqueous solution of HF and the two covering layers 10, 11 are grown, as are the earlier epitaxial layers, by MOVPE. Again normal growth conditions for this technique are applied. The covering layers 10, 11 comprise a 1 μm Cd doped InP layer 10, p approximately equal to 2×10^{18} cm^{-3},

and a 0.15 μm Zn doped GaInAs layer 11, p approximately equal to 4×10^{19} cm^{-3}.

As can be seen in Figure 5, the covering layers 10, 11 present a planar uppermost surface 20 in the region which lies over the mesa and the adjoining areas of the burying layers 8, 9. The planar surface 20 has a width which is greater than three times the width of the active layer of the mesa. (It should be noted that the planar surface 20 is not necessarily achieved by the method described above although such a surface can be commonly achieved.)

Referring to Figure 6, the final laser structure is completed by the conventional steps of providing a contact window 18 over the mesa, in a silica layer 12, and contacts 13, 14, 19 to the window 18 and to the opposing face of the laser. The contact 13, 14 to the window 18 is a sputtered Ti Au tunnelling Schottky contact, which may include a Pt barrier layer, while the contact 19 to the laser's opposing face is a sputtered and alloyed Ti-Au contact.

This final laser structure can be mounted (not shown) on a heat sink by soldering the heat sink to the contact 13, 14 to the window 18. Because of the planar surface 20, the solder need only have a thickness such as to accommodate the steps produced by the contact window 18. Hence the heat sink can be brought into close proximity to the semiconductor material of the mesa.

Some typical operating characteristics of a laser fabricated as described above are shown in Figure 7. A threshold current of 15 mA at 20°C and an output power of 28 mW have been obtained, using continuous wave operation. In pulsed wave operation, an output power of 39mW has been obtained.

In further testing of lasers made as described above, measurements of differential resistance have shown a consistent value above threshold of 6 ohms which indicates negligible loss of injected current through the burying layers 8, 9. This provides direct evidence that the positioning and integrity of the p-n junction of the burying layers 8, 9 were good. Temperature dependence of the threshold current was characterised by a To value of 50°K which is typical of 1.5 μm InGaAsP lasers and the measured external quantum efficiency of the laser was found to be 20%. Near circular far field patterns of 38° perpendicular and 32° parallel to the junction plane were obtained, reflecting the ability of the method of the present invention to provide control of the critical waveguide dimensions.

Speed measurements were carried out using a Textronix S6 sampling head. The pulse response, shown in Figure 8, of a device biased at 20 mA and modulated by a 20 mA current pulse gave values for rise and fall times (10-90%) of 750 psecs and 1 nsec respectively. This indicates a systems capability of at least 565 mbits/sec.

Although the method of the present invention is described above with reference to only one laser, in practice a plurality of lasers can be fabricated using a common double heterostructure wafer. In order to investigate the large area capability of the method, 105 lasers were selected randomly from an area of 4 cm^2 of a wafer, the mesas of the lasers being parallel and spaced apart with a period of 200 μm. Each laser was obtained by cleaving and scribing, typical device dimensions being 200 μm wide by 400 μm long. 81 of the lasers were found to be functional A histogram of threshold currents, I_0, shown in Figure 9, was plotted for the 81 working lasers. More than 70% of the working devices, that is, 54% of the total sample of 105 devices, had threshold currents of less than 30 mA, providing clear evidence of the large scale uniformity of the method.

The manufacture of only one laser structure has been described above. Other structures may also be found effective; for instance variation in the thickness of the various layers may be made. In particular, the position of the n-p junction in the burying layers may be brought closer to the p-n junction in the mesa by growing a shallower first burying layer. This may be more difficult to achieve reproducibly in practice but may provide more efficient electrical confinement to the active layer. Further, either fewer or more layers may be provided, such as extra quaternary layers above and below the active layer where a distributed feedback grating is provided. Extra layers may also be used to provide a second n-p junction within the burying layers.

It may be noted that methods according to the present invention are particularly convenient for use in making distributed feedback lasers because corrugations can conveniently be incorporated into the uppermost surface of the mesa.

Devices such as optical detectors or optical waveguides may also be made using methods according to the present invention which is not limited to the production of semiconductor lasers.

Claims

1. A method of making an optical semiconductor structure comprising InP-based materials, said method comprising the steps of:
   i) depositing a silica layer (6) as a metal organic vapour phase growth suppressing material on a semiconductor wafer (1) having a substrate (2) which carries multiple layers, the wafer having an InP uppermost layer (5);

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and a 0.15 μm Zn doped GaInAs layer 11, p approximately equal to 4×10^{19} cm^{-3}.

As can be seen in Figure 5, the covering layers 10, 11 present a planar uppermost surface 20 in the region which lies over the mesa and the adjoining areas of the burying layers 8, 9. The planar surface 20 has a width which is greater than three times the width of the active layer of the mesa. (It should be noted that the planar surface 20 is not necessarily achieved by the method described above although such a surface can be commonly achieved.)

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Some typical operating characteristics of a laser fabricated as described above are shown in Figure 7. A threshold current of 15 mA at 20°C and an output power of 28 mW have been obtained, using continuous wave operation. In pulsed wave operation, an output power of 39mW has been obtained.

In further testing of lasers made as described above, measurements of differential resistance have shown a consistent value above threshold of 6 ohms which indicates negligible loss of injected current through the burying layers 8, 9. This provides direct evidence that the positioning and integrity of the p-n junction of the burying layers 8, 9 were good. Temperature dependence of the threshold current was characterised by a To value of 50°K which is typical of 1.5 μm InGaAsP lasers and the measured external quantum efficiency of the laser was found to be 20%. Near circular far field patterns of 38° perpendicular and 32° parallel to the junction plane were obtained, reflecting the ability of the method of the present invention to provide control of the critical waveguide dimensions.

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The manufacture of only one laser structure has been described above. Other structures may also be found effective; for instance variation in the thickness of the various layers may be made. In particular, the position of the n-p junction in the burying layers may be brought closer to the p-n junction in the mesa by growing a shallower first burying layer. This may be more difficult to achieve reproducibly in practice but may provide more efficient electrical confinement to the active layer. Further, either fewer or more layers may be provided, such as extra quaternary layers above and below the active layer where a distributed feedback grating is provided. Extra layers may also be used to provide a second n-p junction within the burying layers.

It may be noted that methods according to the present invention are particularly convenient for use in making distributed feedback lasers because corrugations can conveniently be incorporated into the uppermost surface of the mesa.

Devices such as optical detectors or optical waveguides may also be made using methods according to the present invention which is not limited to the production of semiconductor lasers.

Claims

1. A method of making an optical semiconductor structure comprising InP-based materials, said method comprising the steps of:

   i) depositing a silica layer (6) as a metal organic vapour phase growth suppressing material on a semiconductor wafer (1) having a substrate (2) which carries multiple layers, the wafer having an InP uppermost layer (5);

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ii) selectively etching the silica layer (6) to form a stripe (16) of said silica extending in the ⟨110⟩ crystallographic direction of the wafer (1);
iii) creating a mesa having a width at its uppermost surface of 5 μm or less, under the stripe (16), the mesa having substantially non-re-entrant lateral surfaces, there being no overhang of any part of the lateral surfaces which is greater than 10% of the width of the uppermost surface of the mesa;
iv) subjecting the structure thus produced to a temperature which lies within the range from 600 °C to 700 °C inclusive for a period of at least one minute in the presence of PH_3;
v) growing InP burying layers (8,9) by metal organic vapour phase epitaxy to bury the lateral surfaces of the mesa; and
vi) removing the silica stripe (16).

2. A method according to claim 1 wherein steps ii) and iii) further comprise:
forming a mask (7) of resist material on the silica layer (6);
and selectively etching the silica layer (6) by means of the resist mask (7).

3. A method according to claim 1 wherein steps ii) and iii) comprise:
a) forming a mask (7) of resist material on the silica layer (6);
b) etching the silica layer (6), using the mask (7), such that the mask (7) is undercut;
c) reflowing the resist material of the mask (7) so that the portions of the mask which are undercut drop into contact with the semiconductor wafer (1);
d) etching the semiconductor wafer (1) using the reflowed mask (7') to create the mesa; and
e) removing the reflowed mask (7').

4. A method according to Claim 2, wherein step iii) comprises
etching the semiconductor wafer (1) using the mask (7) together with the stripe (16) to create said mesa and
removing the mask (7) of resist material; and
wherein step (i) is preceded by oxidation of the surface of said InP uppermost layer (5) so as to degrade the integrity of the subsequent interface between said surface and the silica layer (6).

5. A method according to claim 4, wherein the oxidation is carried out by flowing an oxidising gas or gas mixture over said surface.

6. A method according to claim 5 wherein the oxidising gas or gas mixture comprises a mixture of N_2 and O_2.

7. A method according to any one of the preceding claims, wherein the period of step iv) is at least three minutes.

8. A method according to claim 7 wherein the period is at least five minutes.

9. A method according to any one of the preceding claims wherein the width of the silica stripe (16) is not more than 0.4μm greater or less than the width of the uppermost surface (15) of the mesa.

10. A method according to any one of the preceding claims, wherein the semiconductor structure is a double heterostructure laser in which the mesa is formed on the InP substrate (2) such as to comprise a three-layered structure of an InP layer (3), an InGaAsP layer (4) and the uppermost InP layer (5), and wherein said InP burying layers (8,9) consist of a lower p doped InP layer (8) and an upper n doped InP layer (9),
and which method further comprises the steps of :
vii) epitaxially forming on top of the mesa and the burying layers (8,9) a further p doped InP layer (10) and a p doped GaInAs layer (11);
viii) forming on top of the GaInAs layer (11) a further silica layer (12);
ix) providing in said further silica layer (12) a contact window (18) over the mesa; and
x) forming contacts (13,14,19) to said contact window (18) and to the opposing face of the substrate to the laser structure.

Patentansprüche

1. Verfahren zum Herstellen einer optischen Halbleiterstruktur, die InP-basierende Stoffe aufweist, wobei das Verfahren die Schritte aufweist:
i) Ablagern einer Siliziumoxidschicht (6) als ein Material, das ein metallorganisches Dampfphasenwachsen unterdrückt, auf einem Halbleiter-Wafer (1) mit einem Substrat (2), der mehrere Schichten trägt, wobei der Wafer eine oberste InP-Schicht (5) aufweist;
ii) selektives Ätzen der Siliziumoxidschicht (6), um einen Streifen (16) des Siliziumoxids zu bilden, der sich in der kristallographi-

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schen ⟨110⟩-Richtung des Wafers (1) erstreckt;
iii) Schaffen eines Mesas, der eine Breite an seiner obersten Oberfläche von 5µm oder weniger hat, unter dem Streifen (16), wobei der Mesa im wesentlichen nicht hinterschnittene seitliche Oberflächen hat, wobei es keinen Überhang irgendeines Teils der seitlichen Oberflächen gibt, der größer als 10% der Breite der obersten Oberfläche des Mesas ist;
iv) Aussetzen der so erzeugten Struktur einer Temperatur, die innerhalb des Bereichs von 600 °C bis 700 °C einschließlich liegt, für eine Dauer von mindestens einer Minute unter Vorhandensein von PH_3;
v) Wachsen von eingrabenden Schichten (8, 9) durch metallorganische Dampfphasenepitaxie, um die seitlichen Oberflächen des Mesas einzugraben; und
vi) Entfernen des Siliziumoxidstreifens (16).

2. Verfahren nach Anspruch 1, wobei die Schritte ii) und iii) weiterhin aufweisen:
Bilden einer Maske (7) aus Resist-Material auf der Siliziumoxidschicht (6); und
selektives Ätzen der Siliziumoxidschicht (6) mittels der Resist-Maske (7).

3. Verfahren nach Anspruch 1, wobei die Schritte ii) und iii) aufweisen:
a) Bilden einer Maske (7) aus Resist-Material auf der Siliziumoxidschicht (6);
b) Ätzen der Siliziumoxidschicht (6) unter Verwendung der Maske (7), so daß die Maske (7) unterschnitten wird;
c) Abfließen Lassen des Resist-Materials der Maske (7), so daß die Abschnitte der Maske, die unterschnitten sind, in Kontakt mit dem Halbleiter-Wafer (1) fallen;
d) Ätzen des Halbleiter-Wafers (1) unter Verwendung der abgeflossenen Maske (7'), um den Mesa zu schaffen; und
e) Entfernen der abgeflossenen Maske (7').

4. Verfahren nach Anspruch 2, wobei Schritt iii) aufweist:
Ätzen des Halbleiter-Wafers (1), unter Verwendung der Maske (7) zusammen mit dem Streifen (16), um den Mesa zu schaffen, und Entfernen der Maske (7) aus Resist-Material; und
wobei dem Schritt (i) eine Oxidation der Oberfläche der obersten InP-Schicht (5) vorausgeht, um die Integrität des nachfolgenden Übergangs zwischen der Oberfläche und der Siliziumoxidschicht (6) zu verschlechtern.

5. Verfahren nach Anspruch 4, wobei die Oxidation ausgeführt wird, indem ein oxidierendes Gas oder ein Gasgemisch über die Oberfläche geflutet wird.

6. Verfahren nach Anspruch 5, wobei das oxidierende Gas oder Gasgemisch eine Mischung aus N_2 und O_2 aufweist.

7. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Dauer von Schritt iv) mindestens drei Minuten ist.

8. Verfahren nach Anspruch 7, wobei die Dauer mindestens fünf Minuten ist.

9. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Breite des Siliziumoxidstreifens (16) nicht um mehr als 0,4 µm größer oder kleiner als die Breite der obersten Oberfläche (15) des Mesas ist.

10. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Halbleiterstruktur ein Doppel-Heterostruktur-Laser ist, in dem der Mesa auf dem InP-Substrat (2) gebildet ist, um eine dreischichtige Struktur aus einer InP-Schicht (3), einer InGaAsP-Schicht (4) und der obersten InP-Schicht (5) aufzuweisen, und wobei die eingrabenden InP-Schichten (8, 9) aus einer unteren p-dotierten InP-Schicht (8) und einer oberen n-dotierten InP-Schicht (9) bestehen, und wobei das Verfahren weiterhin die Schritte aufweist:
vii) epitaxiales Bilden einer weiteren p-dotierten InP-Schicht (10) und einer p-dotierten GaInAs-Schicht 11 auf dem Mesa und den eingrabenden Schichten (8, 9);
viii) Bilden einer weiteren Siliziumoxidschicht (12) auf der GaInAs-Schicht (11);
ix) Vorsehen eines Kontaktfensters (18) in der weiteren Siliziumschicht (12) über dem Mesa; und
x) Bilden von Kontakten (13, 14, 19) an dem Kontaktfenster (18) und an der gegenüberliegenden Seite des Substrats mit der Laserstruktur.

Revendications

1. Un procédé de fabrication d'une structure optique semi-conductrice comprenant des matières à base de InP, ledit procédé comprenant les étapes consistant à:
i) déposer une couche de silice (6) comme matière supprimant une croissance de métal en phase vapeur organique sur une tranche semi-conductrice (1) comprenant un

substrat (2) qui porte des couches multiples, la tranche portant une couche supérieure (5) en InP;
ii) graver sélectivement la couche de silice (6) afin de former une bande (16) de ladite silice s'étendant dans la direction cristallographique ⟨110⟩ de la tranche (1);
iii) créer sous la bande (16) un mesa, dont la largeur à sa surface supérieure est de 5 mm ou moins, les surfaces latérales du mesa étant sensiblement non rentrantes; aucun surplomb d'une partie quelconque des surfaces latérales n'étant supérieure à 10 % de la largeur de la surface supérieure du mesa;
iv) soumettre la structure ainsi produite à une température, qui est située à l'intérieur de la plage de 600 °C à 700 °C inclus, pendant une période d'au moins une minute en présence de PH_3;
v) faire croître des couches d'enterrement en InP (8, 9) par une épitaxie métal en phase vapeur organique afin d'enterrer les surfaces latérales du mesa; et
vi) enlever la bande de silice (16).

2. Un procédé selon la revendication 1 dans lequel les étapes ii) et iii) comprennent en outre:
une formation, sur la couche de silice (6), d'un masque (7) en matière de résine photosensible; et
une gravure sélective de la couche de silice (6) au moyen du masque en résine photosensible (7).

3. Un procédé selon la revendication 1 dans lequel les étapes ii) et iii) comprennent les étapes consistant à:
a) former sur la couche de silice (6) un masque (7) en matière de résine;
b) graver la couche de silice (6) en utilisant le masque (7) en formant une contre-dépouille sous le masque (7);
c) faire fluer de nouveau la matière de résine du masque (7) d'une manière telle que les parties du masque sur lesquelles existe une contre-dépouille tombent en contact avec la tranche semi-conductrice (1);
d) graver la tranche semi-conductrice (1) en utilisant, afin de créer le mesa, le masque (7') après le nouveau fluage;
e) enlever le masque (7') flué de nouveau.

4. Un procédé selon la revendication 2 dans lequel l'étape iii) comprend:
une gravure de la tranche semi-conductrice (1) en utilisant à la fois le masque et la bande (16) afin de créer ledit mesa, et
un enlèvement du masque (7) de matière de résine photosensible; et
dans lequel l'étape i) est précédée par une oxydation de la surface de ladite couche supérieure (5) en InP de façon à dégrader l'intégrité de l'interface ultérieure entre ladite surface et la couche de silice (6).

5. Un procédé selon la revendication 4, dans lequel l'oxydation est effectuée en faisant passer un gaz ou un mélange de gaz oxydants au-dessus de ladite surface.

6. Un procédé selon la revendication 5, dans lequel le gaz ou le mélange de gaz oxydants comprend un mélange de N_2 et O_2.

7. Un procédé selon l'une quelconque des revendications précédentes dans lequel la période de l'étape iv) est d'un moins trois minutes.

8. Un procédé selon la revendication 7 dans lequel la période est d'au moins cinq minutes.

9. Un procédé selon l'une quelconque des revendications précédentes dans lequel la largeur de la bande de silice (16) ne dépasse pas de plus de 0,4 mm à la largeur la surface supérieure (15) du mesa et n'est pas inférieure à cette largeur.

10. Un procédé selon l'une quelconque des revendications précédentes dans lequel la structure semi-conductrice est un laser à double hétérostructure dans lequel le mesa est formé sur le substrat (2) en InP de manière à comprendre une structure en trois couches formée d'une couche en InP (3), d'une couche en InGaAsP (4) et de la couche supérieure en InP (5), et dans lequel lesdites couches d'enterrement en InP (8, 9) consistent en une couche inférieure (8) en InP dopée p et une couche supérieure (9) en InP dopée n, et dans lequel le procédé comprend en outre les étapes consistant à:
vii) former par épitaxie, au dessus du mesa et des couches d'enterrement (8, 9), une autre couche en InP dopée p (10) et une couche d'enterrement en GaInAs dopée p (11);
viii) former au-dessus de la couche en GaInAs (11) une autre couche de silice (12);
ix) ménager dans ladite autre couche de silice (12) une fenêtre de contact (18) au-dessus du mesa; et
x) former, à ladite fenêtre de contacts (18) et à la face opposée du substrat, des contacts (13, 14, 19) vers la structure laser.