FIG. 1

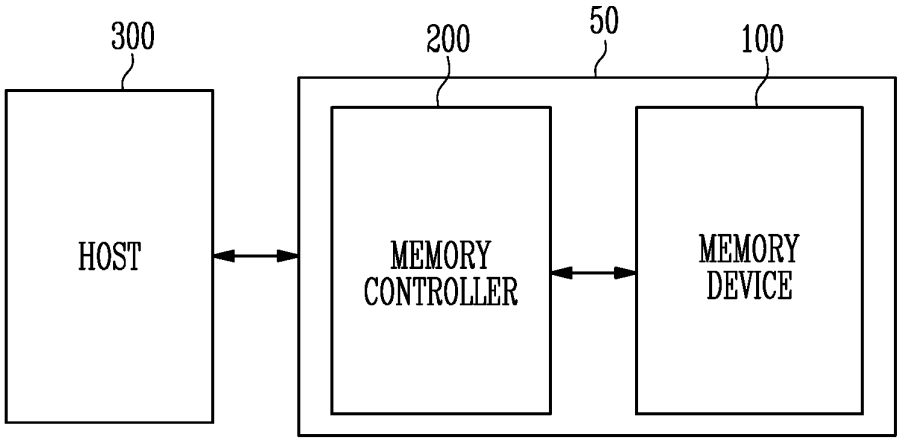


FIG. 2

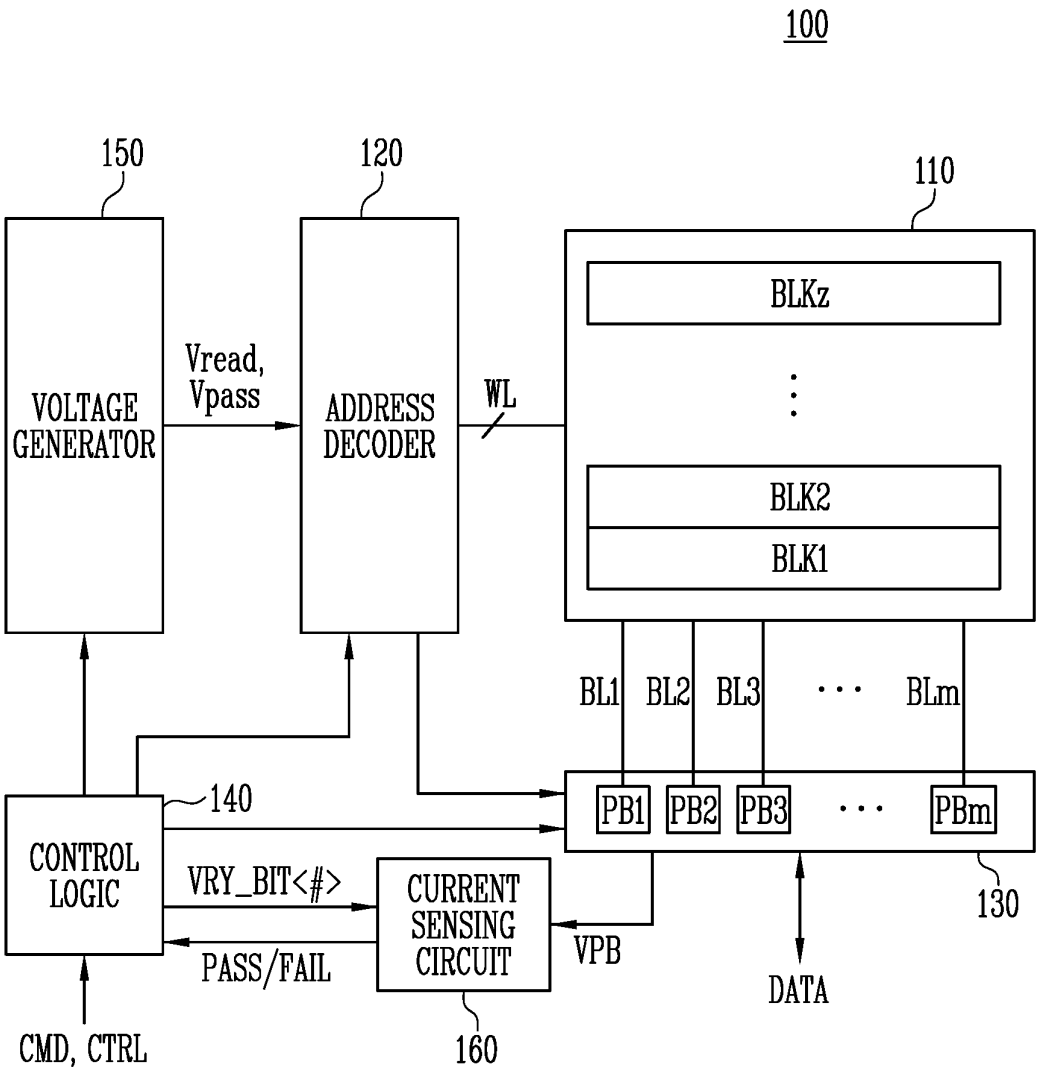

100
150
120
110
VOLTAGE GENERATOR
Vread, Vpass
ADDRESS DECODER
WL
BLKz
BLK2
BLK1
BL1
BL2
BL3
BLm
PB1
PB2
PB3
PBm
130
140
CONTROL LOGIC
VRY_BIT<#>
PASS/FAIL
CURRENT SENSING CIRCUIT
VPB
DATA
CMD, CTRL
160

FIG. 3

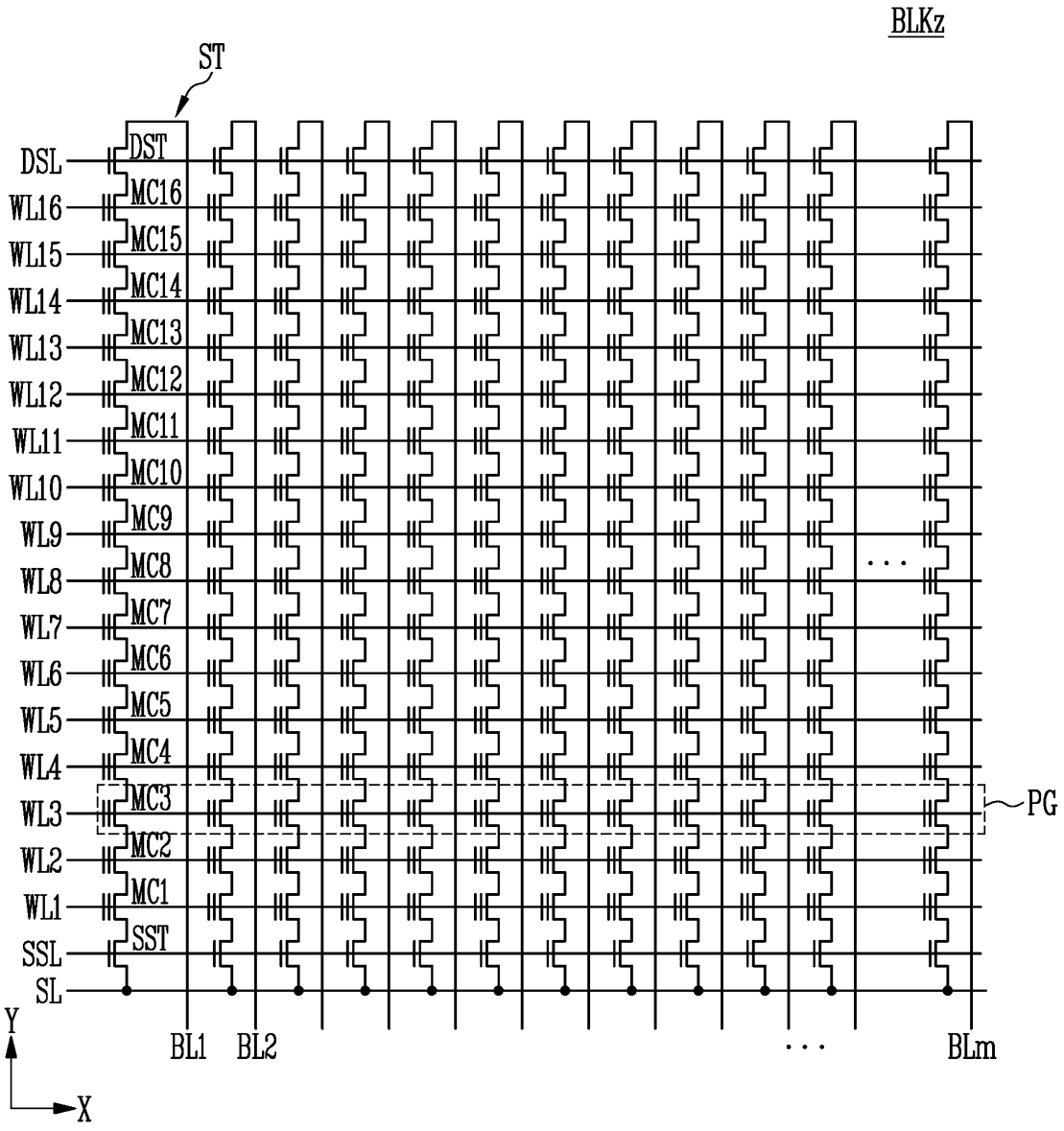

BLKz
ST
DST
DSL
MC16
WL16
MC15
WL15
MC14
WL14
MC13
WL13
MC12
WL12
MC11
WL11
MC10
WL10
MC9
WL9
MC8
WL8
MC7
WL7
MC6
WL6
MC5
WL5
MC4
WL4
MC3
WL3
MC2
WL2
MC1
WL1
SST
SSL
SL
PG
BL1
BL2
BLm
Y
X

FIG. 4

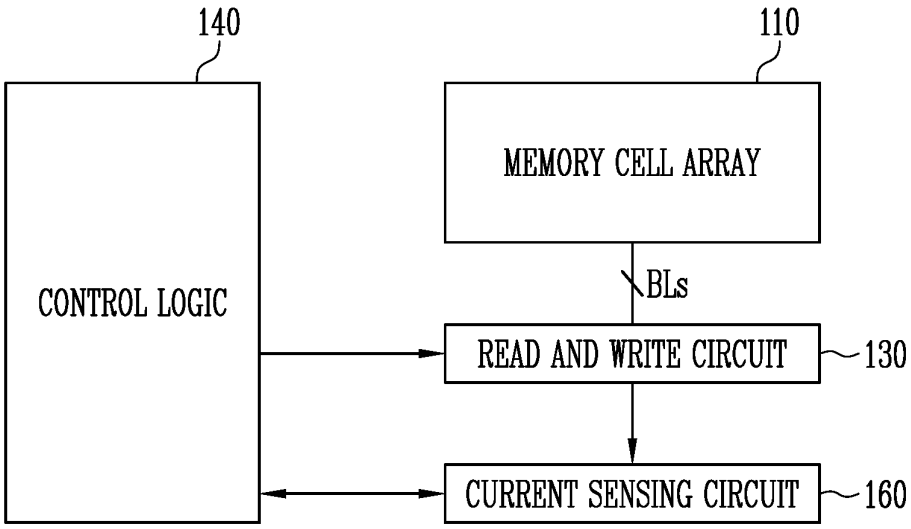

140
110
MEMORY CELL ARRAY
CONTROL LOGIC
BLs
READ AND WRITE CIRCUIT
130
CURRENT SENSING CIRCUIT
160

FIG. 5

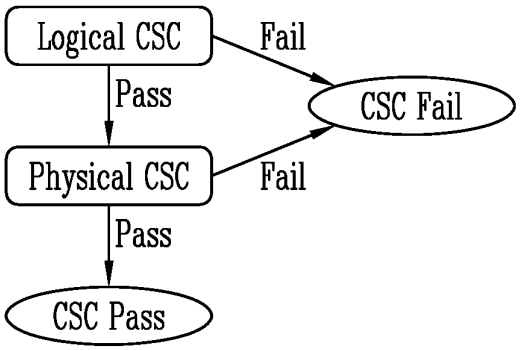

Logical CSC
Fail
Pass
CSC Fail
Physical CSC
Fail
Pass
CSC Pass

FIG. 6

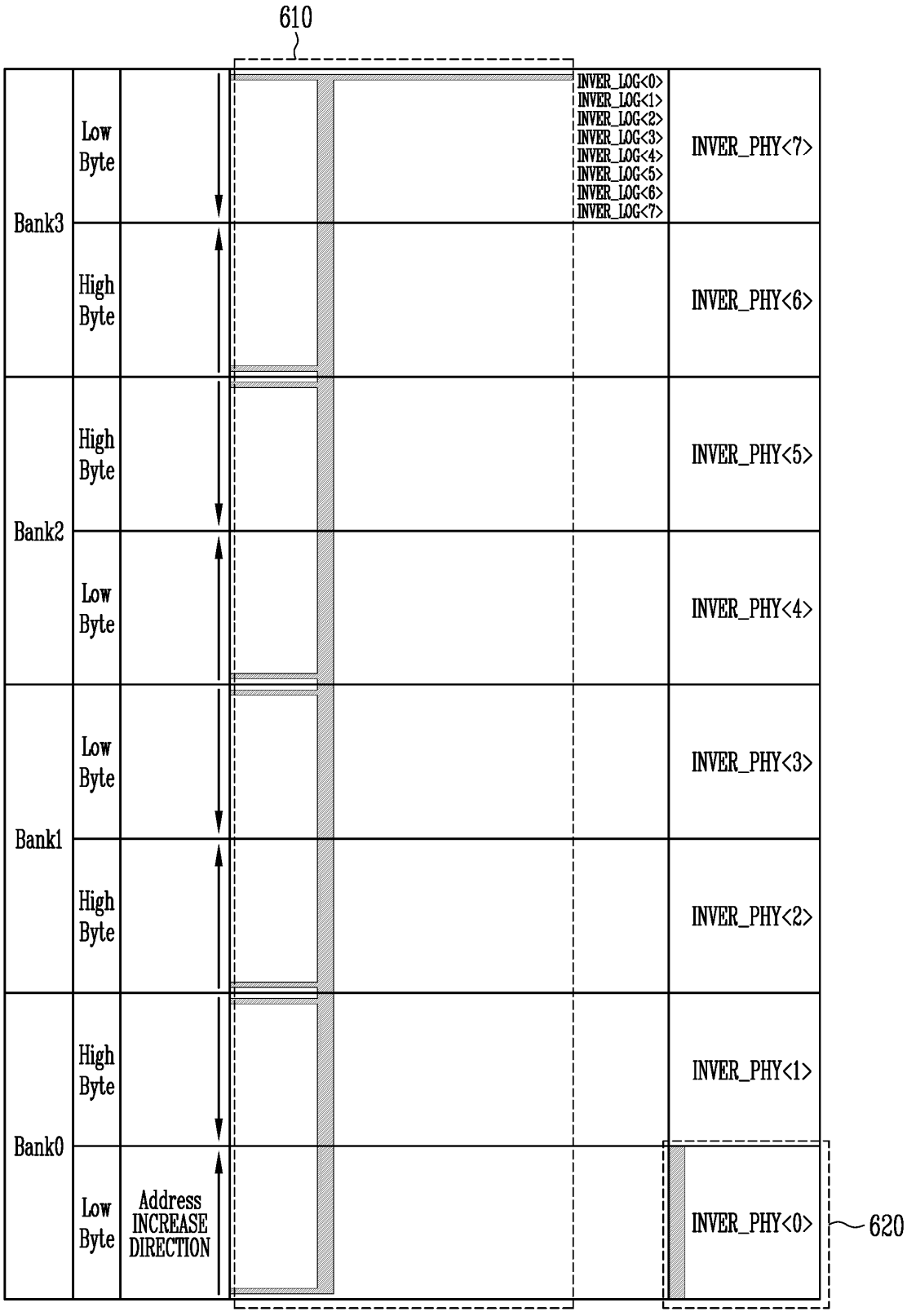

610
Bank3
Low Byte
High Byte
Bank2
High Byte
Low Byte
Bank1
Low Byte
High Byte
Bank0
High Byte
Low Byte
Address INCREASE DIRECTION
INVER_LOG<0>
INVER_LOG<1>
INVER_LOG<2>
INVER_LOG<3>
INVER_LOG<4>
INVER_LOG<5>
INVER_LOG<6>
INVER_LOG<7>
INVER_PHY<7>
INVER_PHY<6>
INVER_PHY<5>
INVER_PHY<4>
INVER_PHY<3>
INVER_PHY<2>
INVER_PHY<1>
INVER_PHY<0>
620

FIG. 7

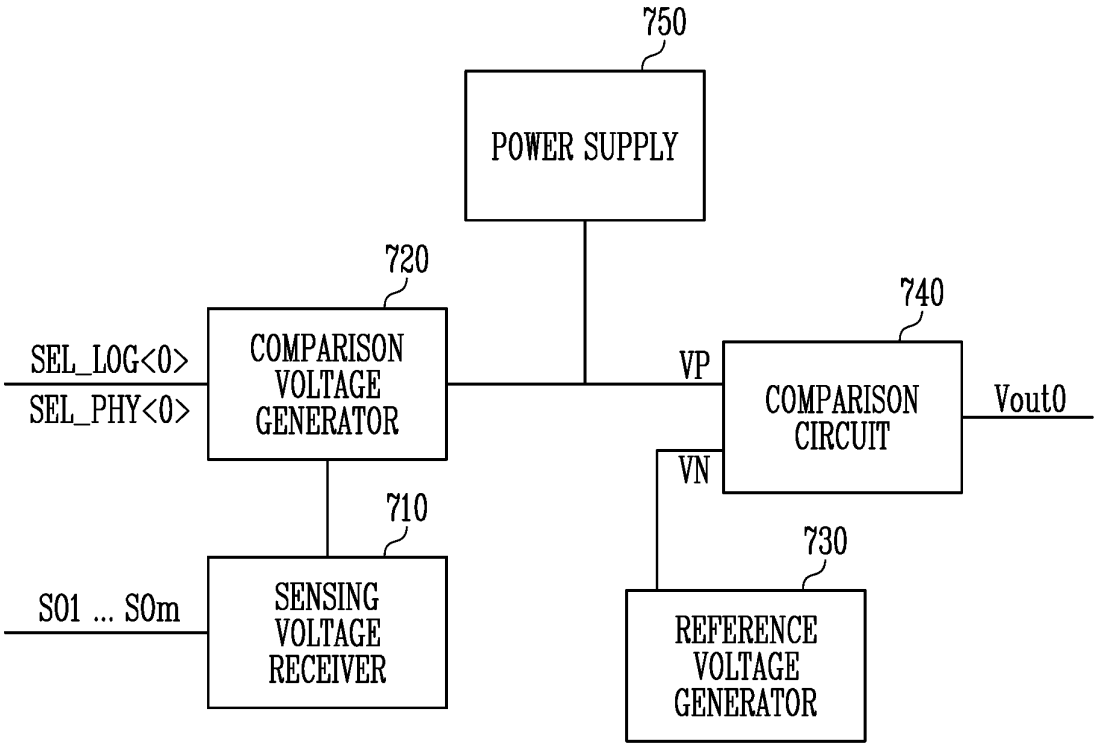

750
POWER SUPPLY
720
740
SEL_LOG<0>
SEL_PHY<0>
COMPARISON VOLTAGE GENERATOR
VP
COMPARISON CIRCUIT
Vout0
VN
710
730
S01 ... S0m
SENSING VOLTAGE RECEIVER
REFERENCE VOLTAGE GENERATOR

FIG. 8

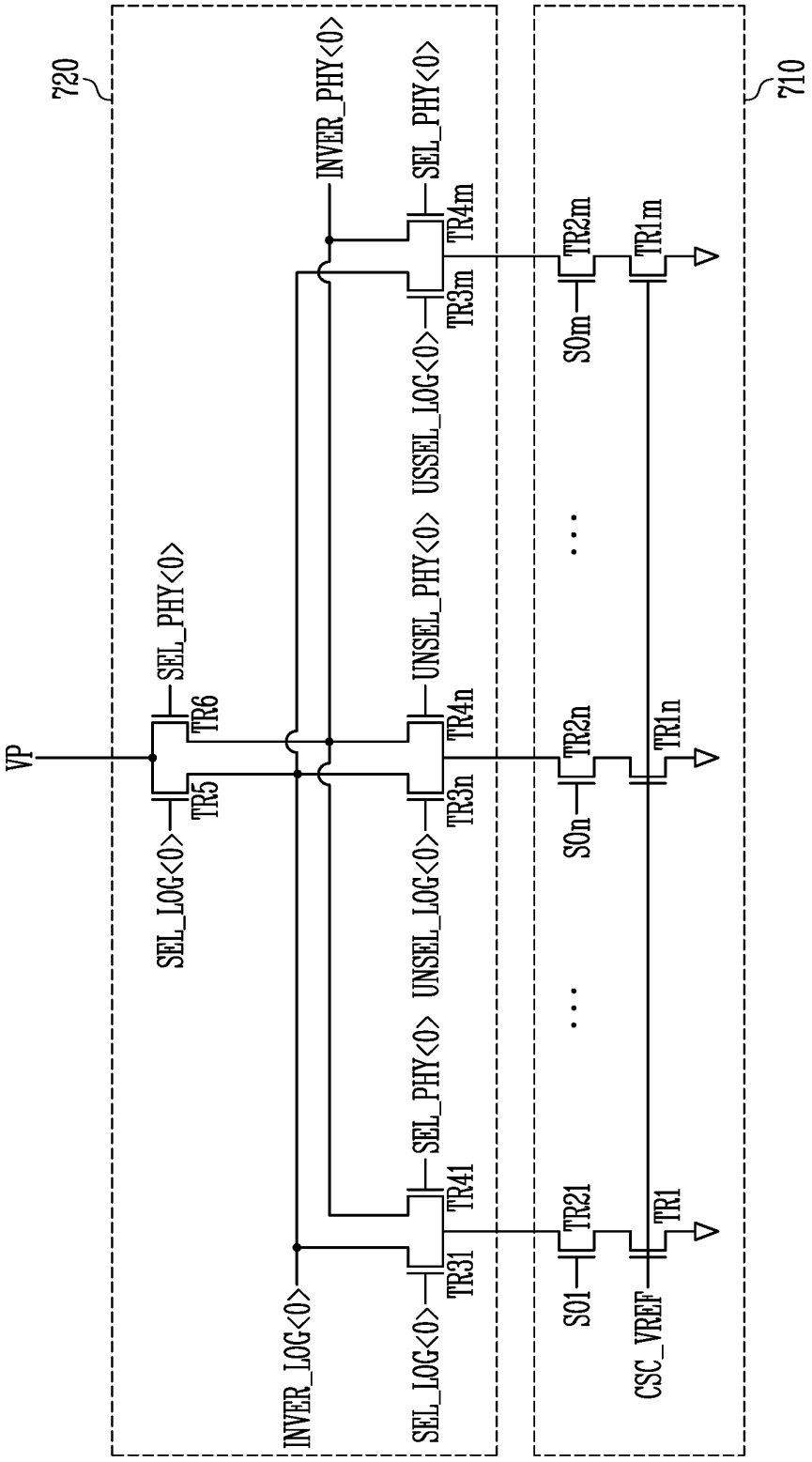

720
710
VP
SEL_PHY<0>
TR6
TR5
SEL_LOG<0>
INVER_PHY<0>
SEL_PHY<0>
TR4m
TR3m
USSEL_LOG<0>
UNSEL_PHY<0>
TR4n
TR3n
UNSEL_LOG<0>
SEL_PHY<0>
TR41
TR31
SEL_LOG<0>
INVER_LOG<0>
TR2m
TR1m
S0m
TR2n
TR1n
S0n
TR21
TR1
S01
CSC_VREF

FIG. 9

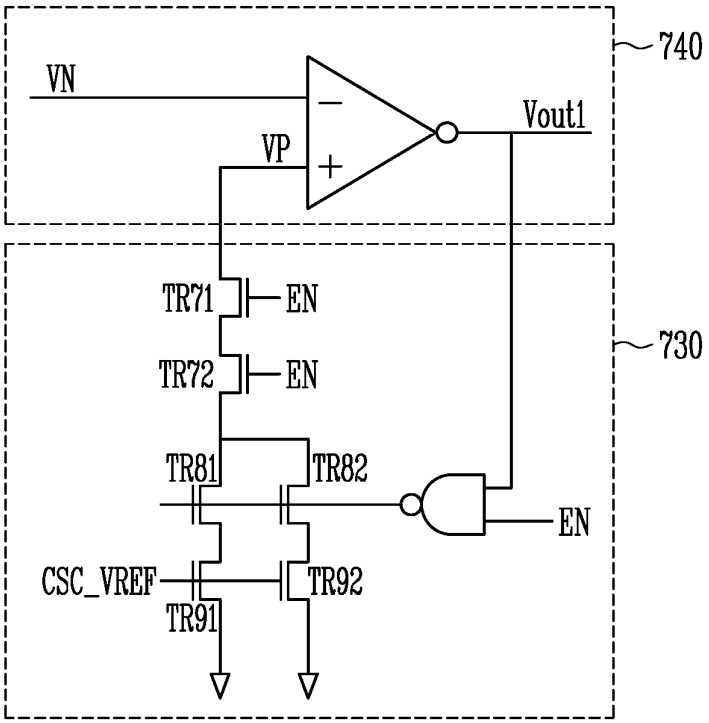

740
VN
Vout1
VP
TR71
EN
TR72
EN
730
TR81
TR82
EN
CSC_VREF
TR92
TR91

FIG. 10

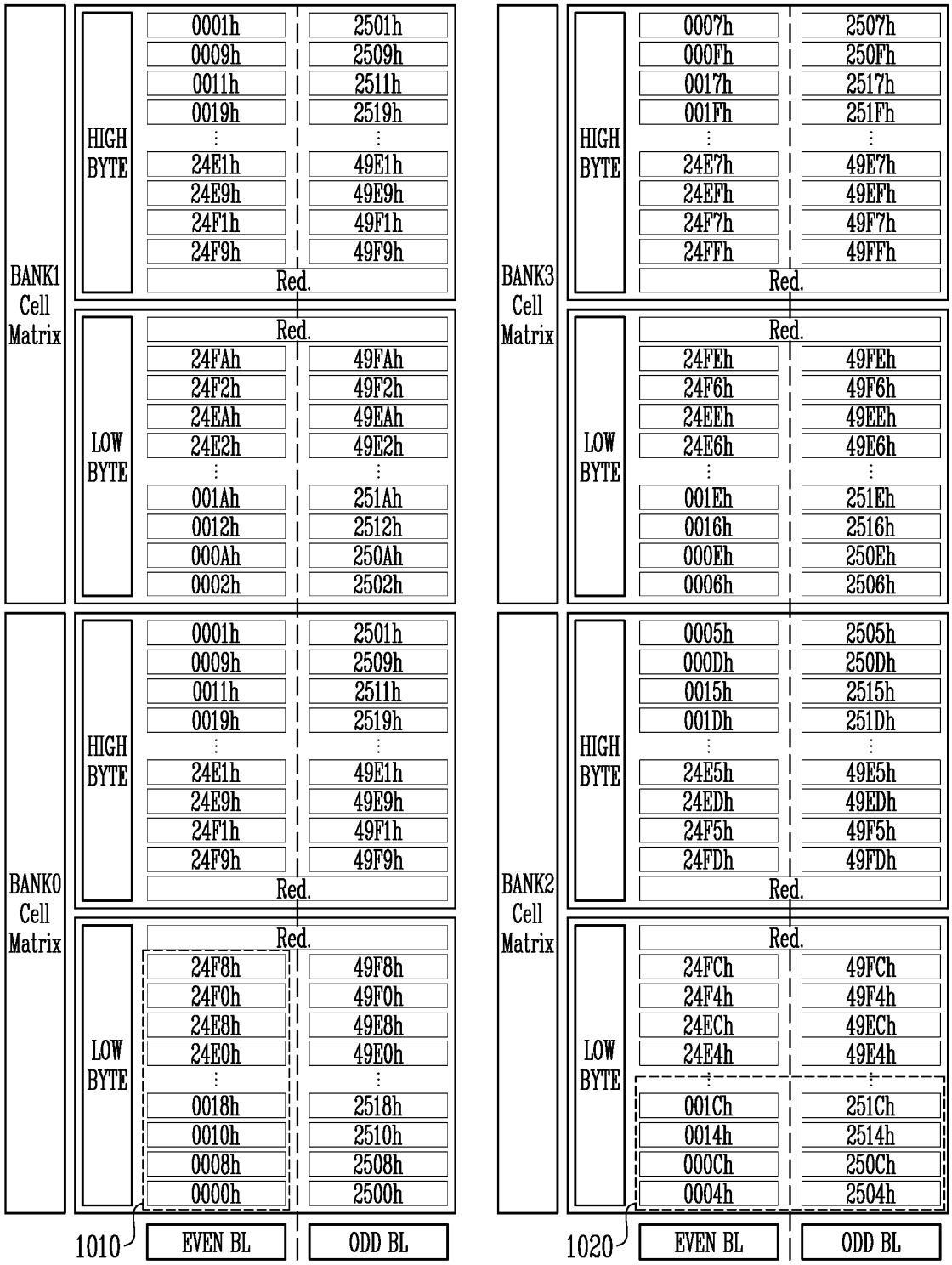

BANK1 Cell Matrix
HIGH BYTE
0001h 2501h
0009h 2509h
0011h 2511h
0019h 2519h
24E1h 49E1h
24E9h 49E9h
24F1h 49F1h
24F9h 49F9h
Red.
LOW BYTE
Red.
24FAh 49FAh
24F2h 49F2h
24EAh 49EAh
24E2h 49E2h
001Ah 251Ah
0012h 2512h
000Ah 250Ah
0002h 2502h
BANK0 Cell Matrix
HIGH BYTE
0001h 2501h
0009h 2509h
0011h 2511h
0019h 2519h
24E1h 49E1h
24E9h 49E9h
24F1h 49F1h
24F9h 49F9h
Red.
LOW BYTE
Red.
24F8h 49F8h
24F0h 49F0h
24E8h 49E8h
24E0h 49E0h
0018h 2518h
0010h 2510h
0008h 2508h
0000h 2500h
1010
EVEN BL
ODD BL
BANK3 Cell Matrix
HIGH BYTE
0007h 2507h
000Fh 250Fh
0017h 2517h
001Fh 251Fh
24E7h 49E7h
24EFh 49EFh
24F7h 49F7h
24FFh 49FFh
Red.
LOW BYTE
Red.
24FEh 49FEh
24F6h 49F6h
24EEh 49EEh
24E6h 49E6h
001Eh 251Eh
0016h 2516h
000Eh 250Eh
0006h 2506h
BANK2 Cell Matrix
HIGH BYTE
0005h 2505h
000Dh 250Dh
0015h 2515h
001Dh 251Dh
24E5h 49E5h
24EDh 49EDh
24F5h 49F5h
24FDh 49FDh
Red.
LOW BYTE
Red.
24FCh 49FCh
24F4h 49F4h
24ECh 49ECh
24E4h 49E4h
001Ch 251Ch
0014h 2514h
000Ch 250Ch
0004h 2504h
1020
EVEN BL
ODD BL

FIG. 11

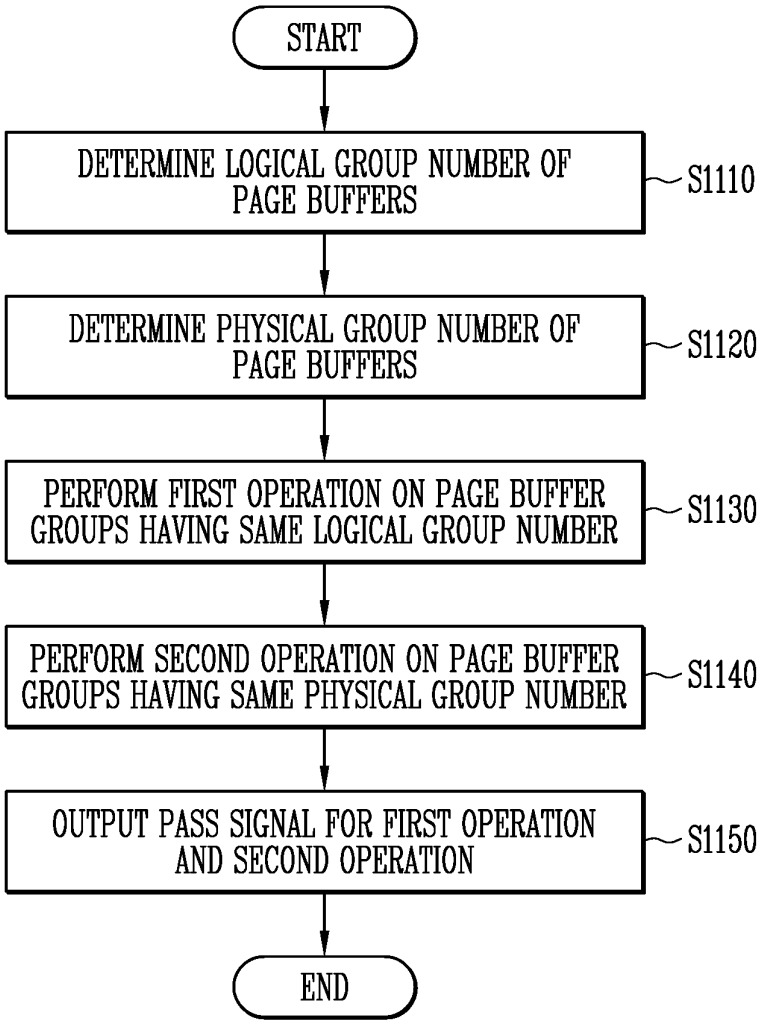

START
DETERMINE LOGICAL GROUP NUMBER OF PAGE BUFFERS
S1110
DETERMINE PHYSICAL GROUP NUMBER OF PAGE BUFFERS
S1120
PERFORM FIRST OPERATION ON PAGE BUFFER GROUPS HAVING SAME LOGICAL GROUP NUMBER
S1130
PERFORM SECOND OPERATION ON PAGE BUFFER GROUPS HAVING SAME PHYSICAL GROUP NUMBER
S1140
OUTPUT PASS SIGNAL FOR FIRST OPERATION AND SECOND OPERATION
S1150
END

FIG. 12

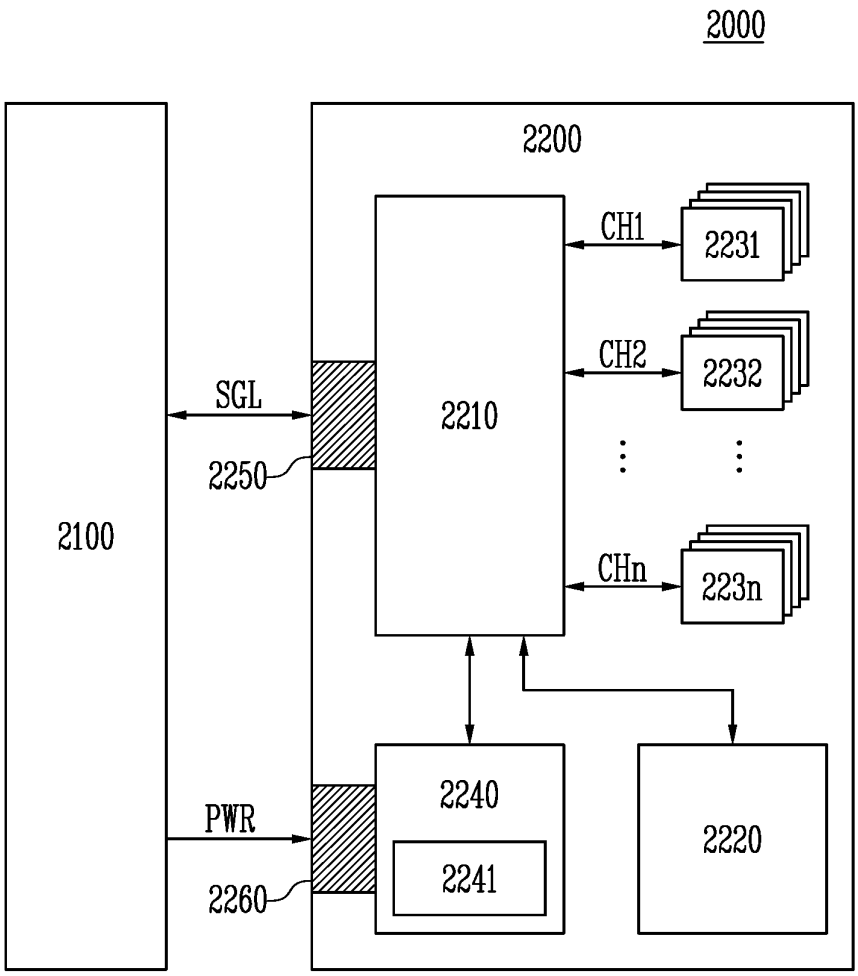

2000
2200
2100
2210
CH1
2231
CH2
2232
CHn
223n
SGL
2250
PWR
2260
2240
2241
2220

FIG. 13

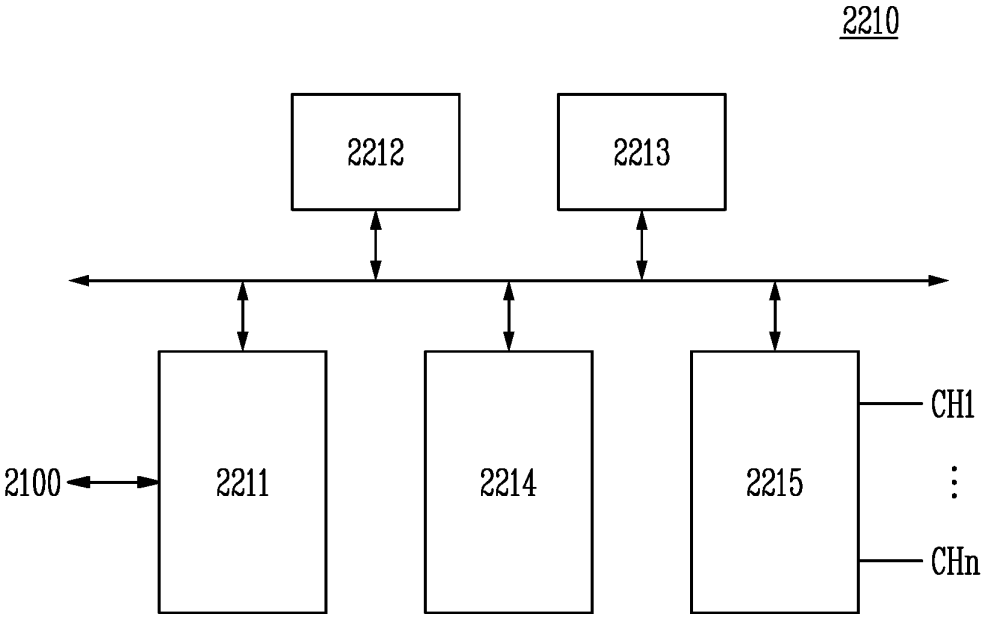

2210
2212
2213
2100
2211
2214
2215
CH1
CHn

FIG. 14

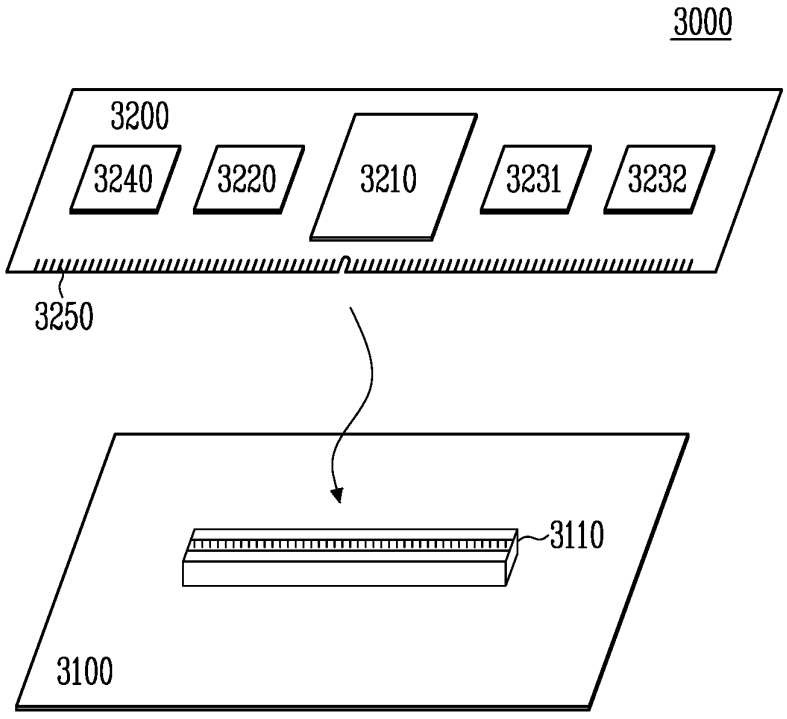

3000
3200
3240
3220
3210
3231
3232
3250
3110
3100

FIG. 15

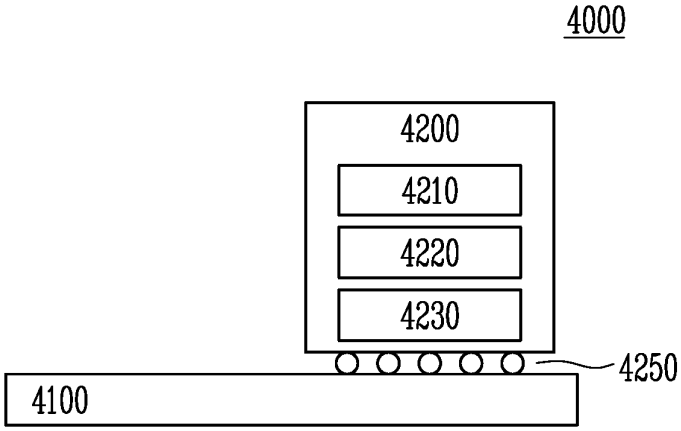
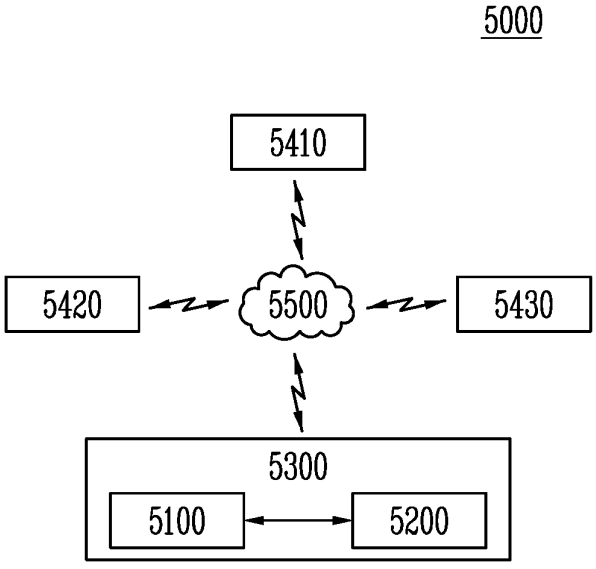

4000
4200
4210
4220
4230
4250
4100

FIG. 16


5000
5410
5420
5500
5430
5300
5100
5200