

SEMICONDUCTOR DEVICE

The present invention concerns a semiconductor device and in particular to, but not exclusively to, one that includes at least a MOS transistor that is formed on a semiconductor substrate. In addition the present invention concerns a structure for protecting circuit elements such as transistors from damaging environments such as a surge input of excessive static electricity from the outside and static electricity that is generated during the production process.

Previously, protection against external surge inputs such as static electricity, were configured by combining a variety of resistances, such as diffusion resistance and polysilicon resistance, or combining diodes and transistors between the bonding pads and internal circuitry.

In recent years, the miniaturisation of the transistor has progressed because of the demand for higher speeds and higher densities. Known transistor structures include a LDD structure, in which a low concentration diffusion layer is formed on the gate end of the drain diffusion layer, or a double diffusion structure where a low concentration region is formed by using the difference between the diffusion coefficients of arsenic and that of phosphorous. These structures are used aggressively for transistors with channel lengths of only about one μm (micron) because of the problems of hot carriers. In addition, the thickness of the gate film has become thinner with the miniaturisation of transistors. For example, in the case of a 0.5 μm (micron) design rule transistor, a 10 nanometer silicon dioxide film is used as the gate film thickness.

In this manner, as the thinning of the gate film thickness has progressed along with the miniaturisation of the circuit elements, the gate film breakdown voltage has, of course, decreased. In the case of a 10 nm gate film thickness that is used in a 0.5 μm (micron) design rule, the breakdown voltage is about 10 volts.

In order to configure an integrated circuit, a sufficient amount of protection circuits have to be created in order to protect the internal circuitry from any excessive surge voltage, such as static electricity, from the outside. In addition, it is necessary to have a structure that allows protection from the static electricity that is generated by the IC production process.

In the protective circuits of the prior art, diodes or transistors were used. However, the breakdown voltage of the circuit elements that form these protective circuits do not decrease much even if the transistors have been miniaturised. For example, the drain breakdown voltage of a 0.5 μm design rule transistor is about 13 volts, which is higher than the breakdown voltage of the gate film. The problem is that before the protective circuit operates, the gate film is permanently destroyed, and so it does not function as a protective circuit.

An object of the present invention is to resolve the problem described above and offer a protective configuration with a high resistance to external surge input.

Accordingly, the present invention relates to a semiconductor device having a substrate of a first conductivity in which is formed at least one region of a second conductivity having a relatively high concentration compared to said substrate to create a diode or a transistor, a gate disposed near said region or regions and at least one protection region disposed adjacent to a respective region and adjacent said gate having a relatively low concentration compared to said or each region for protection thereof by having a lower breakdown voltage than said gate of the device.

The semiconductor device of this invention is characterised in that low voltage resistance circuit elements are formed within the semiconductor device, a protection circuit wherein a transistor or diode is comprised of a high concentration diffusion layer and a low concentration diffusion layer. Such low concentration diffusion layer has an opposite conductivity of the high concentration diffusion layer, and it is formed so that it makes contact with the high concentration diffusion layer.

In addition, in the case of a semiconductor device with a CMOS structure, a low concentration diffusion layer with the opposite conductivity is formed within the

semiconductor by using a diffusion layer that is the same as the low concentration diffusion layer of the LDD structure transistor and by forming low resistance circuit elements within the semiconductor without an increase in the number of production process steps.

Embodiments of the present invention will now be described with reference to the accompanying drawings, of which:

Figures 1(a), (b), and (c) show a top view and cross sections of a first embodiment of this invention;

Figure 2 shows a circuit diagram that applies the first embodiment of this invention;

Figures 3(a), (b) and (c) show a top view and cross sections of a second embodiment of this invention;

Figure 4 shows a circuit diagram that applies the second embodiment of this invention;

Figures 5 (a) and (b) show a top view of a cross section of a third embodiment of this invention;

Figure 6 shows a graph of breakdown voltage against impurity diffusion concentration of a p type layer in a diode;

Figure 7 shows a graph of breakdown voltage against impurity diffusion concentration of an n type layer in a diode;

Figure 8 shows a circuit diagram that applies the third embodiment of this invention;

Figure 9 shows a cross section of a fourth embodiment of this invention;

Figure 10 shows a circuit diagram that applies the fourth embodiment of this invention;

Figure 11 shows a cross section of a fifth embodiment of this invention;

Figure 12 shows a circuit diagram that applies the sixth embodiment of this invention;

Figures 13(a) and (b) show a top view and a cross section of the eighth embodiment of this invention;

Figure 14 shows a cross section of the ninth embodiment of this invention;

Figure 15 shows a cross section that is a variation of the eighth and ninth embodiments of this invention; and

Figure 16 shows cross sections that are variations of the ninth embodiment of this invention.

Figure 1 (a) shows a top view of the first embodiment of the semiconductor device of this invention. Figure 1 (b) shows a cross section of the area represented by line A-A' in figure 1 (a). Figure 1 (c) shows a cross section of the area represented by line B-B' in figure 1 (a). Here, the case of the n-channel transistor will be described. Number 101 is a p-type Si substrate, which has a resistivity of 10 ohm.cm. Because the surface of the substrate has a surface concentration of about $1 \times 10^{16} \text{ cm}^{-3}$ wells may be formed. Number 107 is the gate film, which is formed of a 10 nm SiO_2 film. Number 108 is an oxide film, usually SiO_2 film of approximately 500nm thick, for isolating the circuit elements and which is formed by a method such as the LOCOS method.

Because number 107 and number 108 are formed on the same SiO_2 film, they are connected at the ends. The gate electrode 105 is formed by depositing polysilicon or depositing polysilicon and refractory metal silicide, such as WSi, in a layer that is about 300 nm in thickness. Number 103 is an n-type low concentration diffusion layer with concentration of $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$, which becomes the offset region. It is formed by implanting phosphorous in a concentration from $1 \times 10^{13} \text{ cm}^{-2}$ to $5 \times 10^{14} \text{ cm}^{-2}$ using ion implantation after forming the gate electrode 105. When this phosphorous ion implantation takes place, the n-type layer is formed, in the designated region, by using photoresist to form the designated pattern, as in figure 1(a).

Number 106 is a p-type diffusion layer. As in number 103, after forming the designated pattern using a photoresist, a p-type layer with a concentration from $5 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$ is formed by ion implantation of boron from $5 \times 10^{12} \text{ cm}^{-2}$ to $5 \times 10^{14} \text{ cm}^{-2}$. Subsequently, the side walls of number 104 are formed by forming a

SiO₂ film and etching the entire surface. Next, a high concentration diffusion layer 102, with a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$ is formed by implanting phosphorous of from $1 \times 10^{15} \text{ cm}^{-2}$ to $1 \times 10^{16} \text{ cm}^{-2}$. Finally, contacts and aluminium interconnects (not illustrated) are formed to obtain the semiconductor device of this invention.

The portion indicated by figure 1(c) operates as a transistor. Since it has an LDD structure as in the prior art, it creates transistors with little deterioration due to hot carriers. However, when considering the breakdown voltage of this transistor, the breakdown voltage is determined by the region in which the p-type layer 106 and high concentration n-type layer 102 make contact. That is, illustrated in figure 1(b).

For example, if the concentration of number 106 were set at $1 \times 10^{18} \text{ cm}^{-3}$, the transistor breakdown voltage would be about 7 volts. Since this is sufficiently below the gate film voltage resistance of 10 volts, even if static electricity should enter it, the transistor is sufficiently protected. Moreover, because the number 106 p-type diffusion layer concentration can be controlled freely by means of the amount of ion implantation, the breakdown voltage also can be freely controlled. Thus, this invention can be applied even in cases in which the circuit element is further miniaturised where the gate film becomes thinner and the gate film voltage resistance decreases further.

Figure 2 shows a circuit example that applies this invention. Number 203 is the bonding pad that creates the contact with the outside. Number 201 is a depletion n-channel transistor that is connected as a load. Number 202 is an n-channel transistor in which the breakdown voltage that applies to this invention has been reduced. By using this in this manner, the internal circuitry can be protected from the static electricity that enters from the outside. In addition, by applying the transistors of this invention as transistors that are used in the internal circuitry, even if static electricity is generated in the middle of the production process, the circuit elements are protected. This embodiment has been described with an n-channel transistor. Naturally, it may be applied to a p-channel transistor as well.

Figure 3 shows the second embodiment. It is an example of applying the first embodiment to the CMOS structure and then reducing the number of production process steps. Figure 3(a) shows a top view of the second embodiment. Figure 3(b) shows a cross section of the area represented by line C-C' in figure 3(a). Figure 3(c) shows a cross section of the area represented by line D-D' in figure 3 (a).

Number 301 is a p-type substrate. Number 304 is an n-well that is formed in the p-type substrate 301. Number 311 is a p-channel transistor formed in the n-well. Number 312 is an n-channel transistor formed in the p-type substrate. Number 302 is the gate film, which, like the first embodiment, has a SiO₂ layer that is 10 nm thick. Number 303 is an oxide layer for isolating the circuit elements. Number 305 is the gate electrode. Number 306 is the n-type diffusion layer that will become the source and drain of the n-channel transistor. It is formed at a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$.

Number 310 is a side wall which, for example, is formed of an oxide film, just as in the first embodiment. Number 308 is an n-type low concentration diffusion layer which is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. Number 307 is a p-type diffusion layer, which will become the source and drain of the p-channel transistor, which is formed so that it has a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$. Number 309 is a p-type low concentration diffusion layer, which is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$.

The n-type low concentration layer 308 will become the LDD structure offset in the n-channel transistor. The same n-type low concentration diffusion layer will be formed at the offset region of the p-channel transistor and decrease the breakdown voltage of the p-channel transistor. In the same manner, the p-type low concentration diffusion layer 309 will become the LDD structure offset in the p-channel transistor. The same p-type low concentration diffusion layer will be formed at the offset region of the n-channel transistor and reduce the breakdown voltage of the n-channel transistor.

The low concentration diffusion layers 308 and 309 are formed by ion implantation of phosphorous and boron, respectively, after forming the designated

pattern using a photoresist. Therefore, the formation of the low concentration diffusion layer for reducing the voltage resistance is possible by merely changing the photoresist pattern, making the formation possible without having to increase the number of production process steps.

In addition, in figure 3, the embodiment concerns the case in which transistors with an LDD structure are used in both the n-channel and the p-channel. However, if only one channel has the LDD structure, for example, in the case of an n-channel LDD and a p-channel single drain structure, it is possible to reduce the breakdown voltage of the p-channel transistor by forming an n-type low concentration diffusion layer on the p-channel transistor.

Figure 4 shows a circuit diagram that applies the second embodiment of this invention. Number 401 is a bonding pad. Number 402 is the p-channel transistor that applies this invention. Number 403 is the n-channel transistor that applies this invention. For example, when the concentrations of diffusion layers 308 and 309 are each set to $1 \times 10^{18} \text{ cm}^{-3}$, the transistor breakdown voltage is about 7 volts. Because this is sufficiently below the gate film breakdown voltage of 10 volts, even if static electricity enters the semiconductor device, the transistor will be adequately protected. In addition, because low breakdown voltage circuit elements have been formed on both the grounding side and the power supply side, it is effective against both positive and negative static electricity.

Figure 5 shows the third embodiment of this invention when applied to a diode. Figure 5 (a) shows a top view, while Figure 5 (b) shows a cross section of the area represented by line E-E' of Figure 5 (a). The case of the n-p diode will be described here. Number 501 is a p-type silicon substrate, a 10 ohm.cm substrate. Because the surface of the substrate has a surface concentration of about $1 \times 10^{16} \text{ cm}^{-3}$, wells may be formed. Number 507 is the gate film, which is formed of a 10 nm SiO_2 film. Number 502 is an oxide film for isolating the circuit elements, of a thickness of about 500 nm and which is formed by means of the LOCOS method or other such methods.

Because number 507 and number 502 are formed of the same SiO_2 film, they are connected at the ends. Number 503 is the gate electrode, which is formed of a deposited polysilicon or deposited polysilicon and refractory metal silicide such as WSi, in a layer that is about 300 nm in thickness. Number 506 is a p-type diffusion layer which is formed so that it has a concentration from $5 \times 10^{16} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$ by boron ion implantation from $5 \times 10^{12} \text{ cm}^{-2}$ to $5 \times 10^{14} \text{ cm}^{-2}$.

Subsequently, the side walls of number 504 are formed by forming a SiO_2 film and etching the entire surface. Next, a high concentration diffusion layer 505, with a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$ is formed by phosphorous ion implantation from $1 \times 10^{15} \text{ cm}^{-2}$ to $1 \times 10^{16} \text{ cm}^{-2}$. Finally, the contacts and aluminium interconnects (not illustrated) are formed to obtain the semiconductor device of this invention.

When considering the breakdown voltage of this diode, the breakdown voltage is determined by the region in which the p-type layer 506 and the high concentration n-type layer 505 make contact.

For example, if the concentration of 506 were set at $1 \times 10^{18} \text{ cm}^{-3}$, the diode breakdown voltage would be about 7 volts. Since this is sufficiently below the gate film voltage resistance of 10 volts, even if static electricity should enter the semiconductor device, the transistor is sufficiently protected. Moreover, because the concentration of the p-type diffusion layer 506 can be freely controlled by means of the amount of ion implantation, the breakdown voltage also can be freely controlled. Thus, this invention can be applied even in cases in which the circuit element is further miniaturised where the gate film becomes thinner and the gate film voltage resistance decreases further.

Figure 6 shows the relationship between the breakdown voltage of the diode that is comprised of N-type high concentration diffusion layer 505 and a p-type low concentration diffusion layer 506 against the amount of ion implantation for forming the p-type low concentration diffusion layer 506.

The n-type high concentration diffusion layer is formed by implanting arsenic As.

As shown in figure 6, when the P⁻ dose is set at $1 \times 10^{13} \text{ cm}^{-2}$, the breakdown voltage of the diode would be 8 volts.

As shown in Figure 6 the breakdown voltage can be freely controlled by selecting the P⁻ dose.

Naturally, this diode structure can also be applied to a p-type high concentration diffusion layer and an n-type low concentration diffusion layer.

Figure 7 shows the relationship between breakdown voltage of such a diode against the amount of ion implantation for forming the n-type low concentration diffusion layer.

In this case, the breakdown voltage can be freely controlled by the n-dose as well as in the case of figure 6.

Figure 8 is an example that applies this invention. Numbers 801 and 808 are the bonding pads that create the contact with the outside. Number 801 is the output pin. Number 808 is the input pin. Numbers 802 and 805 are the depletion n-channel transistors that are connected as the load. They form an inverter along with numbers 803 and 806 respectively. Numbers 804 and 807 are diodes with the reduced breakdown voltage applying this invention. By using them in this manner, the internal circuits can be protected from static electricity from the outside. In this case, the n-channel transistor was applied. Naturally, the p-channel transistor may be applied as well.

Figure 9 is a cross section that shows the fourth embodiment of this invention. It is an example of applying the third embodiment to the CMOS structure and then reducing the number of production process steps.

Number 901 is a p-type substrate. Number 902 is an n-well that was formed within the p-type substrate. Number 903 is a p-channel transistor formed in the n-well. Number 904 is an n-channel transistor formed in the substrate. Numbers 905 and 906 are n-p and p-n diodes that were formed in accordance with this invention. Number 908 is the gate film, which, like the first embodiment, has an SiO₂ layer that is 10 nm thick. Number 909 is an oxide layer for isolating the circuit elements. Number 907 is the gate electrode. Number 910 is the n-type diffusion layer that will become the source and

drain of the n-channel transistor, which is formed at a concentration of from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$.

Number 911 is a side wall which, for example, is formed of an oxide film, just as in the first embodiment. Number 912 is an n-type low concentration diffusion layer, which will become the offset of the LDD structure in the n-channel transistor and is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. Number 914 is a p-type diffusion layer, which will become the source and drain of the p-channel transistor, which is formed so that it has a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$. Number 913 is a p-type low concentration diffusion layer, which will become the offset of the p-channel transistor and is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$.

In the diode region 905, the n-type diffusion layer 910 is formed at the end of side wall 911 and the p-type low concentration layer 913 is formed up to the gate end which exists below the side wall. Contrary to this, in the diode region 906, the p-type diffusion layer 914 is formed at the end of the side wall and the n-type low concentration diffusion layer 912 is formed up to the gate end which exists below the side wall.

When considering the 905 and 906 diode breakdown voltage, the diode breakdown voltage can be lowered because the n-type diffusion layer 910 makes contact with the p-type low concentration diffusion layer 913. The diode 906 breakdown voltage can be reduced in the same manner. When considering a specific breakdown voltage value, the breakdown voltage is about 7 volts due to the p-type low concentration region 913 and the n-type low concentration region 912 having a concentration of $1 \times 10^{18} \text{ cm}^{-3}$.

The low concentration diffusion layers 912, 913 are formed by implanting phosphorous and boron, respectively, through ion implantation after forming the designated patterns. Therefore, the formation of the low concentration diffusion layers, for reducing the breakdown voltage, can take place by merely changing the photoresist pattern, and can be formed at the same time as the transistor offset. This means these layers can be formed without increasing the number of production process steps.

In addition, Figure 9 concerns an example that uses transistors in which the n-channel and p-channel have an LDD structure. However, when only one channel has an LDD structure, for example, in a case in which the n-channel has an LDD structure and the p-channel has a single drain structure, it is possible to reduce the breakdown voltage of the p-channel by forming an n-type low concentration diffusion layer in a p-channel transistor.

Figure 10 is a circuit diagram that applies the fourth embodiment of this invention. Numbers 1001 and 1002 are the bonding pads. Number 1001 is the output pin. Number 1002 is the input pin. Numbers 1003 and 1005 are p-channel transistors, each forming a pair with the n-channel transistors, numbers 1004 and 1006, respectively, as well as forming an inverter. Numbers 1007 and 1010 are p-n diodes according to this invention. Numbers 1008 and 1009 are n-p diodes according to this invention. For example, when the ion implantation concentration of layers 912 and 913 are each set to $1 \times 10^{18} \text{ cm}^{-3}$ the transistor breakdown voltage is about 7 volts which is sufficiently below the 10 volt gate film breakdown voltage. Therefore, even if the static electricity enters the semiconductor device, the diode will break and the transistors will be adequately protected. In addition, on both the grounding side and the power supply side there are formed low voltage resistance diodes, which are effective against both positive and negative static electricity.

Embodiments that are the same as the fourth embodiment can be implemented by other methods. A method that forms a low voltage resistance diode without using the end of the gate has been disclosed in Japanese laid open patent publication number Hei 1-166562. However, the fifth embodiment of this invention is an example that applies a low voltage resistance diode that is formed without using the end of a gate to CMOS but which does not increase the number of production process steps.

A cross section of the fifth embodiment is shown in Figure 11. Number 1101 is a p-type substrate. Number 1102 is an n-well that was formed within the p-type substrate 1101. Number 1103 is a p-channel transistor formed in the n-well. Number 1104 is an n-channel transistor formed in the p-type substrate. Numbers 1105 and 1106

are n-p and p-n diodes that were formed according to this invention. Number 1108 is an n-type diffusion layer that will become the source and drain of the n-channel transistor and is formed at a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$.

Number 1109 is an n-type low concentration diffusion layer, which will become the LDD structure offset in the case of an n-channel transistor. It is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. At the same time, the n-type low concentration diffusion layer is formed in this p-n diode region 1106 so that it will also make contact with a p-type diffusion layer 1107. Number 1107 is the p-type diffusion layer that will become the source and drain of the p-channel transition. It has a concentration from $1 \times 10^{20} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$. Number 1110 is a p-type low concentration diffusion layer, which will become the offset of the p-channel transistor and is formed so that it has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. At the same time the p-type low concentration diffusion layer 1110 is formed within the n-p diode region 1105 so that it makes contact with an n-type diffusion layer 1108. By having a structure such as this, a low breakdown voltage diode can be created without an increase in the number of production process steps.

Comparing the fifth embodiment with the third and fourth embodiments, in the third and fourth embodiments, the formation of a low concentration diffusion layer is possible in a self-alignment manner by means of the gate electrode. Accordingly, the density of the circuit elements improves. In addition, properties such as breakdown voltage can be more stabilised.

The sixth embodiment of this invention is one that further promotes the lowering of voltage resistance of the third embodiment. For the purpose of description, an n-p diode will be used. Figure 12 shows a top view of the sixth embodiment of this invention. In the third embodiment in Figure 5, gate electrode 503 was formed so that it covered the entire circuit element isolation region, the p-type low concentration diffusion layer 506 was formed all round the diode and made contact with the n-type diffusion layer 505 around the entire periphery.

In contrast to this, in the case of the sixth embodiment in Figure 12, gate electrode 1201 is formed such that a portion of a circuit element isolation region 1002 is exposed. As a consequence, p-type low concentration diffusion layer 1203 is formed only on two parts of the diode. Number 1205 is the n-type high concentration diffusion layer. At intersecting point 1204 between the circuit element isolation region and the p-type low concentration diffusion layer 1203, the p-type reversal prevention stopper that is formed at the bottom of the circuit element isolation region intersects with the p-type low concentration diffusion layer 1203, resulting in a further increase in the p-type concentration and allowing a further decrease in the breakdown voltage of the diode.

For example, when $1 \times 10^{18} \text{ cm}^{-3}$ is the concentration of p-type low concentration layer 1203 and the p-type reversal prevention stopper 1202 is formed with a concentration of $5 \times 10^{17} \text{ cm}^{-3}$, the diode breakdown voltage is about 6.2 volts, allowing a lower breakdown voltage than the approximately 7 volts of the third embodiment.

The seventh embodiment of this invention applies CMOS to the sixth embodiment of this invention. The cross sectional structure is the same as in Figure 9. However, as in Figure 12 in the case of the flat region of the low voltage resistance diode, a portion of the gate electrode is formed so that the circuit element isolation region is exposed, and there is an intersection point between the circuit element isolation region and the low concentration diffusion layer. In addition, as in the fourth embodiment, the low concentration diffusion layer, which is formed on the diode region, is also used as the offset of the LDD transistor. By having a structure such as this one, a lower breakdown voltage diode than that in the fourth embodiment can be created with absolutely no increase in the number of production process steps.

In the second, fourth and seventh embodiments described above, two types of diodes have been fabricated, the n-p diode and the p-n diode. However, it goes without saying that in a CMOS structure in which the n-channel has an LDD structure and the p-channel has a single drain structure, it is appropriate to form only a p-n diode in which

the n-type low concentration diffusion layer that becomes the n-channel offset makes contact with the p-type diffusion layer that forms the drain of the p-channel transistor.

The eighth embodiment of this invention is an example of the fifth embodiment in which a diode is formed between power supplies. Figure 13 (a) shows a top view of the eighth embodiment of this invention. Figure 13 (b) shows a cross section of the area represented by line F-F' in Figure 13 (a). Here, a description will be given of an example in which a p-type substrate is used. However, of course, an n-type substrate may also be used.

Number 1301 is the p-type substrate. For example, a 10 ohm.cm substrate is used. Number 1302 is the n-well region formed in the p-type substrate. P-channel transistor 1304 is formed in the n-well. The n-channel transistor (not illustrated) is formed in the p-type substrate. Around the n-well, n-type high concentration diffusion layer 1303, which has a concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or higher is formed as the n-type diffusion layer for obtaining the n-well electrical potential VDD. Normally, the same diffusion layer is used for the source and drain of the n-channel transistor. However, they may also be fabricated separately.

P-type high concentration diffusion layer 1305 is formed so that it has a concentration of $1 \times 10^{20} \text{ cm}^{-3}$ or higher as the p-type diffusion layer for obtaining the p-type substrate electrical potential VSS and is formed opposite to the n-type high concentration diffusion layer. P-type diffusion layer 1305 normally is formed at the same time as p-type diffusion layer 1306, which will become the source and drain of p-channel transistor 1304. P-channel transistor 1304 has an LDD structure and is formed so that low concentration diffusion layer 1307 has a concentration from $1 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$.

This embodiment is one that fabricates the low breakdown voltage diode used by the fifth embodiment between the VDD and VSS power supplies, and number 1308 is the same p-type low concentration diffusion layer as number 1307. Because number 1308 is formed at the same time as number 1307, it is possible to form a low breakdown voltage diode between the power supplies without adding additional production process

steps. In addition, even when static electricity enters between the power supplies, it is possible to avoid the static electricity through this low breakdown voltage diode and so the transistors fabricated on the inside will be protected. By fabricating the low breakdown voltage diode between the power supplies, it is possible to fabricate a semiconductor device with a large surface area and a large static electricity resistance.

The ninth embodiment of this invention is the fourth embodiment of this invention applied to a diode formed between the power supplies. Figure 14 shows a cross section of the ninth embodiment of this invention. An n-well is formed within p-substrate 1401. P-channel transistor 1403 is formed within n-well 1402. Number 1404 is the n-type diffusion layer for gaining the electrical potential of the n-well, just as in the eighth embodiment. Number 1405 is the p-type diffusion layer for obtaining the electrical potential of the p-type substrate.

Similar to the eighth embodiment, in order to give the diode between the power supply a low voltage resistance, the p-type low concentration diffusion layer 1406 is fabricated such that it makes contact with number 1404 and the p-type low concentration diffusion layer 1406 is the same diffusion layer 1407 of the p-channel transistor which has an LDD structure. In this embodiment, the p-type low concentration diffusion layer 1406 is formed in a self-alignment manner on the bottom of side wall 1409, which is formed on the side of gate electrode 1408. In contrast to the eighth embodiment, the ninth embodiment allows a reduction in the width of number 1406 because the p-type low concentration diffusion layer 1406 can be formed in a self-alignment manner by means of the gate electrode. This realises the stabilisation of breakdown voltage and the miniaturisation of the device.

In the eighth and the ninth embodiments, the diode fabricated between the power supplies are fabricated throughout the entire well region. However, it is not necessary to fabricate them throughout this entire region. They may be fabricated only on a portion of the well region. In addition, in the eighth and ninth embodiments, the n-type high concentration diffusion layer and the p-type low concentration diffusion layer that is used for the p-channel offset are fabricated so that they make contact. However, as in Figure

15, p-type high concentration diffusion layer 1501 and n-type low concentration diffusion layer 1502, which is used for the n-channel offset, may be allowed to make contact.

In addition, in the ninth embodiment, the diode between the power supplies may be fabricated such that gate electrode covers the circuit element isolation region 1602, as shown in Figure 16 (a). The intent of this invention will not be obstructed in the least by fabricating a portion of gate electrode 1603 on top of the circuit element isolation region 1604, as shown in Figure 16 (b).

As described above, by fabricating the transistors and diodes formed inside of the protection circuitry and inside of the semiconductor device or by fabricating the diode formed between the power supplies comprising the high concentration diffusion layer and the low concentration diffusion layer, which has the opposite conductivity of the high concentration diffusion layer and is formed such that it makes contact with the high concentration diffusion layer it is possible to fabricate low breakdown voltage circuit elements within the semiconductor device. Thus a semiconductor device can be created that can be protected from the surge inputs from the outside, such as static electricity.

In addition, in a semiconductor device with a CMOS structure, by using the opposite conductivity low concentration diffusion layer and by using the same diffusion layer as the low concentration diffusion layer of the LDD structure transistor, low breakdown voltage circuit elements can be fabricated within the semiconductor device without increasing the number of production process steps.

The foregoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.



CLAIMS

1. A semiconductor device having a substrate of a first conductivity in which is formed at least one region of a second conductivity having a relatively high concentration compared to said substrate, a gate disposed near said region or regions to create a diode or a transistor and at least one protection region disposed adjacent a respective region and adjacent said gate having a relatively low concentration compared to said or each region for protection thereof by having a lower breakdown voltage than said gate of the device.
2. A semiconductor device as claimed in claim 1, in which said protection region is formed of the first conductivity.
3. A semiconductor device as claimed in claim 1 or 2, further comprising a well of the second conductivity formed in said substrate, having one of said regions in said well and another said region in said substrate.
4. A semiconductor device as claimed in claim 1, 2 or 3 in which said region or regions comprises a source and a drain of said transistor.
5. A semiconductor device as claimed in claim 4 when dependent on claim 3, in which one of said regions forms the diode.
6. A semiconductor device as claimed in any one of the preceding claims in which said protection region is aligned with a circuit element isolation region formed in the substrate.



7. A semiconductor device substantially as hereinbefore described with reference to any one of the figures.