

The invention relates to a storage arrangement in accordance with the first part of claim 1.

During the reproduction of television signals, it is desirable that the data stream transmitted from a transmitter be processed before display on the screen in order for example, to remove interference, to display additional information or to reproduce the reproduced picture in another raster, in another section or in another picture sequence. Since the transmission and the reproduction of the picture data do not then occur in synchronism, an intermediate storage is required. The problem thereby arises that a very large amount of data has to be intermediately stored and a rapid access to individual data items has to be provided. In principal, it would be possible to provide a first store into which the serial data stream of the transmitted signal is written and to provide a second store from which the signals that are to be displayed on the screen are read out. An appropriate re-ordering or signal processing could then be undertaken between the output of the first store and the input of the second store. However, this is expensive since the necessary stores each require storage room for a complete television picture.

A storage arrangement, consisting of a store having rows and columns, a first address buffering circuit for the rows and a second address buffering circuit for the columns as well as a first shift register having a serial input and a serial output which is connected to a parallel input and output of the store, as well as a second shift register having a serial input and a serial output which is connected to the parallel input and output of the store, is known from the IEEE Journal of Solid State Circuits, Volume SC-21, No 5, October 1986, pages 649-654, New York, US: KIYOTO OHTA et al: "A 1-Mbit DRAM with 33-MHz Serial I/O Ports". Therein however, the row or column addresses for the second shift register are not controllable independently of the row or column addresses for the first shift register.

The object of the invention is to provide a storage arrangement with which serial picture data having various addresses can, to a large extent, be read in and/or out independently of each other by using a single store.

This object is achieved in a storage arrangement in accordance with the first part of claim 1 by the features given in the characterising part.

In accordance with the invention, the data is initially written serially into the shift register and then transferred in blocks of e.g. 8 or 12 parallel bits into storage locations of the store or transferred in parallel from this into the shift register and read out from the latter in serial. Thereby, the possibility exists of correspondingly activating the other shift register during the time periods between the transferral or transmission of data blocks into the first shift register or out of the second shift register. Accordingly, different data streams having different bit rates may flow in the two shift registers without the respective other shift register being interfered with during the input or output processes. Furthermore, by appropriate switching over of the shift registers, the possibility is opened-up of simultaneously writing or reading two different data streams. Thus, one data stream may, for example, be subjected to a further processing in which e.g. some bits are additionally altered while the other data stream is simultaneously supplied to the picture tube. Moreover, the possibility exists of writing-in one data stream with a low data rate and reading out and presenting another data stream with a higher data rate twice or more times in succession.

Developments and advantageous embodiments are specified in the appendant claims. The invention will be explained more fully hereinafter by means of embodiments which are illustrated in the drawings.

Fig. 1 shows a storage arrangement in accordance with the state of the art;

Fig. 2 shows a storage arrangement in accordance with the invention;

Fig. 3 shows a development of the storage arrangement in accordance with the invention.

A store 1 having z rows and s columns is illustrated in Fig. 1. A plurality of storage locations may be allocated to the crossing points of the rows and columns in order to store different colour or brightness values. The storage locations are addressable by a first and second counter 2, 3 which make possible the separate controlling of the rows and columns. The inputs 4 and outputs 5 of the store 1 are connected to parallel inputs 6 or outputs 7 of a shift register 8. Furthermore, The shift register 8 has a serial input 9 and a serial output 10. With this storage arrangement, data can be written into the shift register 8 via the serial input 9, then be transferred

into the store 1 and, at a later time point, transferred back into the shift register 8 and read out via the serial output 10. It is clear that a simultaneous write-in and read out is not thereby possible.

The storage arrangement in accordance with the invention as illustrated in Fig. 2, contains a second shift register 11 which is connected to the store 1 via additional parallel inputs 12 and comprises a serial output 13. A third address counter 14 is allocated to this shift register which makes it possible to control corresponding rows independently of the address counter 2.

In Fig. 3, the second shift register 11 has a serial input 15 and a serial output 13 wherein the output 13 leads to a picture tube 16. Moreover, there is a counter 17 which, together with the counter 14, makes possible the independent addressing of the rows and columns. A data line is led from the picture tube 16 to the serial input 15 in order to feed back signals which have been extracted therefrom, after any requisite correction. The serial output 10 of the first shift register 8 leads to a data processor 18, which, conjointly with the incoming serial data stream, carries out a modification of the data e.g. an interpolation between adjacent lines. The output of the processor 18 leads to the serial input 9 of the shift register 8.

Additional buffer stores may be arranged between the parallel inputs 7, 12 and outputs 6 of the shift registers 8, 11 and the store 1.

The first shift register 8 may serve as a writing shift register and the second shift register as a reading shift register 11.

Thereby, the reading shift register 11 may be clocked at a higher clock frequency preferably at an integral multiple of the clock frequency of the reading shift register 8.

The address counters 2, 3, 14, 17 may be allocatable selectively to each of the inputs 7, 12 and outputs 6 of the shift register.

Also, in the case of shift registers 8, 11 which comprise a whole row, only address counters 2, 14 may be provided for the rows.

Altogether, the storage arrangement in accordance with the invention makes it possible to carry out a suppression of disturbances in the stored picture in that e.g. extremely

divergent picture signals at adjacent picture points of the picture signal are balanced out. Also, an increase in the definition can be effected in order to achieve a subjective improvement for a given bandwidth of the picture signal. Furthermore, it is possible to blend in writing or another picture into an existing picture. Moreover, sections of the picture may be enlarged. All of these processes, which are carried out with items of picture information after the writing in of the original data stream, may be realised in addition to the writing and reading of the screen. For this, it is merely necessary to establish, by means of the addressing of the storage locations, the relationship between the latter and the corresponding shift registers and to write-in or read out the data in the storage locations.

For the accommodation of the additional shift register as well as the counters for the control of the storage addresses, only a small additional amount of space is occupied in comparison with the space on the chip surface which is in total occupied by the store. It is thereby possible to accommodate the complete storage arrangement on one chip whereas double the chip surface would otherwise be necessary.

Claims

1. Storage arrangement consisting of a store (1) having rows (z) and columns (s), a first address counter (2) for the control of the rows of the store and a second address counter (3) for the control of the columns of the store as well as a first shift register (8) having a serial input (9) and a serial output (10) which is connected to a parallel data input (4) and data output (5) of the store, as well as a second shift register (11) having a serial input (15) and a serial output (13) which is connected to the parallel data input and data output of the store, characterised in that, the row addresses in the store for the second shift register (11) are controllable independently of the row addresses in the store for the first shift register (8) by means of a third address counter (14).
2. Storage arrangement in accordance with claim 1, characterised in that, the column addresses in the store for the second shift register (11) are controllable independently of the column addresses in the store for the first shift register (8) by means of a fourth address counter (17).
3. Storage arrangement in accordance with claim 1 or 2, characterised in that, buffer stores are arranged between the parallel inputs (7, 12) and outputs (6) of the shift registers (8, 11) and the store (1).
4. Storage arrangement in accordance with any one or more of the claims 1 to 3, characterised in that, the first shift register (8) serves as a writing shift register and the second shift register as a reading shift register (11).
5. Storage arrangement in accordance with claim 4, characterised in that, the reading shift register (11) is clocked at a higher clock frequency, preferably at an integral multiple of the clock frequency of the writing shift register (8).
6. Storage arrangement in accordance with any one or more of the claims 1 to 5, characterised in that, the address counters (2, 3, 14, 17) are allocatable selectively to each of the inputs (7, 12) and outputs (6) of the shift register.
7. Storage arrangement in accordance with claim 1, characterised in that, in the case of shift registers (8, 11) which comprise a whole row, only address counters (2, 14,) are provided for the rows.

