A PULSE VOLTAGE GENERATION CIRCUIT AND SEMICONDUCTOR PROCESS EQUIPMENT

TECHNICAL FIELD

[0001] The present application relates to the technical field of semiconductor manufacturing, and specifically relates to a pulse voltage generation circuit and a semiconductor process equipment.

BACKGROUND

[0002] Low-pressure, low-temperature, weakly ionized glow discharge plasma is widely used in the field of integrated circuit manufacturing, particularly in process procedures such as plasma etching and plasma-enhanced chemical vapor deposition. As the integration level of integrated circuits continues to increase and advanced process requirements such as a high aspect ratio and a high selectivity are proposed, precise and independent control of a unimodal ion energy distribution function (Ion Energy Distribution Function, IEDF) of plasma becomes increasingly important.

[0003] FIG. 1 illustrates a pulse voltage generation circuit in the prior art. The circuit uses a switching transistor T1 and a switching transistor T2 to form a half-bridge circuit, and can output an operation pulse voltage for controlling an ion distribution by alternately turning on the two switching transistors and performing processing through a subsequent-stage circuit.

[0004] As can be seen in conjunction with FIG. 1, the pulse frequency of the operation pulse voltage output by the circuit is consistent with the pulse frequency of the drive pulse voltage of the switching transistor, and the voltage amplitude of the operation pulse voltage is the amplitude of the DC voltage directly applied to the switching transistor. Therefore, the pulse frequency and the voltage amplitude of the operation pulse voltage output by the circuit directly affect the loss

of the switching transistor. That is, the higher the pulse frequency, the greater the loss of the switching transistor, and meanwhile, the higher the voltage amplitude, the greater the loss of the switching transistor. In the prior art, in order to achieve high-voltage output while satisfying the requirements for switching transistor loss, only a low-frequency operation pulse voltage can be output, resulting in an unsatisfactory control effect of the unimodal IEDF. The unimodal IEDF in the prior art has a relatively high content of low-energy peaks and differs greatly from an ideal unimodal IEDF, seriously affecting the actual process effect.

SUMMARY

[0005] In view of this, the present application is directed to providing a pulse voltage generation circuit and a semiconductor process equipment, to increase the pulse frequency of an operation pulse voltage on the basis of satisfying switching loss requirements and high-voltage output, mitigate the problem of an unsatisfactory unimodal IEDF control effect, and satisfy actual process requirements.

[0006] In a first aspect, the present application provides a pulse voltage generation circuit for a semiconductor process equipment. The circuit includes an energy storage circuit and a switch unit, and the switch unit includes a plurality of first controllable switches, where

[0007] An input terminal of the energy storage circuit is configured to be connected to a DC power supply, an output terminal of the energy storage circuit is respectively connected to an input terminal of each first controllable switch, and an output terminal of each first controllable switch is configured to be grounded;

[0008] A connection point between the energy storage circuit and each first controllable switch is configured to output an operation pulse voltage;

[0009] A control terminal of each first controllable switch is configured to be connected to a controller;

[0010] The first controllable switches are configured to be sequentially turned on under control of the controller, to output the operation pulse voltage;

[0011] Where the conduction time periods of the first controllable switches do not overlap with each other, and the conduction time periods of two first controllable switches adjacent in a conduction sequence are separated by a preset duration;

[0012] The energy storage circuit is configured to store electrical energy when any one of the first controllable switches is turned on, and release the electrical energy within the preset duration.

[0013] In one embodiment, the controller is configured to:

[0014] Output a drive pulse voltage to each first controllable switch according to preset drive pulse voltage parameters, where the drive pulse voltage is used to control a conduction state of the first controllable switch.

[0015] In one embodiment, the pulse voltage generation circuit provided in the first aspect of the present application further includes an oscillation suppression circuit, where,

[0016] An input terminal of the oscillation suppression circuit is connected to the connection point between the energy storage circuit and each first controllable switch, and an output terminal of the oscillation suppression circuit is configured to output the operation pulse voltage;

[0017] The oscillation suppression circuit is configured to suppress voltage fluctuations of the operation pulse voltage.

[0018] In one embodiment, the pulse voltage generation circuit provided in the first aspect of the present application further includes a parameter acquisition circuit, where,

[0019] The parameter acquisition circuit is configured to acquire an actual operation pulse voltage at a preset sampling point, where the preset sampling point includes at least one of the input terminal of the oscillation suppression circuit, the output terminal of the oscillation suppression circuit, or a bias electrode, and the bias electrode is located in a wafer carrier of the semiconductor process equipment.

[0020] In one embodiment, the pulse voltage generation circuit provided in the first aspect of the present application further includes a protection circuit, where,

[0021] The controller is configured to: adjust a DC voltage output by the DC power supply and/or a conduction process of each first controllable switch according to the actual operation pulse voltage.

[0022] A first connection terminal of the protection circuit is configured to be connected to the output terminal of the DC power supply, and a second connection terminal of the protection circuit is connected to the input terminal of the energy storage circuit;

[0023] The controller is connected to a control terminal of the protection circuit;

[0024] The controller is configured to: when a voltage amplitude of the actual operation pulse voltage is greater than a first preset voltage threshold, control the protection circuit to disconnect the connection between the DC power supply and the energy storage circuit and release the electrical energy stored in the energy storage circuit.

[0025] In one embodiment, the protection circuit includes a second controllable switch, a third controllable switch, and a first resistor, where,

[0026] An input terminal of the second controllable switch serves as the first connection terminal of the protection circuit;

[0027] A connection point between an output terminal of the second controllable switch and an input terminal of the third controllable switch serves as the second connection terminal of the protection circuit;

[0028] An output terminal of the third controllable switch is connected to one end of the first resistor, and the other end of the first resistor is grounded;

[0029] Control terminals of the second controllable switch and the third controllable switch are respectively connected to the controller.

[0030] In one embodiment, the energy storage circuit includes an energy storage inductor and a voltage stabilization capacitor, where,

[0031] A first end of the energy storage inductor is connected to a first end of the voltage stabilization capacitor, and a second end of the energy storage inductor serves as the output terminal of the energy storage circuit;

[0032] A second end of the voltage stabilization capacitor is configured to be grounded;

[0033] A connection point between the energy storage inductor and the voltage stabilization capacitor serves as the input terminal of the energy storage circuit.

[0034] In a second aspect, the present application provides a semiconductor process equipment, including a process chamber, a controller, and the pulse voltage generation circuit according to any one of the first aspect of the present application, where,

[0035] A wafer carrier is disposed in the process chamber, and a bias electrode is disposed in the wafer carrier;

[0036] The controller is electrically connected to the control terminal of each first controllable switch of the pulse voltage generation circuit;

[0037] The output terminal of the pulse voltage generation circuit is connected to the bias electrode;

[0038] The controller is configured to control the pulse voltage generation circuit to output an operation pulse voltage to the bias electrode, to control an ion energy distribution.

[0039] In one embodiment, the semiconductor process equipment provided in the second aspect of the present application further includes an RF coil, a matcher, and an RF power supply, where,

[0040] The RF power supply is configured to apply RF power to the RF coil through the matcher, to excite plasma in the process chamber;

[0041] The controller is further electrically connected to the RF power supply, to control output power of the RF power supply.

[0042] In one embodiment, the semiconductor process equipment provided in the second aspect of the present application further includes an ion current detector, where,

[0043] The ion current detector is configured to collect an actual ion current of ions bombarding a wafer placed on the wafer carrier, and the actual ion current is used to characterize an actual ion flux;

[0044] The controller is further configured to adjust the RF power of the RF power supply until a deviation between the actual ion flux and a target ion flux is within a preset flux deviation range.

[0045] In one embodiment, the controller is further configured to perform the following operations:

[0046] Obtain an actual operation pulse voltage at a preset sampling point in the pulse voltage generation circuit;

[0047] Determine actual ion energy according to the actual operation pulse voltage;

[0048] Adjust a DC voltage output by a DC power supply connected to the pulse voltage generation circuit and/or a conduction process of each first controllable switch in the pulse voltage generation circuit, such that an energy distribution of the actual ion energy is a unimodal distribution.

[0049] In one embodiment, the pulse voltage generation circuit includes a protection circuit and an energy storage circuit, and the controller is further configured to perform the following operations:

[0050] If the voltage amplitude of the actual operation pulse voltage is greater than a first preset voltage threshold, control the protection circuit to disconnect the connection between the DC power supply and the energy storage circuit, and release the electrical energy stored in the energy storage circuit;

[0051] Adjust the DC voltage output by the DC power supply and/or the conduction process of each first controllable switch until the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold;

[0052] Control the protection circuit to connect the DC power supply and the energy storage circuit.

[0053] In view of the above, the pulse voltage generation circuit provided by the present application includes an energy storage circuit and a switch unit. A connection point between the energy storage circuit and each first controllable switch in the switch unit is configured to output an operation pulse voltage, and the conduction state of each first controllable switch in the switch unit is controlled by the controller. Since the first controllable switches are connected in parallel, conduction of any first controllable switch causes the output terminal of the energy storage circuit to be grounded, thereby storing electrical energy. Correspondingly, since the conduction

time periods of the first controllable switches do not overlap with each other (i.e., the first controllable switches are not turned on simultaneously), and the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated by a preset duration, all the first controllable switches are turned off within the preset duration, and the energy storage circuit releases electrical energy. Based on this arrangement, when any first controllable switch is turned on, the pulse voltage generation circuit outputs a low level, and the duration corresponding to the foregoing conduction time period is the low-level duration. Correspondingly, when all the first controllable switches are turned off, a high level voltage is output, and the foregoing preset duration is the high-level duration. The first controllable switches are sequentially turned on in the foregoing manner, such that the operation pulse voltage can be output.

[0054] It can thus be seen that the pulse frequency of the operation pulse voltage is the sum of the conduction state switching frequencies of the first controllable switches. By providing a plurality of first controllable switches, the pulse frequency of the operation pulse voltage can be effectively increased. For the first controllable switches, when the pulse frequency of the operation pulse voltage is constant, the pulse frequency is jointly shared by the first controllable switches, thereby effectively reducing the conduction state switching frequency of each first controllable switch and thus effectively reducing switching loss. Meanwhile, since the energy storage circuit can store electrical energy, the electrical energy released by the energy storage circuit within the preset duration is superimposed on the electrical energy output by the DC power supply, thereby effectively increasing the voltage amplitude of the operation pulse voltage. Therefore, the present application can increase the pulse frequency of the operation pulse voltage on the basis of satisfying switching loss requirements and high-voltage output,

thereby mitigating the problem of an unsatisfactory unimodal IEDF control effect and satisfying actual process requirements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0055] To more clearly describe the technical solutions in the embodiments of the present application or the prior art, the accompanying drawings needed in the description of the embodiments or the prior art are briefly introduced below. Apparently, the accompanying drawings in the following description illustrate some embodiments of the present application. A person of ordinary skill in the art may further obtain other accompanying drawings based on these accompanying drawings without creative efforts.

[0056] FIG. 1 is a circuit topology diagram of a pulse voltage generation circuit in the prior art.

[0057] FIG. 2 is a circuit topology diagram of a pulse voltage generation circuit provided in an embodiment of the present application.

[0058] FIG. 3 is a schematic diagram of a control timing sequence corresponding to the pulse voltage generation circuit provided in the embodiment shown in FIG. 2.

[0059] FIG. 4a to FIG. 4c are schematic diagrams of simulation control effects of pulse voltage generation using the pulse voltage generation circuit provided in an embodiment of the present application.

[0060] FIG. 5a to FIG. 5b are schematic diagrams of actual control effects of pulse voltage generation using the pulse voltage generation circuit provided in an embodiment of the present application.

[0061] FIG. 6 is a circuit topology diagram of another pulse voltage generation circuit provided in an embodiment of the present application.

[0062] FIG. 7 is a schematic diagram of a control timing sequence corresponding to the pulse voltage generation circuit provided in the embodiment shown in FIG. 6.

[0063] FIG. 8 is a circuit topology diagram of still another pulse voltage generation circuit provided in an embodiment of the present application.

[0064] FIG. 9 is a structural block diagram of a pulse voltage generation circuit provided in an embodiment of the present application.

[0065] FIG. 10 is a schematic structural diagram of an ion current detector provided in an embodiment of the present application.

[0066] FIG. 11 is a flowchart of a pulse voltage generation method provided in an embodiment of the present application.

[0067] FIG. 12 is a flowchart of another pulse voltage generation method provided in an embodiment of the present application.

[0068] FIG. 13 is a flowchart of still another pulse voltage generation method provided in an embodiment of the present application.

[0069] FIG. 14 is a flowchart of yet another pulse voltage generation method provided in an embodiment of the present application.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0070] The technical solutions in the embodiments of the present application will be clearly and completely described below with reference to the accompanying drawings in the embodiments of the present application. Apparently, the described embodiments are merely some rather than all of the embodiments of the present application. All other embodiments obtained by a person of

ordinary skill in the art based on the embodiments of the present application without creative efforts fall within the scope of the present application.

[0071] As described above, low-pressure, low-temperature, weakly ionized glow discharge plasma is widely used in the field of integrated circuit manufacturing, particularly in process procedures such as plasma etching and plasma-enhanced chemical vapor deposition. As the integration level of integrated circuits continues to increase and advanced process requirements such as a high aspect ratio and a high selectivity are proposed, control of a bimodal ion energy distribution function (Ion Energy Distribution Function, IEDF) used in an etching process has become difficult to satisfy actual application requirements, and precise and independent control of a unimodal IEDF of plasma becomes increasingly important.

[0072] FIG. 1 illustrates a pulse voltage generation circuit in the prior art. The circuit uses a switching transistor T1 and a switching transistor T2 to form a half-bridge circuit. A drain of the switching transistor T1 is connected to a DC high voltage Vbus, a source of the switching transistor T1 is connected to a drain of the switching transistor T2, and a source of the switching transistor T2 is grounded. Drive voltages between gates and sources of the two switching transistors are controlled to switch conduction states of the switching transistors, such that the two switching transistors are alternately turned on, and an operation pulse voltage for controlling an ion distribution is output after processing by a subsequent-stage circuit.

[0073] As can be seen in conjunction with FIG. 1, the pulse frequency of the operation pulse voltage output by the circuit is consistent with the pulse frequency of the drive pulse voltage of the switching transistor, and the voltage amplitude of the operation pulse voltage is the amplitude of the DC voltage directly applied to the switching transistor. Therefore, the pulse frequency and the voltage amplitude of the operation pulse voltage output by the circuit directly affect the loss

of the switching transistor. That is, the higher the pulse frequency, the greater the loss of the switching transistor, and meanwhile, the higher the voltage amplitude, the greater the loss of the switching transistor. In the prior art, in order to achieve high-voltage output while satisfying the requirements for switching transistor loss, only a low-frequency operation pulse voltage can be output. Since the frequency is not sufficiently high, plasma bombardment on a wafer surface (i.e., ion current) causes the potential of the wafer surface to increase significantly, which results in substantial broadening of the generated ion energy distribution, making it difficult to satisfy advanced process requirements such as a high aspect ratio and a high selectivity.

[0074] Although there are other technical solutions in practical applications in which a current compensation circuit is added on the basis of the circuit shown in FIG. 1, thereby adding a negative voltage ramp at one end of the output operation pulse voltage, this approach can mitigate the problem of an unsatisfactory unimodal IEDF control effect to a certain extent. However, because the fundamental problem of a low pulse frequency of the operation pulse voltage is not resolved, the practical application effect is still less than satisfactory. Meanwhile, the addition of a new circuit makes the overall circuit structure and control process more complex, increases the logic overhead of the controller, and also significantly increases the overall cost of the circuit.

[0075] To resolve the foregoing technical problems, the present application provides a pulse voltage generation circuit that increases the pulse frequency of an operation pulse voltage on the basis of satisfying switching loss requirements and high-voltage output, thereby mitigating the problem of an unsatisfactory unimodal IEDF control effect and satisfying actual process requirements.

[0076] The pulse voltage generation circuit provided by the present application is applied to a semiconductor process equipment. In practical applications, the semiconductor process equipment may be an inductively coupled plasma (ICP) etching machine, a capacitively coupled plasma (CCP) etching machine, a plasma-enhanced chemical vapor deposition (PECVD) device, or the like. In view of this, referring to FIG. 2, FIG. 2 illustrates an application scenario of the pulse voltage generation circuit provided by the present application by taking an ICP etching machine as an example. The semiconductor process equipment includes a process chamber 140, a controller 70, an RF power supply 90, an impedance matching circuit 100, and an upper electrode, where, for the ICP etching machine, the upper electrode includes a coupling coil 110, an output terminal of the RF power supply 90 is connected to the impedance matching circuit 100, and the impedance matching circuit 100 is connected to the coupling coil 110. After being started, the RF power supply 90 can apply RF power to the coupling coil 110 through the impedance matching circuit 100 and generate plasma inside the process chamber 140. A wafer carrier 130 is disposed in the process chamber 140 opposite the upper electrode. The wafer carrier 130 may, for example, include an electrostatic chuck, a mechanical chuck, or the like. A bias electrode 40 is disposed in the wafer carrier 130, and the pulse voltage generation circuit provided by the present application is configured to provide a bias voltage to the bias electrode 40 of the wafer carrier 130 in the process chamber 140. As shown in FIG. 2, the pulse voltage generation circuit includes an energy storage circuit 20 and a switch unit 30.

[0077] As shown in FIG. 2, in one embodiment, the energy storage circuit 20 includes an energy storage inductor L1 and a voltage stabilization capacitor C1, where a first end of the energy storage inductor L1 is connected to a first end of the voltage stabilization capacitor C1, and a connection point between the energy storage inductor L1 and the voltage stabilization capacitor

C1 serves as an input terminal of the energy storage circuit 20 and is connected to an output terminal of the DC power supply 10, a second end of the energy storage inductor L1 serves as an output terminal of the energy storage circuit 20 and is connected to an input terminal of the switch unit 30, and a second end of the voltage stabilization capacitor C1 is grounded. In practical applications, a μF-level capacitor is generally selected as the voltage stabilization capacitor C1 and is used to maintain the stability of a voltage output to a subsequent-stage circuit. A μH-level inductor is generally selected as the energy storage inductor L1 and is used to store energy or release energy. The specific selection of the voltage stabilization capacitor C1 and the energy storage inductor L1 needs to be determined in conjunction with factors such as a specific application scenario of the control circuit and circuit design parameters, and the present application does not limit the specific selection of the energy storage inductor L1 and the voltage stabilization capacitor C1.

[0078] As a preferred embodiment, a diode D1 is further disposed in the energy storage circuit 20 provided in this embodiment. Through the unidirectional conduction function of the diode D1, it can be ensured that the current direction on the energy storage inductor L1 remains constant, i.e., the current can only flow from the DC power supply 10 side to the switch unit 30 side, and meanwhile, LC oscillation can also be avoided.

[0079] In some embodiments, the switch unit 30 includes a plurality of first controllable switches, i.e., at least two first controllable switches. In the embodiment shown in FIG. 2, the switch unit 30 is illustrated as including two first controllable switches (i.e., a first controllable switch S1 and a first controllable switch S2). Input terminals of the first controllable switches are connected to each other and serve as the input terminal of the switch unit 30 to be connected to the output terminal of the energy storage circuit 20, and meanwhile, output terminals of the first

controllable switches are grounded. Based on the foregoing connection relationship, it can be seen that the first controllable switches in the switch unit 30 are connected in parallel, and conduction of any first controllable switch can cause the switch unit 30 to be turned on, thereby grounding the energy storage circuit 20. Correspondingly, when all the first controllable switches are turned off, the switch unit 30 can be turned off. A connection point between the input terminal of the switch unit 30 and the output terminal of the energy storage circuit 20 serves as the output terminal of the pulse voltage generation circuit and is connected to the bias electrode 40 disposed in the process chamber 140. Control terminals of the first controllable switches in the switch unit 30 are respectively connected to the controller 70, and the controller 70 can control the conduction states of the first controllable switches.

[0080] It should be noted that, in the embodiment shown in FIG. 2 and subsequent embodiments, the first controllable switch may be implemented by selecting a switching transistor such as Si, SiC, or GaN. Certainly, other controllable switching transistors that can satisfy circuit operation requirements may also be selected, and details thereof are not described one by one herein.

[0081] Based on the foregoing connection relationship, the controller 70 may be an upper-level computer or a lower-level computer, and is mainly used in the present application to control the conduction state of each first controllable switch in the switch unit 30, where the specific conduction state control rules are as follows: the first controllable switches are sequentially turned on, the conduction time periods of the first controllable switches do not overlap with each other, and the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated by a preset duration. It can be understood that sequentially turning on the first controllable switches requires the first controllable switches in the switch unit to be cyclically turned on in a preset sequence during operation of the pulse voltage generation

circuit. Taking the first controllable switch S1 and the first controllable switch S2 shown in FIG. 2 as an example, the process of sequentially turning on the two switches is: first controllable switch S1→first controllable switch S2→first controllable switch S1……, and the cycle continues in this manner until the pulse voltage generation circuit stops operating. The non-overlapping conduction time periods of the first controllable switches can ensure that no first controllable switches in the switch unit are turned on simultaneously, while separating the conduction time periods of two first controllable switches adjacent in the conduction sequence by a preset duration is used to ensure that all the first controllable switches are turned off within the preset duration.

[0082] As described above, the first controllable switches in the switch unit 30 are connected in parallel. During the process in which the controller 70 controls the first controllable switches to be sequentially turned on, conduction of any first controllable switch causes the output terminal of the energy storage circuit 20 to be grounded, and at this time, the energy storage circuit 20 stores electrical energy. Correspondingly, since the conduction time periods of the first controllable switches do not overlap with each other and the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated by a preset duration, all the first controllable switches are turned off within the preset duration, and the energy storage circuit 20 releases the electrical energy stored previously.

[0083] Based on this arrangement, when any first controllable switch is turned on, the pulse voltage generation circuit outputs a low level, and the duration corresponding to the foregoing conduction time period is the low-level duration. Correspondingly, when all the first controllable switches are turned off, a high level voltage is output, and the foregoing preset duration is the high-level duration, thereby converting the DC voltage output by the DC power supply 10 into a

pulse voltage through the switch unit 30. The controller 70 controls the first controllable switches to be sequentially turned on in the foregoing manner, such that an operation pulse voltage can be output to the bias electrode 40 through the connection point between the energy storage circuit 20 and each first controllable switch.

[0084] As shown in FIG. 2, in one embodiment, a control terminal of the DC power supply 10 is connected to the controller 70, and the controller 70 is further configured to control the DC power supply to output a DC voltage. In practical applications, the controller 70 can control the operating state of the DC power supply 10, i.e., control the DC power supply 10 to output the DC voltage or stop outputting the DC voltage. In a preferred embodiment, the output voltage of the DC power supply 10 is adjustable, and the controller 70 can adjust the amplitude of the DC voltage actually output by the DC power supply 10 according to the actual operating condition of the circuit and pulse voltage generation requirements. The output terminal of the DC power supply 10 is connected to the input terminal of the energy storage circuit 20 to output the DC voltage to the energy storage circuit 20. The specific process in which the controller 70 controls the DC power supply 10 to output the DC voltage will be described in subsequent content and is not described in detail herein for the time being.

[0085] In summary, with the pulse voltage generation circuit provided in this embodiment, the sum of the duration corresponding to the conduction time period of a first controllable switch and the preset duration is the pulse period of the operation pulse voltage. Correspondingly, the pulse frequency of the operation pulse voltage is the sum of the conduction state switching frequencies of the first controllable switches. Therefore, providing a plurality of first controllable switches can effectively increase the pulse frequency of the operation pulse voltage. For the first controllable switches, when the pulse frequency of the operation pulse voltage is constant, the

pulse frequency is jointly shared by the first controllable switches, thereby effectively reducing the conduction state switching frequency of each first controllable switch and thus effectively reducing switching loss. Meanwhile, since the energy storage circuit can store electrical energy, the electrical energy released by the energy storage circuit within the preset duration is superimposed on the electrical energy output by the DC power supply, thereby effectively increasing the voltage amplitude of the operation pulse voltage. Therefore, the present application can increase the pulse frequency of the operation pulse voltage on the basis of satisfying switching loss requirements and voltage amplitude requirements, thereby mitigating the problem of an unsatisfactory unimodal IEDF control effect and satisfying actual process requirements.

[0086] In some embodiments, since the pulse frequency of the operation pulse voltage output by the pulse voltage generation circuit provided by the present application is sufficiently high, a good unimodal IEDF control effect can still be achieved without adding another current compensation circuit. Compared with the prior art, the control process can be simplified, thereby reducing the logic overhead of the controller while effectively reducing the overall cost of the circuit.

[0087] Taking the circuit topology shown in FIG. 2 as an example, an implementation of a control signal capable of satisfying the foregoing conduction state control rules for the first controllable switches is provided below. In this embodiment, switching of the conduction state of each first controllable switch in the switch unit is driven by a pulse voltage, i.e., a high level voltage of the pulse voltage controls the first controllable switch to be turned on, and a low level of the pulse voltage controls the first controllable switch to be turned off. To distinguish this pulse voltage from the foregoing operation pulse voltage, the present application defines the

pulse voltage used to drive the conduction state of the first controllable switch as a drive pulse voltage. In practical applications, drive pulse voltage parameters, such as a pulse period, a duty cycle, and a voltage amplitude of the drive pulse voltage, may be configured for the controller according to pulse voltage generation requirements. The controller can determine the drive pulse voltage needed to be output according to the preset drive pulse voltage parameters, and after receiving a control instruction, can respectively output the drive pulse voltage to each first controllable switch.

[0088] In some embodiments, as described above, parameters such as the voltage amplitude, pulse frequency, and duty cycle of the operation pulse voltage finally output by the pulse voltage generation circuit are all affected by the switch unit. Therefore, when the parameters of the operation pulse voltage are determined, the drive pulse voltage can also be determined based on the desired parameters of the operation pulse voltage, which is of great significance in practical applications. This content will be described in subsequent content and is not described in detail herein for the time being.

[0089] The control timing sequence in which the controller controls the switch unit according to the preset drive pulse voltage may be seen in FIG. 3.

[0090] During the t_0- t_1 time period, the first controllable switch S1 is turned on, and the first controllable switch S2 is turned off. At this time, the output terminal of the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S1, the DC power supply 10 charges the energy storage inductor L1, and the output voltage of the pulse voltage generation circuit (i.e., Vout) is 0V.

[0091] During the t_1-t_2 time period (corresponding to the foregoing preset duration), the first controllable switch S1 and the first controllable switch S2 are both turned off, and the energy

storage inductor L1 in the energy storage circuit 20 releases electrical energy, which is superimposed on the electrical energy output by the DC power supply 10, thereby increasing the output voltage amplitude. Meanwhile, due to the effect of the voltage stabilization capacitor C1, the amplitude of the output voltage remains substantially constant during the stage in which both first controllable switches are turned off.

[0092] During the t_2-t_3 time period, the first controllable switch S1 is turned off, and the first controllable switch S2 is turned on. At this time, the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S2, and the DC power supply 10 continues to charge the energy storage inductor L1. Correspondingly, the output voltage of the pulse voltage generation circuit decreases to 0V again.

[0093] During the t_3-t_4 time period, the first controllable switch S1 and the first controllable switch S2 are both turned off, and the DC power supply and the energy storage inductor L1 continue to provide a high-amplitude DC voltage. At time t_4, the first controllable switch S1 is turned on, and the first controllable switch S2 is turned off. At this point, the first controllable switch S1 and the first controllable switch S2 have both completed one drive cycle, and the operation pulse voltage can be output by periodically repeating the foregoing process.

[0094] As can be seen in conjunction with FIG. 3:

[0095] First, during the t_0-t_4 time period, both the drive pulse voltage of the first controllable switch S1 and the drive pulse voltage of the first controllable switch S2 have one high-level output, while the operation pulse voltage has two high-level outputs. Therefore, the pulse frequency of the operation pulse voltage is twice the pulse frequency of the drive pulse voltage of a first controllable switch, i.e., the pulse frequency of the operation pulse voltage is the sum of the pulse frequencies of the drive pulse voltages of the first controllable switches. Therefore,

without increasing the pulse frequency of the drive pulse voltage of a controllable switch, providing a plurality of first controllable switches can significantly increase the pulse frequency of the operation pulse voltage, thereby effectively reducing the loss of the controllable switch while achieving output of an operation pulse voltage having a high pulse frequency.

[0096] Second, the voltage amplitude of the operation pulse voltage can be controlled through the switch unit. In a steady state, the amplification factor of the voltage amplitude of the operation pulse voltage finally output by the pulse voltage generation circuit relative to the DC voltage output by the DC power supply can be calculated according to the following formula:

$$N = M \times \frac{t_a - t_b}{t_c - t_d} \qquad (1)$$

[0097] Where N represents the voltage amplification factor;

[0098] M represents the number of first controllable switches in the switch unit;

[0099] t_a-t_b represents a duration in which any first controllable switch is in a conduction state;

[0100] t_c-t_d represents a preset duration by which the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated.

[0101] For example, if the frequency of the drive pulse voltages of the first controllable switch S1 and the first controllable switch S2 is 5MHz, and the duration of a conduction time period of any first controllable switch is 80ns, the pulse frequency of the output operation pulse voltage is 10MHz, and the pulse width (i.e., the high-level duration) is 20ns. If the DC voltage output by the DC power supply is 100V, the voltage amplitude of the final operation pulse voltage will be amplified to 800V. Therefore, the DC voltage output by the DC power supply can be amplified through the energy storage inductor, and the voltage amplification factor can be adjusted according to the drive pulse voltage of the first controllable switch.

[0102] It should be noted that, in the driving manner corresponding to FIG. 3, the first controllable switches use drive pulse voltages having the same pulse frequency. To satisfy the foregoing principle that the conduction time periods of the first controllable switches do not overlap with each other and the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated by a preset duration, there is necessarily a phase difference between the drive pulse voltages of the first controllable switches. As shown in FIG. 3, the phase difference between two first controllable switches adjacent in the conduction sequence should be equal to the pulse period of the operation pulse voltage expected to be output. Correspondingly, the preset duration by which the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated is the duration for which the operation pulse voltage outputs a high level voltage. In practical applications, this control may be implemented based on rising edges of the drive pulse voltages corresponding to two first controllable switches adjacent in the conduction sequence, or this control may be implemented using a falling edge of the drive pulse voltage of the first controllable switch that is turned on earlier and a rising edge of the drive pulse voltage of the first controllable switch that is turned on later. Certainly, other typical time points may also be used. Any control manner that satisfies the foregoing conduction principle is optional and, provided that it does not exceed the scope of the core concept of the present application, likewise falls within the scope of the present application.

[0103] In view of the above, taking a pulse frequency of the operation pulse voltage of 10MHz as an example, FIG. 4a to FIG. 4c are schematic diagrams of simulation control effects of pulse voltage generation using the pulse voltage generation circuit provided in an embodiment of the present application. FIG. 4a is a schematic waveform diagram of the operation pulse voltage

finally output by the pulse voltage generation circuit. When the pulse frequency of the operation pulse voltage is 10MHz and the duty cycle is 20%, the pulse width is 20ns, and the voltage amplitude of the operation pulse voltage is 5000V. Due to a parallel-plate capacitance effect between the bias electrode and the wafer, when the pulse voltage generation circuit outputs a high level voltage, a corresponding high-level voltage is also induced on the wafer surface. At this time, an accelerating electric field is formed between the high level voltage on the wafer surface and the plasma, attracting electrons to move toward the wafer surface and causing the voltage of the wafer surface to decrease. When the pulse voltage generation circuit outputs a low level, the voltage of the wafer surface becomes a negative voltage, attracting ions to move toward the wafer surface. Since the movement speed of the ions is much lower than the movement speed of the electrons, the decrease in the wafer surface voltage caused by the electrons is much greater than the increase in the wafer surface voltage caused by the ions. Since the pulse frequency of the operation pulse voltage is sufficiently high, a plurality of pulse periods are needed before a stable negative bias pulse waveform as shown by the solid line in FIG. 4b is formed on the wafer surface. In this example, ions are accelerated from the sheath field to the wafer surface during 80% of the pulse period, and electrons are accelerated to the wafer surface during the remaining 20% of the pulse period to neutralize residual positive charges on the wafer surface resulting from ion bombardment.

[0104] Generally, the time for ions to traverse the sheath field and reach the wafer surface is

$$\tau_i = 3\bar{s}\left(\frac{m_i}{2e\overline{V_s}}\right)^{\frac{1}{2}} \qquad (2)$$

[0105] Where $\bar{s}$ represents the average thickness of the sheath field;

[0106] m_i represents the ion mass;

[0107] e represents the elementary charge;

[0108] $\overline{V_s}$ represents the average sheath field voltage.

[0109] Generally, the time for ions to traverse the sheath field and reach the wafer surface is several hundred ns. Since the pulse voltage generation circuit provided by the present application can provide a high-frequency operation pulse voltage, the ions can traverse the sheath field and reach the wafer surface only after passing through a plurality of pulse periods of the operation pulse voltage. During this process, the ions cannot respond to the sheath field voltage $V(t)$ in real time, but instead experience the effect of the average sheath field voltage $V_d(t)$. At this time, the following relationship is satisfied:

$$\frac{dV_d(t)}{dt} = -\frac{V_d(t) - V(t)}{\tau_i} \qquad (3)$$

[0110] As shown in FIG. 4b, the dashed line in the figure shows that, when a high-frequency operation pulse voltage is applied to the bias electrode, the average sheath field voltage waveform experienced by the ions remains substantially constant, which produces the unimodal ion energy distribution shown in FIG. 4c.

[0111] In practical applications, the oscillation variation range of the average sheath field voltage waveform determines the broadening of the unimodal IEDF. Generally, the higher the pulse frequency of the operation pulse voltage, the more pulse periods the ions pass through when traversing the sheath field to reach the wafer surface, the more significant the effect of the average sheath field, and the smaller the ion energy broadening caused by oscillation variations of the average sheath field voltage waveform. The average energy of the ions accelerated in this case can be expressed as:

$$E_0 \approx V_0 \cdot \left(1 - \frac{T_{on}}{T}\right) \approx V_0 \cdot (1 - T_{on} \cdot f) \qquad (4)$$

[0112] Where V_0 represents the pulse voltage amplitude on the wafer surface, which is directly related to the voltage amplitude of the operation pulse voltage output by the pulse voltage generation circuit;

[0113] T_{on} represents the pulse width of the operation pulse voltage;

[0114] T represents the pulse period of the operation pulse voltage;

[0115] f represents the pulse frequency of the operation pulse voltage.

[0116] It can be seen based on formula (4) that the smaller the pulse width of the operation pulse voltage, the greater the average energy of the accelerated ions, and the higher the pulse frequency of the operation pulse voltage, the better the approximation effect of the foregoing formula, because the more pulse periods the ions pass through when traversing the sheath field to reach the wafer surface, the more significant the effect of the average sheath field and the more precise the ion energy control.

[0117] In some embodiments, referring to FIG. 5a to FIG. 5b, FIG. 5a and FIG. 5b are schematic diagrams of actual control effects of pulse voltage generation using the pulse voltage generation circuit provided in an embodiment of the present application, where FIG. 5a shows a voltage waveform induced on the wafer surface when an operation pulse voltage having a pulse frequency of 10MHz is applied to the bias electrode, and the dashed line in the figure shows the average sheath field voltage waveform actually experienced by the ions. Compared with FIG. 4a, changes in the load of the process chamber and inductance of a transmission line cause oscillations in the wafer surface voltage waveform, i.e., there is overshoot within a certain range (the -350V to -300V portion) at a falling edge of the operation pulse voltage as shown in FIG. 5a.

However, since the ions can traverse the sheath field and reach the wafer surface only after passing through a plurality of pulse periods of the operation pulse voltage, the average sheath field voltage waveform actually experienced by the ions is not affected, thereby ensuring that the actual unimodal IEDF shown in FIG. 5b has relatively small broadening, is substantially consistent with the simulation effect shown in FIG. 4c, and satisfies process requirements during actual use.

[0118] In some embodiments, referring to the embodiment shown in FIG. 6, in the pulse voltage generation circuit provided in this embodiment, the switch unit includes four first controllable switches (i.e., S1-S4), and the control timing sequence of the circuit may be seen in FIG. 7.

[0119] During the t_0-t_1 time period, the first controllable switch S1 is turned on, and the other three first controllable switches are turned off. At this time, the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S1, the DC power supply 10 charges the energy storage inductor L1, and the output voltage of the pulse voltage generation circuit (i.e., Vout) is 0V.

[0120] During the t_1-t_2 time period, all four first controllable switches are turned off, and the DC power supply 10 and the energy storage inductor L1 simultaneously provide electrical energy to the bias electrode 40.

[0121] During the t_2-t_3 time period, the first controllable switch S2 is turned on, and the other three first controllable switches are turned off. At this time, the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S2, the DC power supply 10 charges the energy storage inductor L1, and the output voltage of the pulse voltage generation circuit decreases to 0V again.

[0122] During the t_3-t_4 time period, all four first controllable switches are turned off, and the DC power supply 10 and the energy storage inductor L1 simultaneously provide electrical energy to the bias electrode 40.

[0123] During the t_4-t_5 time period, the first controllable switch S3 is turned on, and the other three first controllable switches are turned off. At this time, the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S3, the DC power supply 10 charges the energy storage inductor L1, and the output voltage of the pulse voltage generation circuit decreases to 0V again.

[0124] During the t_5-t_6 time period, all four first controllable switches are turned off, and the DC power supply 10 and the energy storage inductor L1 simultaneously provide electrical energy to the bias electrode 40.

[0125] During the t_6-t_7 time period, the first controllable switch S4 is turned on, and the other three first controllable switches are turned off. At this time, the DC power supply 10 forms a closed loop through the energy storage inductor L1 and the first controllable switch S4, the DC power supply 10 charges the energy storage inductor L1, and the output voltage of the pulse voltage generation circuit decreases to 0V again.

[0126] During the t_7-t_8 time period, all four first controllable switches are turned off, and the DC power supply 10 and the energy storage inductor L1 simultaneously provide electrical energy to the bias electrode 40. At time t8, the first controllable switch S1 is turned on, and the other three first controllable switches are turned off, and the foregoing process starts to be periodically repeated, eventually outputting an operation pulse voltage to the bias electrode 40. If the pulse frequency of the drive pulse voltages of the four first controllable switches is 5MHz, the pulse frequency of the resulting operation pulse voltage is 20MHz.

[0127] The principle by which the embodiment shown in FIG. 6 resolves the technical problem and other related control processes may all be implemented with reference to the foregoing embodiments and are not repeated herein.

[0128] It should be noted that, when the switch unit includes three or more first controllable switches, the conduction state switching frequencies of the first controllable switches may be the same (as shown in FIG. 6 and FIG. 7) or may be different (when two first controllable switches are included, the two switches are alternately turned on, and their conduction state switching frequencies are necessarily the same). Taking FIG. 6 as an example, when the drive pulse voltages shown in FIG. 7 are used, the conduction state switching frequencies of the first controllable switches are the same. In another embodiment, the pulse frequencies of the drive pulse voltages of the first controllable switch S1 and the first controllable switch S2 may be increased, or the pulse frequencies of the drive pulse voltages of the first controllable switch S1 and the first controllable switch S2 may be decreased. Certainly, there may be other adjustment manners, which are not enumerated one by one herein. In practical applications, controllable switches of different specifications may be combined according to actual needs or circuit design costs. It should be emphasized that, regardless of how the drive pulse voltages of the first controllable switches are set, the foregoing conduction principle of the controllable switches must be satisfied. Correspondingly, any control manner capable of satisfying this principle is optional and likewise falls within the scope of the present application.

[0129] It can be understood that, when the conduction state switching frequencies of the first controllable switches are different, the pulse frequency of the operation pulse voltage is still the sum of the pulse frequencies of the drive pulse voltages of the first controllable switches, while the foregoing voltage amplification factor needs to be calculated separately for each first

controllable switch according to the drive pulse voltage thereof, and the sum of the amplification factors corresponding to the first controllable switches is used as the final voltage amplification factor of the switch unit.

[0130] In some embodiments, the pulse voltage generation circuit provided in the embodiment shown in FIG. 6 further includes an oscillation suppression circuit 50. The oscillation suppression circuit 50 is connected between the switch unit 30 and the bias electrode 40 and is configured to output the operation pulse voltage, i.e., an input terminal of the oscillation suppression circuit 50 is connected to a connection point between the energy storage circuit 20 and each first controllable switch, and an output terminal of the oscillation suppression circuit 50 is connected to the bias electrode 40. The oscillation suppression circuit 50 can suppress voltage fluctuations of the operation pulse voltage output to the bias electrode 40.

[0131] In one embodiment, the oscillation suppression circuit 50 includes a diode D2, a second resistor R2, and a third resistor R3, where an anode of the diode D2 is connected to a first end of the third resistor R3, and a connection point therebetween serves as the input terminal of the oscillation suppression circuit 50, a cathode of the diode D2 is connected to a first end of the second resistor R2, a second end of the second resistor R2 is connected to a second end of the third resistor R3, and a connection point therebetween serves as the output terminal of the oscillation suppression circuit 50 and is connected to the bias electrode 40.

[0132] The pulse voltage generation circuit provided in this embodiment is provided with an oscillation suppression circuit. Through the oscillation suppression circuit, the current flowing into the plasma load of the process chamber can be relatively separated from the current flowing out of the plasma load of the process chamber, thereby suppressing pulse voltage waveform oscillations caused by line inductance between the pulse voltage generation circuit and the bias

electrode, making the operation pulse voltage output to the bias electrode more stable, and further making the wafer induced voltage more stable, thereby effectively improving the pulse voltage generation effect.

[0133] On the basis of any of the foregoing embodiments, the present application further provides another pulse voltage generation circuit. As shown in FIG. 8, the pulse voltage generation circuit provided in this embodiment further includes a parameter acquisition circuit (not shown in FIG. 8) and a protection circuit 60.

[0134] In this embodiment, the parameter acquisition circuit is mainly configured to acquire an actual operation pulse voltage at a preset sampling point, where the preset sampling point includes at least one of the input terminal of the oscillation suppression circuit 50, the output terminal of the oscillation suppression circuit 50, or the bias electrode 40. The function of each preset sampling point and the connection manner thereof with the parameter acquisition circuit will be specifically described in the subsequent embodiment shown in FIG. 9 and are not described in detail herein for the time being.

[0135] In this embodiment, the controller is further configured to adjust the output voltage of the DC power supply 10 and/or the conduction state of each first controllable switch according to the actual operation pulse voltage, thereby adjusting the operation pulse voltage finally output to the bias electrode 40. The specific adjustment process will be described in subsequent content and is not described in detail herein for the time being.

[0136] In some embodiments, as shown in FIG. 8, the protection circuit 60 is connected between the DC power supply 10 and the energy storage circuit 20. In one embodiment, the protection circuit includes a second controllable switch Sp, a third controllable switch Sq, and a first resistor R1. Specifically, an input terminal of the second controllable switch Sp serves as a first

connection terminal of the protection circuit 60 and is connected to the output terminal of the DC power supply 10, an output terminal of the second controllable switch Sp is connected to an input terminal of the third controllable switch Sq, and a connection point therebetween serves as a second connection terminal of the protection circuit 60 and is connected to the input terminal of the energy storage circuit 20. An output terminal of the third controllable switch Sq is connected to one end of the first resistor R1, and the other end of the first resistor R1 is grounded. Control terminals of the second controllable switch Sp and the third controllable switch Sq are respectively connected to the controller.

[0137] In this embodiment, the controller is further configured to, when the voltage amplitude of the actual operation pulse voltage acquired by the parameter acquisition circuit is greater than a first preset voltage threshold, control the protection circuit 60 to disconnect the connection between the DC power supply 10 and the energy storage circuit 20 and release the electrical energy stored in the energy storage circuit 20. The specific implementation of the protection process will be described in subsequent content and is not described in detail herein for the time being.

[0138] In summary, compared with the foregoing embodiments, the pulse voltage generation circuit provided in this embodiment additionally includes a parameter acquisition circuit and a protection circuit. By acquiring the actual operation pulse voltage that is output, overvoltage protection for the switch unit and the pulse voltage generation circuit as a whole is implemented, which helps improve the safety and service life of each first controllable switch in the switch unit and the pulse voltage generation circuit as a whole.

[0139] In some embodiments, the present application further provides a semiconductor process equipment. As shown in FIG. 9, the semiconductor process equipment provided by the present

application includes a process chamber 140, a controller 70, and the pulse voltage generation circuit provided in any of the foregoing embodiments.

[0140] As described above, a wafer carrier 130 is disposed in the process chamber 140, and a bias electrode 40 is disposed in the wafer carrier 130. The output terminal of the pulse voltage generation circuit provided in any of the foregoing embodiments is connected to the bias electrode 40 to output an operation pulse voltage to the bias electrode 40. As shown in FIG. 9, to clearly illustrate the semiconductor process equipment provided in this embodiment, the pulse voltage generation circuit is shown in the form of a structural block diagram. For specific implementations of the respective subcircuits constituting the pulse voltage generation circuit in the embodiment shown in FIG. 9, reference may be made to the relevant content of the foregoing embodiments, and details are not repeated herein.

[0141] In some embodiments, the semiconductor process equipment provided in this embodiment further includes an RF power supply 90, an impedance matching circuit 100, an ion current detector 120, and an upper electrode disposed opposite to the wafer carrier 130. As described above, the semiconductor process equipment provided by the present application may be an ICP etching machine or a CCP etching machine. When the semiconductor process equipment is an ICP etching machine, the upper electrode is a coupling coil 110, and when the semiconductor process equipment is a CCP etching machine, the upper electrode is a gas inlet flow equalization plate. In view of this, in the embodiment shown in FIG. 9, the upper electrode is illustrated as the coupling coil 110.

[0142] Specifically, the RF power supply 90 is mainly configured to apply RF power to the upper electrode, thereby generating plasma that bombards the wafer.

[0143] The impedance matching circuit 100 is configured for impedance matching of a plasma generation loop, such that the power of the RF power supply 90 is maximally applied to the coupling coil 110 and the process chamber 140. In practical applications, the configuration of the impedance matching circuit 100 and the matching impedance value need to be set in conjunction with conditions such as the process chamber 140, the coupling coil 110, and the actual wiring of the overall circuit, and the present application likewise does not limit the specific implementation of the impedance matching circuit 100.

[0144] The coupling coil 110 is configured to apply the electrical energy output by the RF power supply 90 to the process chamber 140 by electromagnetic field coupling, thereby generating stable plasma in the process chamber. In practical applications, to achieve a better pulse voltage generation effect, the coupling coil 110 is generally disposed opposite to the bias electrode 40 in the process chamber 140.

[0145] In view of the above, the output terminal of the RF power supply 90 is connected to the impedance matching circuit 100, and the impedance matching circuit 100 is connected to the coupling coil 110. After the RF power supply 90 starts operating, plasma can be generated inside the process chamber 140 through the impedance matching circuit 100 and the coupling coil 110.

[0146] As shown in FIG. 9, a wafer carrier 130 is further disposed in the process chamber 140, and the wafer carrier 130 carries a wafer 150 to be processed. In practical applications, an electrostatic chuck having an insulating ceramic layer disposed therein may be selected as the wafer carrier 130. Certainly, other implementations that can carry the wafer 150 while enabling the wafer 150 to generate an induced voltage and thereby affect ion movement may also be selected, and details thereof are not described herein. The bias electrode 40 described in the foregoing embodiments is disposed inside the wafer carrier 130. After the operation pulse

voltage output by the pulse voltage generation circuit is output to the bias electrode 40, the insulating ceramic layer inside the wafer carrier 130 is located between the bias electrode 40 and the wafer 150, and a parallel-plate capacitive effect is produced between the bias electrode 40 and the wafer 150. The operation pulse voltage output by the pulse voltage generation circuit acts on the plasma inside the process chamber 140 by capacitive coupling, thereby implementing control of the plasma.

[0147] In a preferred embodiment, a circuit portion of the pulse voltage generation circuit configured to output the operation pulse voltage is disposed directly below the process chamber 140, thereby effectively shortening the connection line between the pulse voltage generation circuit and the bias electrode 40, greatly reducing the inductance of the connection line, reducing pulse waveform oscillations caused by the inductance, and helping mitigate the problem of an unsatisfactory unimodal IEDF control effect.

[0148] The parameter acquisition circuit 80 described in the foregoing embodiments is mainly configured to acquire an actual operation pulse voltage at a preset sampling point. As shown in FIG. 9, the preset sampling points are respectively the input terminal of the oscillation suppression circuit 50 (which may also be regarded as the output terminal of the switch unit 30), the output terminal of the oscillation suppression circuit 50, and the bias electrode 40. It should be noted that, in practical applications, one or more of the foregoing three preset sampling points may be used. The selection of a preset sampling point mainly depends on influencing conditions such as the difficulty of connecting the parameter acquisition circuit 80 to the preset sampling point, the accuracy of a sampling parameter, and the degree of matching between the sampling parameter and a control function. When a plurality of preset sampling points are used, the controller further needs to be configured to implement a screening mechanism for the sampling

parameters, i.e., how to determine a sampling parameter to be finally used from among a plurality of sampling parameters.

[0149] To enable the parameter acquisition circuit 80 to acquire parameters at a plurality of preset sampling points, in one embodiment, the parameter acquisition circuit 80 includes three acquisition modules, which are respectively an ion energy acquisition module, a first voltage acquisition module, and a second voltage acquisition module.

[0150] The ion energy acquisition module is connected to the back surface of the wafer 150 through a conductive lift pin and acquires, in real time, the operation pulse voltage induced on the surface of the wafer 150. It can be understood that the operation pulse voltage can generally be characterized by three parameters, i.e., a voltage amplitude, a pulse frequency, and a pulse width. In view of this, the ion energy acquisition module includes three main components: a voltage amplitude acquisition module, a pulse frequency acquisition module, and a pulse width acquisition module. The voltage amplitude acquisition module acquires a voltage peak value of the operation pulse voltage on the surface of the wafer 150, the pulse frequency acquisition module acquires the pulse frequency of the operation pulse voltage on the surface of the wafer 150, and the pulse width acquisition module acquires the pulse width of the operation pulse voltage on the surface of the wafer 150.

[0151] The first voltage acquisition module is configured to acquire the operation pulse voltage at the input terminal of the oscillation suppression circuit 50, and the second voltage acquisition module is configured to acquire the operation pulse voltage at the output terminal of the oscillation suppression circuit 50.

[0152] The respective constituent modules in the parameter acquisition circuit 80 send the obtained parameter information to the controller 70, and the controller 70 implements control of

the operating process of the pulse voltage generation circuit. The specific control process will be described in subsequent content and is not described in detail herein for the time being.

[0153] As for specific implementations of other constituent portions of the pulse voltage generation circuit shown in FIG. 9, such as the DC power supply 10, the protection circuit 60, the energy storage circuit 20, the switch unit 30, the oscillation suppression circuit 50, or the like, reference may be made to the relevant content in the foregoing embodiments, and details are not repeated herein.

[0154] In some embodiments, the pulse voltage generation circuit provided in this embodiment further includes an ion current detector 120. The ion current detector 120 can collect an ion current of ions that bombard the surface of the wafer 150 after being accelerated through the sheath field inside the process chamber 140.

[0155] As shown in FIG. 10, the ion current detector 120 includes a filter grid 1201, a first grid electrode 1202, a second grid electrode 1203, and a collection member 1204. The filter grid 1201 functions to allow ions and electrons of the plasma inside the process chamber 140 to enter the ion current detector 120, and in practical applications, the filter grid 1201 needs to be grounded. The first grid electrode 1202 has the same grid aperture as the filter grid 1201. During operation of the ion current detector 120, a negative voltage having a certain amplitude needs to be applied to the first grid electrode 1202 to prevent electrons from entering an ion collection space inside the ion current detector 120. The collection member 1204 is configured to attract ions into the collection space, thereby detecting an ion current. A negative voltage lower than a voltage applied to the collection member 1204 is applied to the second grid electrode 1203, thereby preventing secondary electrons generated by ions bombarding the collection member 1204 from

escaping and affecting measurement results. The collection member 1204 is made of a graphite material and collects an actual ion current of ions bombarding the wafer.

[0156] To feed the ion current acquired by the ion current detector 120 back to the controller 70, the parameter acquisition circuit 80 further includes an ion flux acquisition module. The module is connected through a wire to the bottom of the collection member 1204 of the ion current detector 120, converts the actual ion current into a voltage signal using a resistor and acquires the voltage signal, thereby determining an actual ion flux bombarding the wafer 150 and feeding the actual ion flux back to the controller 70. The controller 70 adjusts the output power of the RF power supply 90 according to the actual ion flux, ultimately achieving precise control of the ion flux.

[0157] In summary, compared with the foregoing embodiments, the pulse voltage generation circuit provided in this embodiment, on the basis of outputting an operation pulse voltage to implement precise control of ion energy, further includes a plasma generation loop and a ion current detector. The output power of a plasma generator is adjusted based on the actual ion flux detected by the ion current detector and fed back through the parameter acquisition circuit to adjust the ion flux, thereby implementing dual control of ion energy and ion flux, effectively improving the pulse voltage generation effect, and further improving the wafer processing level.

[0158] In the foregoing embodiments, the controller in the semiconductor process equipment mainly implements control of an operating process of the semiconductor process equipment. The controller includes at least one memory and at least one processor, and the processor is configured to execute the pulse voltage generation method provided in any of the embodiments of FIG. 11 to FIG. 14.

[0159] Referring to FIG. 11, one embodiment of the pulse voltage generation method provided by the present application includes the following operations:

[0160] At S100, in response to a control instruction, the DC power supply is controlled to output a DC voltage, and the first controllable switches in the switch unit are controlled to be sequentially turned on, such that the pulse voltage generation circuit outputs an operation pulse voltage for controlling ions.

[0161] In practical applications, the control instruction may originate from any device or apparatus capable of controlling operation of the pulse voltage generation circuit. For example, it may be the semiconductor process equipment to which the pulse voltage generation circuit belongs, or may be another host computer capable of communicating with the controller in the pulse voltage generation circuit. Alternatively, the controller in the pulse voltage generation circuit communicates with other modules in the semiconductor process equipment, and when it is determined that the pulse voltage generation circuit needs to operate, the control instruction is automatically generated by the controller itself. The present application does not limit a specific manner in which the pulse voltage generation circuit obtains the control instruction.

[0162] After obtaining the control instruction, the controller controls the DC power supply in the pulse voltage generation circuit to output a DC voltage and controls the switch unit to operate, such that the pulse voltage generation circuit outputs an operation pulse voltage.

[0163] In one embodiment, the control instruction includes a target voltage value. After receiving the control instruction, the controller can control the DC power supply to operate according to the target voltage value.

[0164] In another embodiment, the control instruction may include only enable information of the DC power supply, and the controller controls the DC power supply to operate based on the

enable information according to a preset initial voltage value of the controller itself or an initial voltage value calculated from other parameters.

[0165] In one embodiment, the control instruction may further include a target parameter for controlling operation of the switch unit, such as a voltage amplitude, a pulse frequency, a duty cycle, or the like of the drive pulse voltage. After obtaining the control instruction, the controller can control the switch unit to operate according to the target parameter.

[0166] In another embodiment, the control instruction may likewise include only enable information of the switch unit, and the controller controls the switch unit to operate based on the enable information according to preset control information of the controller itself.

[0167] It should be noted that, during the process of controlling the conduction states of the first controllable switches in the switch unit to output the operation pulse voltage, the control rules to be followed are likewise as follows: the first controllable switches are sequentially turned on, the conduction time periods of the first controllable switches do not overlap with each other, and the conduction time periods of two first controllable switches adjacent in the conduction sequence are separated by a preset duration. As for the specific process of outputting the operation pulse voltage based on the specific circuit topology of the pulse voltage generation circuit and the control rules, reference may be made to the relevant content in the foregoing embodiments, and details are not repeated herein.

[0168] With the pulse voltage generation method provided in this embodiment, the pulse frequency of the output operation pulse voltage is the sum of the conduction state switching frequencies of the first controllable switches. Therefore, providing a plurality of first controllable switches can effectively increase the pulse frequency of the operation pulse voltage. For the first controllable switches, when the pulse frequency of the operation pulse voltage is constant, the

pulse frequency is jointly shared by the first controllable switches, thereby effectively reducing the conduction state switching frequency of each first controllable switch and thus effectively reducing switching loss. Meanwhile, since the energy storage circuit can store electrical energy, the electrical energy released by the energy storage circuit within the preset duration is superimposed on the electrical energy output by the DC power supply, thereby effectively increasing the voltage amplitude of the operation pulse voltage. Therefore, the present application can increase the pulse frequency of the operation pulse voltage on the basis of satisfying switching loss requirements and voltage amplitude requirements, thereby mitigating the problem of an unsatisfactory unimodal IEDF control effect and satisfying actual process requirements.

[0169] Moreover, since the pulse frequency of the operation pulse voltage output by the pulse voltage generation circuit is sufficiently high, a good unimodal IEDF control effect can still be achieved without adding another current compensation circuit. Compared with the prior art, the pulse voltage generation method provided in this embodiment has simpler control logic and can reduce the logic overhead of the controller and the requirements for hardware performance of the controller.

[0170] In some embodiments, referring to FIG. 12, FIG. 12 is a flowchart of another pulse voltage generation method provided in an embodiment of the present application. On the basis of the foregoing embodiment, the pulse voltage generation method provided in this embodiment includes the following operations.

[0171] At S200, in response to a control instruction, the DC power supply is controlled to output a DC voltage, and a drive pulse voltage is respectively output to each first controllable switch according to preset drive pulse voltage parameters.

[0172] For optional implementations of the control instruction and optional implementations in which the controller controls the DC power supply to output a DC voltage in response to the control instruction, reference may be made to the relevant content in the foregoing embodiments, and details are not repeated herein.

[0173] In the pulse voltage generation method provided in this embodiment, a drive pulse voltage is used to control the conduction state of each first controllable switch in the switch unit, and the first controllable switches use drive pulse voltages having the same pulse waveform. In view of this, the controller respectively outputs a drive pulse voltage to each first controllable switch based on the preset drive pulse voltage parameters.

[0174] It should be noted that there are a plurality of parameters capable of characterizing the drive pulse voltage, such as a voltage amplitude, a pulse period, a pulse frequency, a duty cycle, a pulse width, or the like. A complete drive pulse voltage waveform can be defined by a combination of some of these parameters. In practical applications, specific drive pulse voltage parameters may be selected according to actual needs.

[0175] It should further be noted that, in a determined operation scenario, the waveform of the operation pulse voltage needed for processing a wafer can generally be predetermined. In some embodiments, as can be seen from the foregoing content, the waveform of the operation pulse voltage is directly affected by the DC voltage output by the DC power supply in the pulse voltage generation circuit, the arrangement of the first controllable switches in the switch unit, and the driving conditions. For a determined pulse voltage generation circuit, the range of the DC voltage output by the DC power supply and the arrangement of the first controllable switches in the switch unit are known. Therefore, an initial value of a parameter of the drive pulse voltage

and an initial value of the DC voltage of the DC power supply can be determined based on the foregoing information.

[0176] As described above, during the process of using the drive pulse voltages to control operation of the switch unit, the foregoing conduction control rules likewise need to be satisfied. Therefore, the phase differences between the drive pulse voltages corresponding to the first controllable switches need to be limited. A specific limiting manner may be implemented with reference to the relevant content in the foregoing embodiments, and details are not repeated herein.

[0177] At S210, an actual operation pulse voltage at a preset sampling point in the pulse voltage generation circuit is obtained.

[0178] For the specific selection of the preset sampling point, reference may be made to the foregoing content, and details are not repeated herein. The parameter acquisition circuit acquires the actual operation pulse voltage at the preset sampling point and feeds the obtained actual operation pulse voltage back to the controller.

[0179] It should be noted that, similar to the foregoing drive pulse voltage, the operation pulse voltage can likewise be characterized by parameters such as a voltage amplitude, a pulse period, a pulse frequency, a duty cycle, and a pulse width. Therefore, obtaining the actual operation pulse voltage as described in this operation actually refers to obtaining an actual value of a target parameter among the foregoing parameters. Certainly, the target parameter is selected on the premise that the waveform of the operation pulse voltage can be completely described. For example, the target parameter may include a voltage amplitude, a pulse frequency, and a pulse width.

[0180] At S220, actual ion energy is determined according to the actual operation pulse voltage.

[0181] For a specific implementation of calculating the actual ion energy according to the actual operation pulse voltage, reference may be made to related technologies, and details are not described herein.

[0182] At S230, the DC voltage output by the DC power supply and/or the conduction process of each first controllable switch is adjusted, such that the energy distribution of the actual ion energy is a unimodal distribution.

[0183] In practical applications, because loss and electromagnetic interference inevitably occur during transmission of the operation pulse voltage to the bias electrode, there is a certain deviation between the actual operation pulse voltage and the operation pulse voltage output by the pulse voltage generation circuit, thereby causing the energy distribution of the actual ion energy to deviate from a unimodal distribution and affecting the ion control effect.

[0184] Based on the foregoing formula (4), ion energy is affected by the voltage amplitude, pulse width, and pulse frequency of the operation pulse voltage. As can be seen from the pulse voltage generation circuit provided in the foregoing embodiments, these parameters are directly affected by the DC voltage output by the DC power supply and the conduction process of each first controllable switch in the switch unit. Therefore, the output operation pulse voltage can be adjusted by adjusting the DC voltage output by the DC power supply and/or the conduction process of each first controllable switch, thereby adjusting the actual ion energy such that the energy distribution of the actual ion energy is a unimodal distribution. As can be seen from the foregoing content, adjusting the first controllable switches in the switch unit can change a plurality of parameters such as the voltage amplification factor, the pulse frequency, and the pulse width. Moreover, adjusting the DC voltage of the DC power supply and the voltage amplification factor can both change the voltage amplitude of the operation pulse voltage.

[0185] It should be noted that, since both the DC power supply and the switch unit can affect the final output of the pulse voltage generation circuit, at least one of the DC power supply or the switch unit can be adjusted. Moreover, during an actual adjustment process, a plurality of adjustments are often needed to adjust the energy distribution of the actual ion energy to a unimodal distribution.

[0186] In summary, the pulse voltage generation method provided in this embodiment adjusts the operating process of the pulse voltage generation circuit according to the actual ion energy acting on the wafer during operation of the pulse voltage generation circuit, and adjusts the energy distribution of the actual ion energy to a unimodal distribution, thereby effectively improving the control precision of the ion energy and thereby helping improve wafer processing performance.

[0187] In some embodiments, referring to FIG. 13, FIG. 13 is a flowchart of still another pulse voltage generation method provided in an embodiment of the present application. The pulse voltage generation method provided in this embodiment includes the following operations.

[0188] At S300, an actual operation pulse voltage at a preset sampling point in the pulse voltage generation circuit is obtained.

[0189] In one embodiment, S300 may be implemented with reference to the relevant content of S210 in the embodiment shown in FIG. 12, and details are not repeated herein.

[0190] At S310, whether the voltage amplitude of the actual operation pulse voltage is greater than a first preset voltage threshold is determined. If yes, S320 is performed.

[0191] As can be seen from the operating process of the pulse voltage generation circuit provided in the foregoing embodiments, when all the first controllable switches in the switch unit are turned off, the pulse voltage generation circuit outputs a high level voltage. The high level

voltage is obtained by superimposing the electrical energy released by the energy storage circuit on the electrical energy output by the DC power supply and has a very high voltage amplitude. Moreover, the high level voltage is directly applied to the first controllable switches, increasing the risk that the first controllable switches are damaged due to overvoltage.

[0192] To improve the operational safety of the first controllable switches, the magnitude relationship between the voltage amplitude of the actual operation pulse voltage and the first preset voltage threshold needs to be determined. In practical applications, first controllable switches of different specifications correspond to different maximum withstand voltages. Therefore, the first preset voltage threshold may be set based on the maximum withstand voltage of the first controllable switch. It can be understood that the first preset voltage threshold should be less than or equal to the maximum withstand voltage of the first controllable switch. As for the specific value of the first preset voltage threshold, it needs to be set in conjunction with specific control requirements and protection requirements, and the present application does not limit this.

[0193] If the voltage amplitude of the actual operation pulse voltage is greater than the first preset voltage threshold, S320 continues to be performed. Conversely, if the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold, the pulse voltage generation circuit is controlled to continue operating, and operation of the protection circuit is not triggered.

[0194] At S320, the protection circuit is controlled to disconnect the connection between the DC power supply and the energy storage circuit and release the electrical energy stored in the energy storage circuit.

[0195] When the voltage amplitude of the actual operation pulse voltage is greater than the first preset voltage threshold, the protection circuit is controlled to disconnect the connection between the DC power supply and the energy storage circuit, thereby terminating continued provision of electrical energy by the DC power supply to a subsequent-stage circuit, while releasing the electrical energy stored in the energy storage circuit.

[0196] Taking the pulse voltage generation circuit provided in the embodiment shown in FIG. 8 as an example, when the voltage amplitude of the actual operation pulse voltage is greater than the first preset voltage threshold, the controller first controls the second controllable switch Sp to be turned off to cut off the output of the DC power supply. Meanwhile, the controller controls the third controllable switch Sq to be turned on, and the electrical energy stored in the energy storage inductor L1 is rapidly released through the first resistor R1, thereby preventing damage to the first controllable switches in the switch unit.

[0197] It can be understood that, when the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold, the controller controls the second controllable switch Sp to be turned on and the third controllable switch Sq to be turned off, and the DC power supply continues to output a DC voltage, which is converted by the switch unit to output the operation pulse voltage.

[0198] In another embodiment, the controller may further set a second preset voltage threshold, where the second preset voltage threshold is less than the first preset voltage threshold. When the voltage amplitude of the actual operation pulse voltage is greater than the second preset voltage threshold and less than the first preset voltage threshold, it indicates that the voltage amplitude of the actual operation pulse voltage has reached an early-warning stage but has not yet significantly affected the safety of the first controllable switch. The controller may reduce the

DC voltage output by the DC power supply to ensure the safety of the first controllable switch without operation of the protection circuit, i.e., without affecting the overall operation of the circuit. Through cooperation between the first preset voltage threshold and the second preset voltage threshold, stepped protection of the first controllable switch and the pulse voltage generation circuit as a whole can be implemented, thereby avoiding frequent operation of the protection circuit while ensuring circuit safety, and further improving the stability and reliability of circuit operation.

[0199] At S330, the DC voltage output by the DC power supply and/or the conduction process of each first controllable switch is adjusted until the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold.

[0200] As described above, the voltage amplitude of the operation pulse voltage output by the pulse voltage generation circuit is mainly affected by two parameters: one is the DC voltage output by the DC power supply, and the other is the voltage amplification factor of the switch unit. In view of this, after the protection circuit is controlled to perform the protection action described in S320, the DC voltage output by the DC power supply may be reduced, or the voltage amplification factor may be reduced by adjusting the conduction process of each first controllable switch. Certainly, the foregoing two adjustment measures may be taken simultaneously until the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold.

[0201] In practical applications, after one adjustment is performed, the voltage amplitude of the operation pulse voltage may be acquired again, and the foregoing operations may be repeatedly performed, such that the voltage amplitude of the actual operation pulse voltage is made less than or equal to the first preset voltage threshold through a plurality of adjustments.

[0202] At S340, the protection circuit is controlled to connect the DC power supply and the energy storage circuit.

[0203] When the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold, it indicates that the pulse voltage generation circuit can operate normally, and the controller controls the protection circuit to connect the DC power supply and the energy storage circuit. Taking the pulse voltage generation circuit provided in the embodiment shown in FIG. 8 as an example, the controller controls the third controllable switch Sq to be turned off and, correspondingly, controls the second controllable switch Sp to be turned on, and the circuit resumes normal operation.

[0204] In summary, the pulse voltage generation method provided in this embodiment monitors the voltage amplitude of the actual operation pulse voltage, and controls operation and recovery of the protection circuit according to the magnitude relationship between the voltage amplitude of the actual operation pulse voltage and the preset voltage threshold, thereby effectively improving the safety of each first controllable switch in the switch unit and the pulse voltage generation circuit as a whole, and further improving the stability and reliability of operation of the pulse voltage generation circuit.

[0205] In some embodiments, on the basis of the pulse voltage generation method provided in any of the foregoing embodiments, the following operations shown in FIG. 14 may further be included.

[0206] At S400, an actual ion flux bombarding the wafer is obtained.

[0207] As described above, the pulse voltage generation circuit is provided with an ion current detector and a parameter acquisition circuit. The ion current detector acquires an actual ion current of ions that bombard the wafer surface after being accelerated through the sheath field

inside the process chamber, and outputs the obtained actual ion current to the parameter acquisition circuit.

[0208] An ion flux acquisition module is disposed in the parameter acquisition circuit. The module is connected through a wire to the bottom of the collection member of the ion current detector, converts the actual ion current into a voltage signal using a resistor and acquires the voltage signal, thereby determining the actual ion flux bombarding the wafer. The controller is connected to the parameter acquisition circuit and obtains the actual ion flux fed back by the parameter acquisition circuit.

[0209] At S410, the output power of the plasma generator is adjusted until a deviation between the actual ion flux and a target ion flux is within a preset flux deviation range.

[0210] The target ion flux is an ion flux expected to be needed for processing the wafer and can generally be determined before processing the wafer according to the specifications of the wafer to be processed and a specific processing process. Certainly, the target ion flux may also be determined according to other information or manners, and the present application does not limit this. In an actual application process, after the target ion flux is determined, the target ion flux may be stored in the controller.

[0211] In some embodiments, considering the difficulty of actual control and the requirements for control precision, the present application provides a preset flux deviation range, and the deviation between the actual ion flux and the target ion flux is limited by the preset flux deviation range. It can be understood that, when the deviation between the actual ion flux and the target ion flux is within the preset flux deviation range, the current actual ion flux is considered to satisfy the process requirements. Conversely, when the deviation between the actual ion flux and the target ion flux is not within the preset flux deviation range, the current actual ion flux is

considered unable to satisfy the process requirements. In practical applications, the preset flux deviation range may be set according to the performance of the pulse voltage generation circuit and specific process requirements, and the present application does not limit the specific setting of the preset flux deviation range.

[0212] In view of the above, when the deviation between the actual ion flux and the target ion flux is not within the preset flux deviation range, the output power of the plasma generator is adjusted until the deviation between the actual ion flux and the target ion flux is within the preset flux deviation range.

[0213] In summary, compared with the pulse voltage generation methods provided in the foregoing embodiments, the pulse voltage generation method provided in this embodiment, on the basis of outputting an operation pulse voltage to implement precise control of ion energy, adjusts the output power of the plasma generator based on the actual ion flux detected by the ion current detector and fed back through the parameter acquisition circuit, and adjusts the ion flux, thereby implementing dual control of ion energy and ion flux, effectively improving the pulse voltage generation effect, and further improving the wafer processing level.

[0214] In some embodiments, this embodiment further provides a computer-readable storage medium, such as a floppy disk, an optical disc, a hard disk, a flash memory, a USB flash drive, an SD (Secure Digital Memory Card, secure digital card) card, an MMC (Multimedia Card, multimedia card) card, or the like. One or more instructions for implementing the foregoing operations are stored in the computer-readable storage medium. When the one or more instructions are executed by one or more processors, the processor is caused to execute the pulse voltage generation method described above. For relevant specific implementations, reference may be made to the foregoing description, and details are not redundantly described herein.

[0215] In addition to the foregoing method and device, an embodiment of the present application may further be a computer program product, which includes computer program instructions. When the computer program instructions are run by a processor, the processor is caused to perform the operations in the pulse voltage generation method according to various embodiments of the present application described above in this specification.

[0216] Program code for performing the operations of the embodiments of the present application may be written in any combination of one or more programming languages. The programming languages include object-oriented programming languages, such as Java, C++, or the like, and further include conventional procedural programming languages, such as the "C" language or similar programming languages. The program code may be executed entirely on a user computing device, partially on a user device, as an independent software package, partially on a user computing device and partially on a remote computing device, or entirely on a remote computing device or server.

[0217] A person skilled in the art can understand that the content disclosed in the present application may have various variations and improvements. For example, the various devices or components described above may be implemented by hardware, or may be implemented by software, firmware, or a combination of some or all of the three.

[0218] Moreover, although the present application makes various references to certain units in a system according to the embodiments of the present application, any number of different units may be used and run on a client and/or server. The units are merely illustrative, and different aspects of the system and method may use different units.

[0219] Flowcharts are used in the present application to illustrate operations of methods according to the embodiments of the present application. It should be understood that preceding

or subsequent operations do not necessarily need to be performed precisely in sequence. Instead, various operations may be processed in reverse order or simultaneously. Meanwhile, other operations may also be added to these processes.

[0220] A person of ordinary skill in the art can understand that all or some of the operations in the foregoing methods may be completed by instructing relevant hardware through a computer program, and the program may be stored in a computer-readable storage medium, such as a read-only memory. Optionally, all or some of the operations in the foregoing embodiments may also be implemented using one or more integrated circuits. Correspondingly, each module/unit in the foregoing embodiments may be implemented in the form of hardware or in the form of a software functional module. The present application is not limited to any particular form of combination of hardware and software.

[0221] Unless otherwise defined, all terms used herein have the same meanings as commonly understood by a person of ordinary skill in the art to which the present application pertains. It should also be understood that terms such as those defined in commonly used dictionaries should be interpreted as having meanings consistent with their meanings in the context of the related art, and should not be interpreted in idealized or excessively formal senses unless expressly so defined herein.

[0222] The foregoing is a description of the present application and should not be considered a limitation thereof. Although several example embodiments of the present application have been described, a person skilled in the art will readily understand that many modifications may be made to the example embodiments without departing from the novel teachings and advantages of the present application. Therefore, all such modifications are intended to be included within the scope of the present application as defined by the claims. It should be understood that the

foregoing is a description of the present application and should not be considered limited to the particular disclosed embodiments, and modifications to the disclosed embodiments and other embodiments are intended to be included within the scope of the appended claims. The present application is defined by the claims and equivalents thereof.

CLAIMS

WHAT IS CLAIMED IS:

1. A pulse voltage generation circuit for a semiconductor process equipment, comprising: an energy storage circuit and a switch unit, the switch unit comprising a plurality of first controllable switches, wherein,

an input terminal of the energy storage circuit is configured to be connected to a DC power supply, an output terminal of the energy storage circuit is respectively connected to an input terminal of each of the first controllable switches, and an output terminal of each of the first controllable switches is configured to be grounded;

a connection point between the energy storage circuit and each of the first controllable switches is configured to output an operation pulse voltage;

a control terminal of each of the first controllable switches is configured to be connected to a controller;

the first controllable switches are configured to be sequentially turned on under control of the controller, to output the operation pulse voltage;

wherein, conduction time periods of the first controllable switches do not overlap with each other, and conduction time periods of two of the first controllable switches adjacent in a conduction sequence are separated by a preset duration;

the energy storage circuit is configured to store electrical energy when any one of the first controllable switches is turned on, and release the electrical energy within the preset duration.

2. The pulse voltage generation circuit according to claim 1, wherein the controller is configured to:

output a drive pulse voltage to each of the first controllable switches according to preset drive pulse voltage parameters, wherein the drive pulse voltage is configured to control a conduction state of the first controllable switch.

3. The pulse voltage generation circuit according to claim 1, further comprising: an oscillation suppression circuit, wherein,

an input terminal of the oscillation suppression circuit is connected to a connection point between the energy storage circuit and each of the first controllable switches, and an output terminal of the oscillation suppression circuit is configured to output the operation pulse voltage;

the oscillation suppression circuit is configured to suppress voltage fluctuations of the operation pulse voltage.

4. The pulse voltage generation circuit according to claim 3, further comprising: a parameter acquisition circuit, wherein,

the parameter acquisition circuit is configured to acquire an actual operation pulse voltage at a preset sampling point, the preset sampling point comprising at least one of the input terminal of the oscillation suppression circuit, the output terminal of the oscillation suppression circuit, or a bias electrode, wherein the bias electrode is located in a wafer carrier of the semiconductor process equipment;

the controller is configured to: adjust a DC voltage output by the DC power supply and/or a conduction process of each of the first controllable switches according to the actual operation pulse voltage.

5. The pulse voltage generation circuit according to claim 4, further comprising: a protection circuit, wherein,

a first connection terminal of the protection circuit is configured to be connected to an output terminal of the DC power supply, and a second connection terminal of the protection circuit is connected to an input terminal of the energy storage circuit;

the controller is connected to a control terminal of the protection circuit;

the controller is configured to: when a voltage amplitude of the actual operation pulse voltage is greater than a first preset voltage threshold, control the protection circuit to disconnect a connection between the DC power supply and the energy storage circuit and release electrical energy stored in the energy storage circuit.

6. The pulse voltage generation circuit according to claim 5, wherein the protection circuit comprises: a second controllable switch, a third controllable switch, and a first resistor, wherein,

an input terminal of the second controllable switch serves as the first connection terminal of the protection circuit;

a connection point between an output terminal of the second controllable switch and an input terminal of the third controllable switch serves as the second connection terminal of the protection circuit;

an output terminal of the third controllable switch is connected to one end of the first resistor, and the other end of the first resistor is configured to be grounded;

control terminals of the second controllable switch and the third controllable switch are respectively connected to the controller.

7. The pulse voltage generation circuit according to any one of claims 1 to 6, wherein the energy storage circuit comprises: an energy storage inductor and a voltage stabilization capacitor, wherein,

a first end of the energy storage inductor is connected to a first end of the voltage stabilization capacitor, and a second end of the energy storage inductor serves as the output terminal of the energy storage circuit;

a second end of the voltage stabilization capacitor is configured to be grounded;

a connection point between the energy storage inductor and the voltage stabilization capacitor serves as the input terminal of the energy storage circuit.

8. A semiconductor process equipment, comprising: a process chamber, a controller, and the pulse voltage generation circuit according to any one of claims 1 to 7, wherein,

a wafer carrier is disposed in the process chamber, and a bias electrode is disposed in the wafer carrier;

the controller is electrically connected to a control terminal of each first controllable switch of the pulse voltage generation circuit;

an output terminal of the pulse voltage generation circuit is connected to the bias electrode;

the controller is configured to control the pulse voltage generation circuit to output an operation pulse voltage to the bias electrode, to control an ion energy distribution.

9. The semiconductor process equipment according to claim 8, further comprising: an RF coil, a matcher, and an RF power supply, wherein,

the RF power supply is configured to apply RF power to the RF coil through the matcher, to excite plasma in the process chamber;

the controller is further electrically connected to the RF power supply, to control output power of the RF power supply.

10. The semiconductor process equipment according to claim 9, further comprising: an ion current detector, wherein,

the ion current detector is configured to acquire an actual ion current of ions bombarding a wafer placed on the wafer carrier, the actual ion current being configured to characterize an actual ion flux;

the controller is further configured to adjust RF power of the RF power supply until a deviation between the actual ion flux and a target ion flux is within a preset flux deviation range.

11. The semiconductor process equipment according to any one of claims 8 to 10, wherein the controller is further configured to perform the following operations:

obtain an actual operation pulse voltage at a preset sampling point in the pulse voltage generation circuit;

determine actual ion energy according to the actual operation pulse voltage;

adjust a DC voltage output by a DC power supply connected to the pulse voltage generation circuit and/or a conduction process of each first controllable switch in the pulse voltage generation circuit, such that an energy distribution of the actual ion energy is a unimodal distribution.

12. The semiconductor process equipment according to claim 11, wherein the pulse voltage generation circuit comprises a protection circuit and an energy storage circuit, and the controller is further configured to perform the following operations:

if a voltage amplitude of the actual operation pulse voltage is greater than a first preset voltage threshold, control the protection circuit to disconnect a connection between the DC power supply and the energy storage circuit, and release electrical energy stored in the energy storage circuit;

adjust the DC voltage output by the DC power supply and/or a conduction process of each of the first controllable switches until the voltage amplitude of the actual operation pulse voltage is less than or equal to the first preset voltage threshold;

control the protection circuit to connect the DC power supply and the energy storage circuit.