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METHOD OF VACUUM PACKAGING A SEMICONDUCTOR DEVICE ASSEMBLY

FIELD OF THE INVENTION

The present invention relates generally to methods of electronic packaging technology, and specifically to a vacuum type of electronic packaging technology used with air gap interconnect semiconductor chips.

BACKGROUND OF THE INVENTION

Modern integrated circuit semiconductor devices are complex three-dimensional structures with metallized conductor lines, such as interconnects, separated or insulated by interlayer dielectrics. Inorganic materials, such as silicon dioxides (SiO_2) and silicon nitride (Si_3N_4), are conventionally used as these interlayer dielectrics.

Recently, the photo-definable derivatives of certain polymeric materials, such as polyimides, silicone-polyimides, and benzocyclobutenes, have become widely used as interlayer dielectrics because they tend to have lower dielectric constants (k) compared to inorganic interlayer dielectrics. A lower-k interlayer dielectric reduces the signal propagation delays and enhances the system performance. For example silicon dioxide has a dielectric constant of about 4, while Teflon® is a material that has one of the lower dielectric constants, i.e. about 2.0 (Air has a dielectric constant of 1). However Teflon® has certain characteristics and process issues that must be addressed before it can be widely used.

The major functions of electronic packaging are to: a) support and protect the chip from hostile environments; b) distribute the signals onto and off of the silicon chip; c) provide a path for the electrical current that powers the circuits on the chip; and d) remove the heat generated by the circuits.

Back end-of-line (BEOL) resistance capacitance (RC) is becoming increasingly important in ultra large-scale integration (ULSI) where an integrated circuit (IC) contains over 10 million semiconductor devices, and thus where the design rule approaches 0.25 μm and smaller.

U.S. Patent No. 5,866,442 to Brand et al. describes a semiconductor device assembly with a semiconductor device spaced apart from a substrate to define a gap to be filled by a fill material. The substrate has thermal vias formed therein and after the semiconductor device is connected to the substrate and the fill material is positioned about the gap to form a seal, a vacuum is drawn through the thermal vias and a pressure is applied to the fill material to urge the fill material into the interior of the gap.

U.S. Patent No. 5,766,987 to Mitchell et al. describes methods and equipment whereby microelectronic assemblies such as semiconductor chip assemblies are encapsulated. Covering layers not only protect both the terminals carried by a dielectric layer and the bottom surface of the semiconductor chips in each assembly, but also confine a liquid encapsulant and prevents contamination of the terminals and the chip bottom surfaces. The liquid encapsulant and the assemblies are placed into a tilting fixture, the fixture is closed and evacuated, and the encapsulant is them poured onto the assemblies while maintaining the fixture under vacuum. The fixture is then pressurized during cure of the encapsulant.

U.S. Patent No. 5,401,687 to Cole et al. describes a method for preserving an air bridge structure on an integrated circuit chip used in an overlay process. A patternable protective layer is applied for mechanical strength to prevent deformation during subsequent processing. A polymeric film layer is applied over the chip and protective layer and interconnections are fabricated through the polymeric film layer. The polymeric film layer is removed from the area over the air bridge structure and the protective layer is then removed leaving the resultant structure with an undamaged air bridge free of residue.

U.S. Patent No. 5,798,557 to Salatino et al. and U.S. Patent No. 5,915,168 to Salatino et al. (a divisional of the Salatino 5,798,557 Patent), describe a packaged integrated circuit (IC) and method of making same, respectively, where the IC is a wafer level hermetically packaged IC that has a protective cover wafer bonded to a semiconductor device substrate wafer. The substrate wafer may contain a cavity. The cover wafer seals integrated circuits and other devices such as air bridge structures, resonant beams, surface acoustic wave (SAW) devices, trimmable resistors and micromachines. Some devices are formed on the surface of cavities formed in the protective cover wafer. Dies are separated to complete the process.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a semiconductor chip device package having a vacuum within interconnect voids in the semiconductor chip device to reduce the interconnective RC delay and prevent metal corrosion.

Another object of the present invention is to provide a low cost packaging technology which changes the dielectric k-value to reduce the interconnective RC delay and prevent metal corrosion.

Yet another object of the present invention is to provide a method of forming a packaged semiconductor assembly by drawing a vacuum on an entire air gap semiconductor device to form a vacuum within the voids separating the interconnects.

A further object of the present invention is to provide a semiconductor chip device package having a vacuum within interconnect voids in the semiconductor chip device to lower the interlevel dielectric constant to reduce the signal propagation delays and enhance the system performance.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a semiconductor chip device package is comprised of a semiconductor substrate having semiconductor devices formed on the semiconductor substrate. At least one dielectric layer is over the semiconductor substrate. At least one layer of interconnects is over the semiconductor devices and within the at least one respective dielectric layer with at least a portion of the interconnects being separated by voids having a vacuum or air therein. A passivation layer is over the uppermost of the at least one layer of interconnects. Wherein the semiconductor chip device is vacuum sealed within a semiconductor chip device package.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the method of forming a packaged semiconductor assembly according to the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Fig. 1 schematically illustrates in cross-sectional representation a preferred embodiment of the present invention.

Fig. 2 schematically illustrates in cross-sectional representation a sample air gap structure of a semiconductor device, having dual damascene interconnects, used with the method of the present invention.

Fig. 3 schematically illustrates in cross-sectional representation a sample air gap structure of a semiconductor device, having interconnects with an upper metal line and a lower metal plug, used with the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Accordingly as shown in Fig. 1, semiconductor chip device 10, 10' is shown within, for example, a first level, electronic package 20 made in accordance with an embodiment of the present invention. Electronic package 20 may be one of several types of electronic packages as will be noted hereafter. Unless otherwise specified, all structures, layers, etc. may be formed or accomplished by conventional methods known in the prior art.

Fig. 2 illustrates a semiconductor chip device 10 of the present invention having dual damascene interconnects 32.

Fig. 3 illustrates a semiconductor chip device 10' of the present invention having interconnects 32' with an upper metal line 34' and a lower metal plug 36'.

Either semiconductor chip device 10, 10' structure may be used in the present invention as well as any other semiconductor chip device utilizing air gap technology.

As shown in Figs. 2 and 3, regardless of which semiconductor chip device 10, 10' of Figs. 2 and 3, respectively, is selected, the following description is essentially common to each semiconductor chip device 10, 10' so used.

Each semiconductor chip device 10, 10' has starting semiconductor structure 30, 30' which is understood to possibly include a semiconductor wafer or substrate with exposed active and passive devices on the upper surface of the wafer. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

A first dielectric layer (not shown) is formed over semiconductor structure 30, 30'. Either a first dual damascene interconnect 32 layer 40 of Fig. 2, or a first interconnect 32' layer 40' comprising a horizontal metal line 34' over a vertical metal plug 36' of Fig. 3, is formed within the first dielectric layer by photoresist masking/patterning and etching steps as is known in the prior art. Interconnects 32, 32' contact the exposed active and/or passive devices on the upper surface of the wafer.

As desired a second dielectric layer (not shown) is formed over first interconnect layer 40, 40' and the first dielectric layer. Again, another layer of interconnects 32 or 32' is formed, this time over the first level of interconnects.

A second dual damascene interconnect layer 50 is formed over first dual damascene interconnect layer 40 in forming the semiconductor chip device 10 of Fig. 2. A second interconnect layer 50' comprising a horizontal metal line 34' over

a vertical metal plug 36′ is formed over first interconnect layer 40′ in forming the semiconductor chip device 10′ of Fig. 3. Of course it is possible to combine dual damascene interconnects with interconnects having a horizontal metal line over a vertical metal plug, or visa versa.

Additional layers of dielectric layers and interconnect layers may be formed as desired. Only two levels of interconnects 40, 50; 40′, 50′ are illustrated herein. Dielectric layers may be comprised of low-k materials such as silicon oxide (SiO_2), for example, and interconnect layers 40, 40′; 50, 50′ may be comprised of tungsten (W), for example. Other materials may be used as is known in the prior art.

After the final dielectric and interconnect layer is formed, at least a portion of the dielectric material separating interconnect layers 40, 40′; 50, 50′ (for example in a two interconnect layer semiconductor chip device as illustrated in Figs. 2 and 3) is etched to form air filled voids 60, 60′ between interconnect layers 40, 40′; 50, 50′ at least in some portions of the semiconductor chip device 10, 10′.

Passivation layer 70, 70′ is then formed over the structure and may comprise silicon nitride (Si_3N_4), for example. Passivation layer 70, 70′ further has openings 72, 72′ therein communicating with at least some of voids 60, 60′. Voids

60, 60′ contain the ambient atmosphere such as air. This completes formation of semiconductor chip device 10, 10′.

Semiconductor chip device 10, 10′ is then packaged within, for example, a first level electronic package (vacuum type packaging) 20. Any type of packaging currently used in the industry may be used as long as the packaging can maintain the vacuum. For example, the following vacuum type packaging may be used ceramic, rubber seal, hermetic seal and metal cap.

As shown in Fig. 1, semiconductor chip device 10, 10′ is affixed to a support structure, such as chip pad or lead frame 80. Chip pad 80 may be attached to lower portion 82 of outer package structure 84, for example, by legs 86 or other such structure.

Semiconductor chip device 10, 10′ may be electrically connected to other devices external to outer package structure 84 by affixing wire bonds 88, to the bonding pads (not shown) of semiconductor chip device 10, 10′ (not shown) by solder balls 90. The other end of wire bonds 88 are affixed to lead frames 92 which extend from electronic package 20.

Upper portion 94 of outer package structure 84 is affixed to lower portion 82 of outer package structure 84. Upper portion 94 of outer package

structure 84 may be formed from thermoplastic polymers, thermosetting polymers or elastomers, such as, for example, plastic, mold resin, silicones, epoxies, polyurethanes, polyimides, silicone-polyimides, parylenes, Teflon®, ceramic metal, and composite polymers. Outer package 84 may be any of the materials used currently in the market as long as it can keep the vacuum.

Outer package structure 84 has one or more openings at 96, for example, and a source of vacuum is applied through openings 96. For example, outer package structure 84 may be placed within a chamber (not shown) upon which a vacuum may be drawn by a pump, for example (not shown).

As a vacuum is formed within outer package structure 84, the air, or ambient atmosphere, is preferably drawn from voids 60, 60' through openings 72, 72' in passivation layer 70, 70' as shown at 98 (Also see Figs. 2 and 3). The air, or ambient atmosphere is further drawn from outer package structure 84 through outer package structure openings 96 as shown at 100 to create a vacuum within voids 60, 60' and within outer package structure 84 from about 10^{-6} Torr to 10^{-10} Torr, and more preferably from about 10^{-7} Torr to 10^{-8} Torr.

Openings 72, 72' may be sealed allowing air filled voids 60, 60' to remain within semiconductor chip device 10, 10' although passivation layer 70, 70' preferably has openings 72, 72', respectively, permitting formation of a vacuum

within voids 60, 60′ when the vacuum is formed within outer package structure 84 as described above.

Outer package structure openings 96 are sealed while maintaining the vacuum within voids 60, 60′ and within sealed outer package structure 84. This completes the formation of electronic package 20 of the present invention. Electronic package 20 may be hermetically sealed.

For semiconductor chip device packages 20 that are low-pin-count integrated circuit devices having a pin count less than about 300, the semiconductor chip device package may be a plastic quad flat pack (PQFP), Swiss outline package (SOP), Swiss outline J-leaded (SOJ), small outline integrated circuit (SOIC), plastic leaded chip carrier (PLCC), thin quad flat pack (TQFP), thin small outline package (TSOP), direct chip attach on printed circuit board (DCA), or a chip scale package (CSP), for example.

For semiconductor chip device packages 20 that are mid-pin-count integrated circuit devices having a pin count from about 250 to 600 such as main memory and cache memory, the semiconductor chip device package may be a tape carrier package (TCP), plastic pin grid array (PPGA), ceramic pin grid array (CPGA), or a plastic ball grid array (PBGA), for example.

For higher pin count semiconductor chip device packages 20 having a pin count greater than about 500, such as application specific integrated circuits (ASIC), the semiconductor chip device package may be a ceramic ball grid array (CBGA), tape ball grid array (TBGA), or metal ball grid array (MBGA), for example.

For very high pin count semiconductor chip device packages 20 having a pin count of at least about 1000, such as performance integrated circuit devices, the semiconductor chip device package may be an area-array solder-bumped flip-chip technology package.

Whatever package type is used, there are several advantages to having a vacuum within voids 60, 60′ (and within outer package structure 84).

One such advantage is that since a vacuum is formed with voids 60, 60′ there is less likelihood of contamination of the underlying semiconductor devices in semiconductor structure 30, 30′ connected to interconnects 32, 32′. This is because there is not any dielectric material separating interconnects 32, 32′ which may have contaminants, and there is minimal air, or ambient atmosphere within voids 60, 60′ which may also have contaminants

Another advantage is that the vacuum within voids 60, 60' and within outer package structure 84 provides for a more efficient and greater dissipation of heat from the semiconductor chip device and from outer package structure 84

Yet another advantage is that the vacuum within voids 60, 60' reduces the interlayer dielectric constant (k) to 1, reducing the signal propagation delays and enhancing the system performance.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.

CLAIMS

We claim:

1. A semiconductor chip device package comprised of:



a semiconductor substrate;

semiconductor devices formed on said semiconductor substrate;

at least one dielectric layer over said semiconductor substrate;

at least one layer of interconnects over said semiconductor devices and within said at least one respective dielectric layer; at least a portion of said interconnects being separated by voids; said voids having a vacuum or air therein; and

a passivation layer over the uppermost of said at least one layer of interconnects;

wherein said semiconductor chip device is vacuum sealed within a semiconductor chip device package.

2. The device of claim 1, wherein said semiconductor chip device package is a low-pin-count integrated circuit device having a pin count less than about 200, and said package is selected from the group comprising: plastic quad flat pack (PQFP); Swiss outline package (SOP); Swiss outline J-leaded (SOJ); small outline integrated circuit (SOIC); plastic leaded chip carrier (PLCC); thin quad flat pack (TQFP); thin

small outline package (TSOP); direct chip attach on printed circuit board (DCA); and chip scale package (CSP).



3. The device of claim 1, wherein said semiconductor chip device package is a mid-pin-count integrated circuit device having a pin count from about 250 to 600 such as main memory and cache memory, and said package is selected from the group comprising: tape carrier package (TCP); plastic pin grid array (PPGA); ceramic pin grid array (CPGA); and plastic ball grid array (PBGA).

4. The device of claim 1, wherein said semiconductor chip device package is a higher-pin-count integrated circuit device having a pin count greater than about 500 such as application specific integrated circuits (ASIC), and said package is selected from the group comprising: ceramic ball grid array (CBGA); tape ball grid array (TBGA); and metal ball grid array (MBGA).

5. The device of claim 1, wherein said semiconductor chip device package is a very-high-pin-count integrated circuit device having a pin count of at least about 1000 such as performance integrated circuit devices, and said package is an area-array solder-bumped flip-chip technology package.

6. The device of claim 1, wherein said passivation layer has openings therein exposing said voids.

7. The device of claim 1, wherein said interconnects are dual damascene interconnects.



8. The device of claim 1, wherein said voids having a vacuum .

9. A semiconductor chip device package comprised of:

a semiconductor substrate;

semiconductor devices formed on said semiconductor substrate;

at least one dielectric layer over said semiconductor substrate;

at least one layer of interconnects over said semiconductor devices and within said at least one respective dielectric layer; at least a portion of said interconnects being separated by voids; said voids having a vacuum or air therein; and

a passivation layer over the uppermost of said at least one layer of interconnects;

wherein said semiconductor chip device is vacuum sealed within a package and is electrically connected to lead frames extending from said package to form a semiconductor chip device package.

10. The device of claim 9, wherein said semiconductor chip device package is a low-pin-count integrated circuit device having a pin count less than about 200, and

said package is selected from the group comprising: plastic quad flat pack (PQFP); Swiss outline package (SOP); Swiss outline J-leaded (SOJ); small outline integrated circuit (SOIC); plastic leaded chip carrier (PLCC); thin quad flat pack (TQFP); thin small outline package (TSOP); direct chip attach on printed circuit board (DCA); and chip scale package (CSP).



11. The device of claim 9, wherein said semiconductor chip device package is a mid-pin-count integrated circuit device having a pin count from about 250 to 600 such as main memory and cache memory, and said package is selected from the group comprising: tape carrier package (TCP); plastic pin grid array (PPGA); ceramic pin grid array (CPGA); and plastic ball grid array (PBGA).

12. The device of claim 9, wherein said semiconductor chip device package is a higher-pin-count integrated circuit device having a pin count greater than about 500 such as application specific integrated circuits (ASIC), and said package is selected from the group comprising: ceramic ball grid array (CBGA); tape ball grid array (TBGA); and metal ball grid array (MBGA).

13. The device of claim 9, wherein said semiconductor chip device package is a very-high-pin-count integrated circuit device having a pin count of at least about 1000 such as performance integrated circuit devices, and said package is an area-array solder-bumped flip-chip technology package.

14. The device of claim 9, wherein said passivation layer has openings therein exposing said voids.



15. The device of claim 9, wherein said interconnects are dual damascene interconnects.

16. The device of claim 9, wherein said voids having a vacuum.

17. A method of fabricating a packaged semiconductor chip device, comprising the steps of:

providing a semiconductor substrate;

forming semiconductor devices on said semiconductor substrate;

forming a dielectric layer over said semiconductor substrate;

forming at least one layer of interconnects over said semiconductor devices and within said dielectric layer so that at least a portion of said interconnects are separated by voids;

forming a passivation layer over the uppermost of said at least one layer of interconnects to form a semiconductor chip;

affixing said semiconductor chip to a support structure within an enclosed package frame having gases therein;

withdrawing said gases from said enclosed package frame creating a vacuum within said voids of said chip interconnects; and

sealing said enclosed package frame to create a semiconductor chip device package while maintaining said vacuum within said voids;

wherein said semiconductor chip is vacuum sealed within said semiconductor chip device package and is electrically connected to lead frames extending from said semiconductor chip device package.



18. The method of claim 17, wherein said semiconductor chip device package is a low-pin-count integrated circuit device having a pin count less than about 200, and said package is selected from the group comprising: plastic quad flat pack (PQFP); Swiss outline package (SOP); Swiss outline J-leaded (SOJ); small outline integrated circuit (SOIC); plastic leaded chip carrier (PLCC); thin quad flat pack (TQFP); thin small outline package (TSOP); direct chip attach on printed circuit board (DCA); and chip scale package (CSP).

19. The method of claim 17, wherein said semiconductor chip device package is a mid-pin-count integrated circuit device having a pin count from about 250 to 600 such as main memory and cache memory, and said package is selected from the group comprising: tape carrier package (TCP); plastic pin grid array (PPGA); ceramic pin grid array (CPGA); and plastic ball grid array (PBGA).

20. The method of claim 17, wherein said semiconductor chip device package is a higher-pin-count integrated circuit device having a pin count greater than about 500 such as application specific integrated circuits (ASIC), and said package is selected from the group comprising: ceramic ball grid array (CBGA); tape ball grid array (TBGA); and metal ball grid array (MBGA).



21. The method of claim 17, wherein said semiconductor chip device package is a very-high-pin-count integrated circuit device having a pin count of at least about 1000 such as performance integrated circuit devices, and said package is an area-array solder-bumped flip-chip technology package.

22. The method of claim 17, wherein said passivation layer has openings therein communicating with said voids between said chip interconnects.

23. The method of claim 17, wherein said passivation layer has openings therein communicating with said voids between said chip interconnects, and said vacuum in said voids is created by forming a vacuum over said semiconductor chip device and withdrawing said gasses from said voids through said passivation layer openings, creating a vacuum in said voids.

24. The method of claim 17, wherein said interconnects are dual damascene interconnects.

25. The method of claim 17, wherein said interconnects comprise an upper metal line and a lower metal plug.



26. The method of claim 17, wherein said chip is electrically connected to lead frames extruding from said enclosed package frame.