(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 December 2003 (24.12.2003)

PCT

(10) International Publication Number
WO 03/107425 A2

(51) International Patent Classification[7]: H01L 27/115

(21) International Application Number: PCT/JP03/07431

(22) International Filing Date: 11 June 2003 (11.06.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
NO. 2002-176029 17 June 2002 (17.06.2002) JP

(71) Applicants: **KABUSHIKI KAISHA TOSHIBA** [JP/JP]; 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001 (JP). **INFINEON TECHNOLOGIES AG** [DE/DE]; St-Martin Str. 53, 81669 Munich (DE).

(72) Inventors: **KANAYA, Hiroyuki**; c/o Intellectual Property division, Toshiba Corporation, 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001 (JP). **HILLIGER, Andreas**; 68-27, Yamatemachi, Naka-ku, Yokohama-shi, Kanagawa 231-0862 (JP).

(74) Agents: **SUZUYE, Takehiko** et al.; c/o SUZUYE & SUZUYE, 7-2, Kasumigaseki 3-chome, Chiyoda-ku, Tokyo 100-0013 (JP).

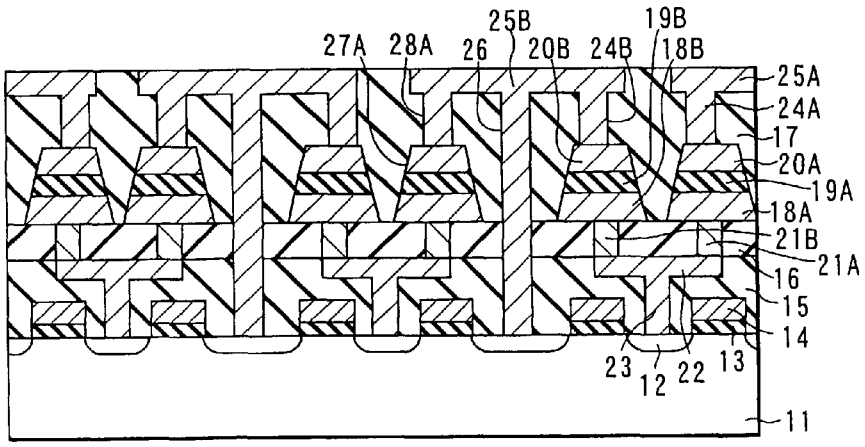
(81) Designated States *(national)*: CN, KR, SG.

(84) Designated States *(regional)*: European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE HAVING FERROELECTRIC FILM AND MANUFACTURING METHOD THEREOF



(57) Abstract: A B S T R A C T First and second semiconductor regions are formed separately from each other in a semiconductor substrate. A gate electrode is formed above the semiconductor substrate which lies between the first and second semiconductor regions. An interlayer insulating film is formed on the semiconductor substrate to cover the first and second semiconductor regions and the gate electrode. First and second lower electrodes are formed on the interlayer insulating film. A first contact plug is formed in the interlayer insulating film in contact with the first lower electrode. A second contact plug is formed in the interlayer insulating film in contact with the second lower electrode. A first ferroelectric film is formed on the first lower electrode. A first upper electrode is formed on the first ferroelectric film. A second ferroelectric film is formed on the second lower electrode. A second upper electrode is formed on the second ferroelectric film.

WO 03/107425 A2