METHOD OF PROCESSING SEMICONDUCTOR WAFERS TO BUILD IN BACK SURFACE DAMAGE

Background of the Invention

The present invention relates generally to a method of processing semiconductor wafers, and, more particularly, to a method of processing semiconductor wafers for producing relatively flat wafers having back surface damage for external gettering.

Semiconductor wafers are generally prepared from a single crystal ingot, such as a silicon ingot, which is trimmed and ground to have one or more flats for proper orientation of the wafer in subsequent procedures. The ingot is then sliced into individual wafers which are each subjected to a number of processing operations to reduce the thickness of the wafer, remove damage caused by the slicing operation, and to create a highly reflective surface. Typically, the peripheral edge of each wafer is rounded to reduce the risk of wafer damage during further processing. A lapping operation (an abrasive slurry process) is then performed on the front and back surfaces of the wafer to reduce the thickness of the wafer and remove damage induced by the slicing operation. A chemical etching operation or a rough grinding operation may also be performed to reduce the thickness and remove damage.

Upon completion of the lapping operation, one or both surfaces of each wafer are usually polished using a polishing pad, a colloidal silica slurry (polishing slurry) and a chemical etchant to remove damage to the surfaces induced by prior operations and to ensure that the wafer is planar. Thereafter, it is often desirable to induce damage on the back surface of each wafer to provide external gettering sites. Conventionally, the back surface of each wafer is subjected to

an abrasive process, such as pressure jetting, or a polysilicon deposition process to induce damage on the back surface for external gettering sites. The front surface of the wafer must be protected while the damage is induced on the back surface. The wafers are then cleaned and the front surface may be finish polished. Finally, the wafers are inspected prior to delivery to the customer for dicing the wafer into semiconductor chips.

The finished wafers must meet certain surface flatness requirements. Such wafers must be polished particularly flat in order to print circuits on them (or on layers deposited upon them) by, for example, an electron beam-lithographic or photolithographic process. Wafer flatness in the focal point of the electron beam delineator or optical printer is important for uniform imaging in the electron beam-lithographic and photolithographic processes. The flatness of the wafer surface directly impacts device line width capability, process latitude, yield and throughput. The continuing reduction in device geometry and increasingly stringent device fabrication specifications are forcing manufacturers of semiconductor wafers to prepare flatter wafers. To achieve flatter wafers, double surface polishing has become the process of choice.

However, flatness is negatively impacted by conventional methods for creating back side damage to facilitate gettering. The conventional method of processing a semiconductor wafer requires a process after double surface polishing in order to induce damage to provide gettering sites on the back surface of the wafer. After this gettering process, an additional polishing process on the front surface of the wafer is

required to remove the processed damage. This additional process can severely degrade the wafer flatness. The additional step is costly in that processing and handling are increased, and it requires that special precautions be taken to protect the front surface from damage.

Summary of the Invention

Among the several objects of this invention may be noted the provision of a method for processing a semiconductor wafer sliced from a single-crystal ingot that reduces the processing required for shaping each wafer; the provision of such a process which produces a relatively flat wafer; the provision of such a process which produces a wafer having gettering sites; and the provision of such a process which is economical for use in processing wafers.

Generally, a method of the present invention for processing a semiconductor wafer sliced from a single-crystal ingot and having front and back surfaces and a peripheral edge comprises lapping the front and back surfaces of the wafer to reduce the thickness of the wafer and to improve the flatness of the wafer. The lapping step creates damage on the front and back surfaces. The method further comprises fine grinding the front surface of the wafer to reduce the damage on the front surface caused by the lapping and to further reduce the thickness of the wafer. During the fine grinding step, the damage on the back surface is left intact. The front and back surfaces of the wafer are simultaneously polished using a polishing slurry to improve the flatness of the wafer and to reduce wafer damage on the front and back surfaces. The wafer damage remaining on the back surface after polishing is greater than the wafer damage on the front surface. The wafer damage remaining on the back surface facilitates gettering.

In another aspect of the invention, a method of processing the semiconductor wafer comprises lapping the front and back surfaces of the wafer to reduce the thickness of the wafer and to improve the flatness of the wafer. The lapping step creates damage on the front and back surfaces. The method further comprises simultaneously polishing the front and back surfaces of the wafer such that less wafer material is removed from the back surface than the front surface. The wafer damage remaining on the back surface is greater than the wafer damage on the front surface. The wafer damage remaining on the back surface facilitates gettering.

Other objects and advantages of the invention will be apparent from the following detailed description.

Brief Description of the Drawings

Fig. 1 is a flow diagram of a method of a first embodiment of the present invention for processing a semiconductor wafer;

Fig. 2 is a flow diagram of a method of a second embodiment.

Detailed Description of the Preferred Embodiments

Fig. 1 illustrates a preferred method of processing a semiconductor wafer in which a fine grinding operation is performed on the front surface before a double surface polishing operation. This method produces a wafer having back surface damage for gettering sites, but does not require a back surface processing step in order to induce back surface damage to provide gettering sites. In other words, no step is performed on the back surface that is not also performed on the front surface.

The semiconductor wafer is sliced from a single-crystal ingot, such as by using a conventional inner diameter saw or conventional wire saw, to have a predetermined initial thickness. The sliced wafer is generally disk-shaped and convex, and has a peripheral edge and opposing front and back surfaces. For purposes of this description, the front surface is the surface upon which devices are ultimately printed. The initial thickness of each wafer is substantially greater than the desired final thickness to allow subsequent processing operations to reduce the thickness of the wafer without the risk of damaging or fracturing the wafer. As an example, the initial thickness may be in the range of about 800-950 microns, while final thickness is about 700-750 microns.

After slicing, the wafer is subjected to ultrasonic cleaning to remove abrasive particles and debris deposited on the wafer from the slicing operation. The peripheral edge of the wafer is profiled (e.g., rounded) by a conventional edge grinder (not shown) to reduce the risk of chipping or fracture of the wafer edge during further processing.

The wafer is then placed in a conventional lapping apparatus (not shown) for lapping the front and back surfaces to reduce the thickness of the wafer and to improve the flatness of the wafer. Reduction of the thickness via the lapping operation also removes damage caused by the wafer slicing operation. The lapping step, however, creates damage (signature damage) on the front and back surfaces that has different characteristics than the damage caused by the wafer slicing operation. Suitable lapping apparatus include Peter Wolters Model Nos. AC1400 and AC2000, manufactured by Peter Wolters Corporation, Plainville, MA. The lapping apparatus preferably employs a slurry including an abrasive, such as alumina or silicon carbide, having grains sized between 5 and 30 microns, and preferably about 15 microns. The lapping

operation removes a predetermined thickness of wafer material, such as about 40 to 120 microns, and preferably about 75-85 microns is removed by the lapping operation. The lapping apparatus removes material from the wafer at a rate preferably between 3 and 20 microns per minute. The operation of the conventional lapping apparatus will be apparent to those skilled in the art and therefore will not be further described.

Once the lapping operation is completed, the wafer is then cleaned and placed in a fine grinding apparatus (not shown) in which the front surface of the wafer is subjected to a fine grinding operation to reduce the damage on the front surface induced by the lapping step and to further reduce the thickness of the wafer. The damage on the back surface is left intact during the fine grinding operation. The fine grinding apparatus is preferably a conventional vertical spindle circumferential grinding apparatus. A suitable fine grinding apparatus is manufactured by Disco Corporation, Santa Clara, CA, under the trade name DFG 840. This apparatus includes a pair of grinding wheels attached to respective motor driven spindles that rotate the grinding wheels and are capable of being moved up and down on a vertical axis. The wafer is drawn by vacuum against a chuck of a support table with one surface of the wafer lying against the chuck and the opposite surface facing one of the grinding wheels in opposed relationship.

As the grinding wheel is rotated by the motor driven spindle, the spindle is lowered along its vertical axis into contact with the wafer to grind down the surface of the wafer. The vertical axis of the spindle is offset from the center of the wafer so that only a peripheral portion of the grinding wheel contacts the wafer. While the grinding wheel is in contact with the wafer, the wafer rotates around its center to

assure uniform grinding of the front surface of the wafer. The grinding wheels used in the grinding apparatus are preferably a cup-shaped, resin bonded diamond grinding wheel known to those skilled in the art as comprising a resin matrix impregnated with grains of suitable size and material for grinding silicon. The average size of the grains impregnated into the resin matrix of the grinding wheel are preferably in the range of .5 to 7 microns, and more preferably in the range of 3 to 5 microns.

The rate at which the grinding wheel is infed toward the wafer for grinding down the wafer thickness (otherwise referred to as the grinding speed) is in the range of about 1 to 35 microns per minute, and more preferably about 15 microns per minute. The fine grinding operation removes a small thickness from the wafer, preferably between 5-20 microns and more preferably about 10 microns. It is to be understood that a grinding apparatus having only a single spindle and grinding wheel may be used for the fine grinding operation without departing from the scope of the invention.

Preferably, the damage remaining on the back surface is not significantly reduced between the lapping step and the polishing step. After the fine grinding operation, particulate matter is removed from the front surface of the wafer, preferably by a conventional chemical etching operation well known to those in the art. This operation is not directed to removing damage from the back surface. A dilute etching solution is used so that the cleaning step removes no more than a small amount of wafer material. Typically, the etching operation will remove about 1 to 2 microns of wafer material.

The wafer is then subjected to a conventional double surface polishing operation (commonly referred to as "double-side polishing" or "DSP") in which both surfaces are polished

simultaneously to improve the flatness of the wafer and to reduce wafer damage on the front and back surfaces. The wafer damage is reduced about the same on the front and back surfaces, but the wafer damage remaining on the back surface is greater than the wafer damage on the front surface. The wafer damage remaining on the back surface facilitates gettering on the back surface. The same apparatus may be used for both the lapping and the DSP steps, such as the AC1400 or the AC2000 machine described above. The DSP apparatus includes polishing pads mounted on rotating plates and an alkali colloidal silica slurry (polishing slurry) supplied to the pad-wafer interface. Suitable polishing pads include Model Nos. H-2 and Suba 600 manufactured by Rodel Corporation, Newark, DE. A suitable slurry is manufactured by E.I. du Pont de Nemours and Co. under the trade name SYTON. The DSP step preferably removes about 10-30 microns of wafer thickness. Preferably, the thickness is removed at a rate of about .5 to 3.5 microns per minute, more preferably about .5 to 2 microns per minute. The DSP step preferably removes nearly all the damage from the front surface, while leaving some amount of damage on the back surface for gettering sites. It will be apparent to those skilled in the art that the thickness necessarily removed in the DSP step will generally vary in relation with the amount of damage caused in the lapping step.

One type of measurement of the amount of damage on the back surface is a count of "oxidation induced stacking faults" (OISF), which indicates the density of damage sites on the wafer surface. Generally, a relatively high OISF count is preferred on the back surface for facilitating gettering. In this invention, the OISF count for the back surface is increased by using a larger grain lapping abrasive, such as about 15 micron alumina grains, and by removing a relatively small amount of wafer thickness in the DSP step, such as about

6 microns. This relationship will be apparent from the examples discussed below. A satisfactory OISF count on a back surface for a typical application would be between about 10,000 and 40,000 counts per square centimeter, but the desired number will vary greatly depending upon the application and customer requirements.

The DSP step flattens the wafer to a flatness that is not attainable in single surface polishing processes. Wafers can be characterized for flatness in terms of a global flatness variation parameter (for example, total thickness variation ("TTV") or in terms of a local site flatness variation parameter (for example, Site Total Indicated Reading ("STIR")). TTV, frequently used to measure global flatness variation, is the difference between the maximum and minimum thicknesses of the wafer. STIR, frequently used to measure local site flatness variation, is the sum of the maximum positive and negative deviations of the surface in a small area of the wafer from a reference plane which is parallel to the back surface of the wafer and intersects the front surface at the center of the local site. A more detailed discussion of the characterization of wafer flatness can be found in F. Shimura, Semiconductor Silicon Crystal Technology (Academic Press 1989), pp. 191-195. For example, a conventional polished semiconductor wafer typically will have a TTV exceeding about 1.0 μm and a STIR (back reference center focus) exceeding about 0.25 μm for any 25mm X 20mm site. The mean TTV and STIR of the wafers after the DSP step in the present invention is significantly lower.

After the DSP step, the front surface is finish polished using a conventional polishing apparatus. The finish polishing step substantially eliminates the damage in the front surface and thus reduces nonspecularly reflected light from the front surface. Typically, about .1 to 3 microns of

wafer thickness is removed in the front surface polishing step, depending on the depth of scratches remaining after the DSP step. However, excessive material removed in the finish polishing step has been found to degrade the flatness of the wafer. It is within the scope of this invention to omit the front surface finish polishing step.

EXAMPLE

Fifteen silicon semiconductor wafers, each having a diameter of 200mm, were processed according to the method illustrated in Fig. 1 and described above as the first embodiment. The lapping operation was performed to remove approximately 80 microns (40 microns on each of the front and back surfaces) of material from each wafer using 15 μm grain lapping slurry. The front surface of each wafer was then subjected to the fine grinding operation to remove an additional 15-17 microns of thickness from the wafer. Each wafer was then subjected to the DSP operation, in which about 5-6 microns were removed from the wafers, an approximately equal amount being removed from the front and back surfaces. The OISF count of the back surface of one wafer was measured at 20,000 per square centimeter after the DSP operation.

SECOND EMBODIMENT

In a second embodiment of this invention shown in Fig. 2, the fine grinding step is omitted. In this second embodiment, slicing, ultrasonic cleaning, edge profiling and lapping are performed as described in the first embodiment, except that the abrasive used in the lapping apparatus is preferably between about 5-10 microns. The smaller size is preferred because it produces less damage on the surfaces, thus reducing the amount of wafer material that must be removed in the DSP step. The wafer is then cleaned and then subjected to a DSP

step similar to the step described in the first embodiment except that more material is removed from the front surface than the back surface.

The DSP step of the second embodiment preferably removes nearly all the damage from the front surface, while leaving some amount of damage on the back surface. The damage sites on the back surface facilitate gettering on the back surface. The DSP apparatus can be set to remove a significantly different amount of material from the front surface than the back surface. This "differential removal" can be accomplished, for instance, by increasing the temperature of the upper polishing pad in contact with the front surface relative to the temperature of the lower polishing pad in contact with the back surface. The temperature of each polishing pad is controlled by circulating water which is in thermal communication with the respective plates in contact with the pads. The AC1400 and AC2000 model polishers include a control system for controlling the temperature of the circulating water in communication with the upper plate and a separate control system for the circulating water in communication with the lower plate. The separate systems enable the user to increase the temperature of the upper polishing pad with respect to that of the lower polishing pad and thereby remove more material from the front surface than the back surface. Alternatively, the differential removal can be accomplished by controlling the rotational velocity of the polishing pads. The effective velocity of the wafers against each polishing pad may be varied so that, for instance, the lower polishing pad moves in the same direction and at nearly the same velocity as the wafer while the upper polishing pad moves in the opposite direction of the wafer. This will cause greater material removal from the front surface than the back surface.

Steps subsequent to the DSP step are performed in the same manner as in the first embodiment. Preferably, none of the damage on the back surface is removed between the lapping and DSP steps. More preferably, no processing is performed on the back surface between the lapping and DSP steps other than cleaning the back surface.

As described herein, the method of the present invention processes the wafer up to and including the finish polishing operation, at which point the wafer is cleaned, packaged and delivered to a customer.

In view of the above, it will be seen that the several objects of the invention are achieved and other advantageous results attained. The present invention is significantly more efficient in producing a relatively flat wafer having back side damage for gettering sites. The invention eliminates the conventional processing step necessary to create damage on the back surface. Damage that is conventionally created on both surfaces during lapping is preserved on the back surface during processing. The invention reduces processing time because it eliminates the need to protect the front surface when the back surface is processed. Moreover, the invention produces a relatively flat wafer because no back side damage step (which degrades flatness) is performed after double side polishing. Damage is "built in" to the back surface of the wafer because more damage is removed from the front surface than the back surface before the DSP step. Thus, the conventional processing step is eliminated and the wafer produced is relatively flat.

When introducing elements of the present invention or the preferred embodiment(s) thereof, the articles "a", "an", "the"

and "said" are intended to mean that there are one or more of the elements. The terms "comprising", "including" and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example and were herein described in detail. It should be understood, however, that it is not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Claims

WHAT IS CLAIMED IS:

1. A method of processing a semiconductor wafer sliced from a single-crystal ingot and having front and back surfaces and a peripheral edge comprising the steps, in order, of:

(a) lapping the front and back surfaces of the wafer to reduce the thickness of the wafer and to improve the flatness of the wafer, the lapping step creating damage on the front and back surfaces;

(b) fine grinding the front surface of the wafer to reduce the damage on the front surface remaining after the lapping step, the damage on the back surface being left intact; and

(c) simultaneously polishing the front and back surfaces of the wafer using a polishing slurry to improve the flatness of the wafer and to reduce wafer damage on the front and back surfaces, the wafer damage remaining on the back surface being greater than the wafer damage on the front surface, the wafer damage remaining on the back surface facilitating gettering.

2. The method set forth in claim 1 wherein the processing of the wafer from lapping up to and including polishing is free of any step performed on the back surface which is not also performed on the front surface.

3. The method set forth in claim 2 wherein the damage on the back surface of the wafer is not substantially reduced between said lapping step and said polishing step.

4. The method set forth in claim 2 further comprising the step of finish polishing the front surface of the wafer to reduce nonspecularly reflected light.

5. The method set forth in claim 2 wherein the step of lapping is conducted at a material removal rate in the range of 3 - 20 microns per minute.

6. The method set forth in claim 5 wherein lapping slurry used in the lapping step includes alumina abrasive material having grains sized in the range of 5 - 30 microns.

7. The method set forth in claim 6 wherein the lapping step reduces the wafer thickness by about 40 - 120 microns, the grinding step further reduces the wafer thickness by about 5 - 20 microns and the simultaneous polishing step further reduces the wafer thickness by about 10 - 30 microns.

8. A method of processing a semiconductor wafer sliced from a single-crystal ingot and having front and back surfaces and a peripheral edge comprising the steps, in order, of:

(a) lapping the front and back surfaces of the wafer to reduce the thickness of the wafer and to improve the flatness of the wafer, the lapping step creating damage on the front and back surfaces; and

(b) simultaneously polishing the front and back surfaces of the wafer such that less wafer material is removed from the back surface than the front surface by polishing the front surface at a higher temperature than the back surface, the wafer damage remaining on the back surface being greater than the wafer damage on the front surface, the wafer damage remaining on the back surface facilitating gettering.

9. The method set forth in claim 8 wherein the damage on the back surface of the wafer is not reduced between said lapping step and said polishing step.