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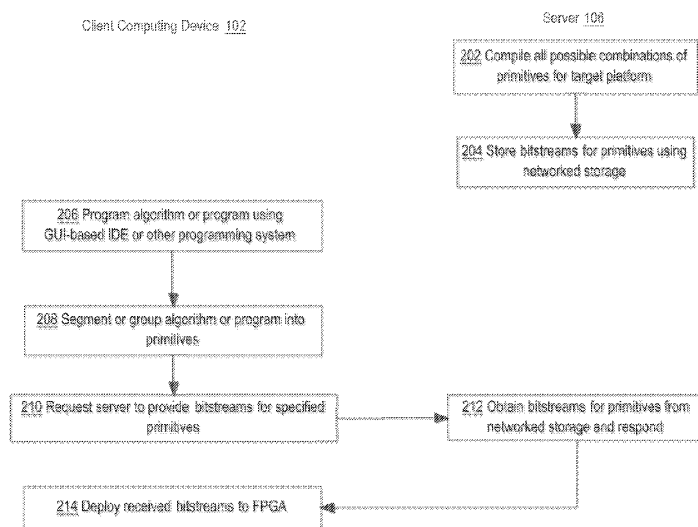
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(54) Title: IMPROVED PROCESS OF PROGRAMMING FIELD PROGRAMMABLE GATE ARRAYS USING PARTIAL RE-CONFIGURATION

Fig. 2



(57) Abstract: Programming field programmable gate array (FPGA) digital electronic integrated circuits (ICs) or other ICs that support partial reconfiguration, a particular FPGA having reconfigurable partitions and primitive variations configurable in each of the reconfigurable partitions, comprises: before writing configuration bitstreams to the FPGA, compiling and storing primitive bitstreams for different primitive functions that can be implemented on the particular FPGA; receiving input in a graphical user interface to connect graphical blocks representing functional logic of an algorithm to implement on the particular FPGA, the graphical blocks relating to reconfigurable logic; automatically determining a subset of the primitive functions comprising particular primitive functions that correspond to the graphical blocks; obtaining, from the digital storage, a subset of the primitive bitstreams that corresponds to the subset of the primitive functions; using partial reconfiguration operations, writing the subset of the primitive bitstreams to the particular FPGA.

[Continued on next page]

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