988,903

PATENT SPECIFICATION 988,903

DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Semiconductor Devices and Methods of Making Same.

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to semiconductor devices and methods of making same and more particularly to semiconductor devices including an epitaxial layer as an integral part thereof, and is divided from our co-pending patent application No. 4150/62 (Serial No. 988,902).

In modern-day electronic packaging, the need for small as well as light-weight electronic devices has become critical. The discovery of the various semiconductor devices such as the transistor and the tunnel diode has made it possible for circuit designers to achieve component densities several orders of magnitude higher than was possible using the vacuum tube circuit components. However, in many applications the size and weight of many electronic systems utilizing the semiconductor devices is much greater than is desired or can be tolerated.

In co-pending British Patent Application No. 3633/60 serial No. 945,734, there is disclosed an unique integrated electronic circuit fabricated from single crystal semiconductor material. As described in this co-pending patent application, circuit modules comprising several different circuit components such as transistors, diodes, resistors and capacitors are fabricated from a single crystal semiconductor structure. These circuit modules are referred to as semiconductor networks and for the purpose of this application a semiconductor network is defined as a single crystal semiconductor structure including at least two circuit components of different types which may be interconnected.

The discovery of these semiconductor networks constituted a major breakthrough in the field of circuit miniaturization in that the entire electronic circuit modules, such as multivibrators, amplifiers or oscillators in a space and of a weight usually allocated to one transistor are available.

Many of these semiconductor networks, however, fail to function as well as the same circuit modules comprising individual components and compromises must be made between the desired reduction in size and weight and the desired circuit characteristics and capabilities. The reason many of the semiconductor networks of the prior art fail to perform as well as their counterparts made from individual components is that the components of each semiconductor network are all formed from the same single crystal of semiconductor material. The transistors, diodes and capacitors are all made by diffusing impurities into this crystal and resistors are made by using the resistivity of the semiconductor material of this crystal. Thus the original characteristics of this crystal affects the properties of all the circuit components that are formed therein. The disadvantage of this fact is that for some components it may be desirable to have one characteristic in some portions of the crystal and for others it may be desirable to have the opposite. For example, for resistors it is usually desirable that the resistivity of the semiconductor material be high because higher resistances may be obtained and a given resistance can be obtained in a shorter dimension. On the other hand, it is usually desirable that transistors be formed out of

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relatively low resistivity material in that in this manner a low saturation voltage is achieved and collector storage is reduced. When such conflicting desires for the characteristics of the crystal of a semiconductor network occur, a compromise must be made resulting in the reduction of the operating quality of the circuit module.

An object of the present invention is to provide a semiconductor device including an epitaxial layer as an integral part thereof with regions of alternating conductivity type arranged in the epitaxial layer with the electrical connections thereto in such a manner that the circuit element characteristics are independent of the characteristics of the substrate on which the epitaxial layer is deposited, thereby permitting such a structure to be especially suitable for semiconductor networks wherein other circuit elements are formed in or on the substrate.

The present invention is a semiconductor device comprising an epitaxial layer overlying a single crystal semiconductor substrate, said layer including three regions of alternating conductivity type extending to one plane surface of said layer and electrical connections respectively to each of said regions attached to said one plane surface.

The present invention is also a method of fabricating a semiconductor device comprising diffusing an impurity into a single crystal semiconductor substrate to form therein a heavily doped surface zone of one conductivity type, thereafter providing on said substrate over said zone an epitaxial layer of said one conductivity type, forming, in said layer, three regions of alternating conductivity type each extending to one plane surface of said layer including diffusing an impurity into said layer to form a first one of said regions of opposite conductivity type whereby the semiconductor material underlying said first one of said regions comprises a second one of said regions, diffusing an impurity into said first one of said regions to form the third one of said regions of said one conductivity type, and attaching electrical connections respectively to each of said regions on said one plane surface.

Embodiments of the invention will now be described, by way of example with reference to the accompanying drawings wherein:

Fig. 1 shows in cross section a semiconductor network of the prior art;

Fig. 2 is a diagram of a circuit provided by the semiconductor network of Fig. 1;

Fig. 3 is a cross-sectional showing of an intermediate stage in the manufacture of a semiconductor network embodying the present invention;

Fig. 4 is a view in perspective of a semiconductor network according to the present invention providing the circuit of Fig. 2;

Fig. 5 is a cross section through the semiconductor network of Fig. 4 along the line 5—5.

The semiconductor network of the prior art illustrated in Fig. 1 comprises a single crystal 11 of relatively high resistivity semiconductor material such as silicon. In the illustrative example of Fig. 1 the crystal 11 has an N-type conductivity and a resistivity of 10 ohm-centimetres. At one end of the block 11 a region 13 of P-type conductivity is formed by diffusion and a heavily doped region 15 of N-type conductivity is formed by diffusion in the region 13. The top of the block 11 is etched to leave a mesa 16 including the region 13 and the region 15 projecting up from the main body of the block 11. The PN junctions between the N-type conductivity region 15 and the remaining P-type conductivity material of the region 13 and between the remaining N-type conductivity material of the block 11 and the P-type conductivity material of the region 13 from an NPN transistor in the mesa 16 with the P-type conductivity material of the region 13 providing the base, the region 15 providing the emitter and the remaining N-type conductivity material of the block 11 providing the collector. An ohmic contact 17 is provided to the P-type conductivity material of the region 13 and acts as the base electrode of the transistor. An ohmic contact 21 to the block 11 directly beneath the mesa 16 provides the collector electrode of the transistor, and an ohmic contact 23 to the heavily doped region 15 provides the emitter electrode of the transistor. At the opposite end of the block 11 from the mesa 16, an ohmic contact 19 is provided. The relatively high resistivity material between the contacts 19 and 21 in the block 11, in effect, provides a resistor connected to the collector of the transistor in the mesa 16.

Fig. 2 illustrates schematically the circuit provided by the semiconductor network of Fig. 1. As shown in Fig. 2, a resistor 25 is connected between a terminal 18 and the collector of an NPN transistor 27. A terminal 24 is connected to the emitter of the transistor 27, a terminal 22 is connected to the base of the transistor 27, and a terminal 20 is connected to the collector of the transistor 27, or in other words to the junction between the resistor 25 and the collector of the transistor 27. The resistor 25 is provided by the resistivity of the semiconductor material between contacts 19 and 21 and the transistor 27 is provided by the transistor of the mesa 16. The terminals 18, 20, 22 and 24 are provided by the contacts 19, 21, 17 and 23 respectively. Because of the difficulty of forming ohmic contacts on high resistivity material, as a practical matter the resistivity

of the block 11 is limited to 10 ohm-centimetres. As a result, the resistor 25 provided by the base 11 has a maximum value of 40,000 ohms in a practical embodiment of this semiconductor network. Furthermore, the use of material of even this high resistivity in the block 11 has resulted in several serious compromises in the design of the transistor 27. Because the relatively high resistivity material of the block 11 provides the collector of the transistor 27, the transistor 27 will have a relatively high value of saturation voltage. This high saturation voltage is undesirable, particularly when the transistor 27 is to be used in a switching application. For in a switching application it is desired that when the transistor 27 is conducting or turned on, the transistor will act as nearly as possible as a short circuit. Because the transistor 27 has a relatively high saturation voltage, it will have a relatively high voltage between its collector and emitter when it is conducting or turned on and thus will not approach the desired short circuit. Furthermore, the relatively high resistivity of the collector of the transistor 27 provided by the block 11 also permits increased collector storage, which results in a considerably slower switching time for the device.

The present invention enables the circuit of Fig. 2 to be provided by a semiconductor network in which a much high resistivity material provides the resistor 25, thus obtaining a much higher resistance for the resistor 25, whereas the collector region of the transistor 27 is provided by a much lower resistivity material. The improved semiconductor network providing the circuit of Fig. 2 embodying the present invention is illustrated in Figs. 3 to 5.

As shown in Fig. 3, which illustrates the semiconductor network in an intermediate stage of manufacture, a high resistivity single crystal of semiconductor material in wafer form designated by the reference number 29 is provided. In the embodiment of Figs. 3 to 5, the wafer 29 will have a resistivity of 100 ohm-centimetres and is of N-type conductivity. Two heavily doped N-type regions or zones 31 and 32 (about 0.1 ohm-centimetres or less) are formed by diffusion into the top surface of the wafer 29 at opposite ends thereof. On top of the wafer or substrate 29 an epitaxial layer 33 of semiconductor material is grown. The layer 33 will be a continuation of the single crystal, which is essential. The term "epitaxial layer" as used herein and in the claims is to be construed as meaning a layer having the same crystalline structure as the substrate on or over which it is epitaxially grown or deposited. One way to produce this epitaxial layer is to vapour deposit semiconductor material on the base or substrate 29 in accordance with the disclosure in "Epitaxial Growth of Silicon" by Wajda et al IBM Journal of Research and Development, 4, pages 288—295 (1960) and "Impurity Introduction During Epitaxial Growth of Silicon" by Glang et al, IBM Journal of Research and Development, 4, pages 299—301 (1960). The characteristics, including the resistivity and the conductivity type of the epitaxial layer, can be freely selected. In the embodiment of Fig. 3 the conductivity is selected to be of N-type and the resistivity is selected to be relatively low, and preferably between 0.5 and 1.0 ohm-centimetres. A P-type region 35 is formed in the N-type epitaxial layer 33 by diffusion. This region 35 is formed over the heavily doped N-type region 31 in the wafer 29. A heavily doped N-type region 37 is formed in the P-type region 35 by diffusion. Also a heavily doped N-type region 39 is formed in the N-type material of the layer 33 alongside of the region 35 by diffusion and a heavily doped N-type region 41 is formed in the layer 33 over the N-type region 32 by diffusion. The epitaxial layer 33 is then etched to leave the mesas designated generally in Figs. 4 and 5 by the reference numbers 43 and 45. The layer 33 is etched entirely away so that the mesas 43 and 45 are joined only by the high resistivity material of the wafer 29. The etching is carried out so that the mesa 43 contains the P-type region 35 with the N-type region 37 therein and also the heavily doped N-type region 39 and the mesa 45 contains the heavily doped N-type region 41. The regions in the mesa 43 form a transistor with the N-type region 37 providing the emitter, the P-type material of the region 35 providing the base, and the remaining N-type material of the layer 33 in the mesa 43 providing the collector. The heavily doped N-type region 39 in the mesa 43 is used to provide a contact to the collector of the transistor. An ohmic contact 49 is made to the heavily doped N-type region 37 to provide the emitter electrode, an ohmic contact 47 is made to the remaining P-type material in the region 35 to provide the base electrode, and an ohmic contact 48 is made to the region 39 to provide the collector electrode. An ohmic contact 50 is made to the heavily doped region 41. This semi-conductor network shown in Figs. 4 and 5 will provide the circuit illustrated in Fig. 2 with the mesa 43 providing the transistor 27 and with the semiconductor material between the mesas 45 and 43 providing the resistor 25. The terminals 18, 20, 22 and 24 are provided by the contacts 50, 48, 47 and 49, respectively. Because high resistivity material is used for the wafer 29, the resistance of the resistor 25 may be made much higher and also the wafer 29 does not have to be made nearly as long to provide an

adequately high resistance. Furthermore, the resistivity of the collector region of the transistor 27 is substantially reduced since this collector region is provided by the epitaxial layer 33 which has a relatively low resistivity. Thus, the translator 27 will have a low saturation voltage permitting it to act more as a short circuit when it is switched on and also it will have greatly reduced collector storage resulting in a much faster switching time for the transistor 27. Furthermore, the provision of the heavily doped region 41 in the low resistivity epitaxial layer in the mesa 45 formed on the heavily doped region 32 in the high resistivity base permits a good ohmic contact to the high resistivity material. Similarly, the heavily doped region 31 makes a good ohmic contact between the collector region of the transistor and the high resistivity material of the wafer 29 and also limits depletion layer width in the collector noticeably improving switching characteristics of the transistor. Thus, all of the problems discussed above associated with the semiconductor network of the prior art illustrated in Fig. 1 are overcome by the use of the epitaxial layer 33 and the various heavily doped zones in forming the semiconductor network.

As illustrated in Fig. 3, the epitaxial layer permits a heavily doped region such as the regions 31 and 32 to be completely surrounded in a single crystal structure by material that is more lightly doped. In the embodiment in Figs. 4 and 5, these buried regions 31 and 32 permit good ohmic contact to be made to the high resistivity material of the wafer 29. It will be obvious that this structure will have many other applications in semiconductor networks and the achievement of this structure vastly widens the horizon in the technology of this field.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising an epitaxial layer overlying a single crystal semiconductor substrate, said layer including three regions of alternating conductivity type extending to one plane surface of said layer and electrical connections respectively to each of said regions attached to said one plane surface.

2. A semiconductor device according to claim 1, wherein said layer includes, on its surface in one of said regions, a heavily doped zone having the same conductivity type as that region and wherein said heavily doped zone is under the electrical connection to that region.

3. A semiconductor device according to claim 2, including a heavily doped zone beneath said one of said regions and having the same conductivity type thereas.

4. A semiconductor device according to claim 3, wherein said one of said regions is the collector region of a transistor, and the other of said regions are the base and emitter regions of said transistor.

5. A method of fabricating a semiconductor device comprising diffusing an impurity into a single crystal semiconductor substrate to form therein a heavily doped surface zone of one conductivity type, thereafter providing on said substrate over said zone an epitaxial layer of said one conductivity type, forming, in said layer, three regions of alternating conductivity type each extending to one plane surface of said layer including diffusing an impurity into said layer to form a first one of said regions of opposite conductivity type whereby the semiconductor material underlying said first one of said regions comprises a second one of said regions, diffusing an impurity into said first one of said regions to form the third one of said regions of said one conductivity type, and attaching electrical connections respectively to each of said regions on said one plane surface.

6. A method according to claim 5, including forming another heavily doped zone of said one conductivity type in said second one of said regions prior to attaching the electrical connection to that region and thereafter attaching the electrical connection to that region on said another heavily doped zone.

7. A semiconductor device when produced by the method of claim 5 or 6.

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adequately high resistance. Furthermore, the resistivity of the collector region of the transistor 27 is substantially reduced since this collector region is provided by the epitaxial layer 33 which has a relatively low resistivity. Thus, the translator 27 will have a low saturation voltage permitting it to act more as a short circuit when it is switched on and also it will have greatly reduced collector storage resulting in a much faster switching time for the transistor 27. Furthermore, the provision of the heavily doped region 41 in the low resistivity epitaxial layer in the mesa 45 formed on the heavily doped region 32 in the high resistivity base permits a good ohmic contact to the high resistivity material. Similarly, the heavily doped region 31 makes a good ohmic contact between the collector region of the transistor and the high resistivity material of the wafer 29 and also limits depletion layer width in the collector noticeably improving switching characteristics of the transistor. Thus, all of the problems discussed above associated with the semiconductor network of the prior art illustrated in Fig. 1 are overcome by the use of the epitaxial layer 33 and the various heavily doped zones in forming the semiconductor network.

As illustrated in Fig. 3, the epitaxial layer permits a heavily doped region such as the regions 31 and 32 to be completely surrounded in a single crystal structure by material that is more lightly doped. In the embodiment in Figs. 4 and 5, these buried regions 31 and 32 permit good ohmic contact to be made to the high resistivity material of the wafer 29. It will be obvious that this structure will have many other applications in semiconductor networks and the achievement of this structure vastly widens the horizon in the technology of this field.

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2. A semiconductor device according to claim 1, wherein said layer includes, on its surface in one of said regions, a heavily doped zone having the same conductivity type as that region and wherein said heavily doped zone is under the electrical connection to that region.

3. A semiconductor device according to claim 2, including a heavily doped zone beneath said one of said regions and having the same conductivity type thereas.

4. A semiconductor device according to claim 3, wherein said one of said regions is the collector region of a transistor, and the other of said regions are the base and emitter regions of said transistor.

5. A method of fabricating a semiconductor device comprising diffusing an impurity into a single crystal semiconductor substrate to form therein a heavily doped surface zone of one conductivity type, thereafter providing on said substrate over said zone an epitaxial layer of said one conductivity type, forming, in said layer, three regions of alternating conductivity type each extending to one plane surface of said layer including diffusing an impurity into said layer to form a first one of said regions of opposite conductivity type whereby the semiconductor material underlying said first one of said regions comprises a second one of said regions, diffusing an impurity into said first one of said regions to form the third one of said regions of said one conductivity type, and attaching electrical connections respectively to each of said regions on said one plane surface.

6. A method according to claim 5, including forming another heavily doped zone of said one conductivity type in said second one of said regions prior to attaching the electrical connection to that region and thereafter attaching the electrical connection to that region on said another heavily doped zone.

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