

SEMICONDUCTOR PACKAGE WITH POSITION MEMBER AND METHOD OF MANUFACTURING THE SAME

Field of the Invention

[0001] The present invention generally relates to semiconductor packages and packaging technologies, and more particularly to a semiconductor package with at least one position member and a method for manufacturing the semiconductor package.

Background of the Invention

[0002] In semiconductor package designs, semiconductor dies are mounted onto a substrate, and then encapsulated in a mold cavity. As semiconductor packages get thinner and thinner, molding cavity and molding gaps are so stretched that only a very thin layer of molding compound covers the die(s). Therefore, any variation of compound thickness will result in package warping. In addition, mismatch of coefficient of thermal expansion (CTE) between various materials inside a thin package can cause huge warpage.

[0003] Thin semiconductor packages employ thin dies and leadframes. As a result, when the die and leadframe thickness gets thinner, they are more prone to flexing during the assembly process. FIG 1 shows an exemplary thin semiconductor package 1 that comprises a split pad 2, a lead terminal 3, a die 4, a bond wire 5, and an encapsulant 6. Since the gap between the pad and the upper molding surface (not shown) is very narrow, the mold flow will cause the die to flex (from 4 to 4') and the die pad to shift.

[0004] Attempts have been made to remedy the warpage problems for semiconductor packages. For example, U.S. 6,331,448 discloses a semiconductor package that comprises a leadframe including offsets from a major plane at a non-perpendicular angle thereto. It claims that the offsets are useful for preventing warpage, bowing, skewing, or other distortions of the semiconductor package when subjected to the high temperature or changes in temperature. As another example, U.S. 6,020,221 discloses a semiconductor device that comprises a stiffener member, where the stiffener member is attachable to the semiconductor package substrate for purposes of minimizing package

warpage. But none concerns the flexing problem of die and/or die-attach pad during the molding process.

[0005] There are also attempts made to remedy the displacement of assembly components during the molding process of a semiconductor package. For example, U.S. 6,028,368 discloses a semiconductor device with potting resin structures that are affixed to a plurality of predetermined faces of the leadframe so as to limit the shifting of the die and leadframe structures during the molding process. However, these potting structures may not be able to stop the vertical movement of the die and leadframe completely.

[0006] Another example is the encapsulation of dies mounted on a flexible tape substrate. When positioned in a mold tooling, as a molding compound flows into the mold chamber and around the mounted die, the flexible tape can flutter and become warped or bent resulting in a bowed die structure, and an uneven layer of encapsulant formed around the die structure, which can lead to structure failure. U.S. 2005/0023562 A1 discloses a semiconductor device that comprises a pair of semiconductor dies mounted on opposing sides of a flexible tape substrate, the outer surfaces of the dies having one or more standoffs disposed thereon. The standoffs can be brought into contact with an inner surface of the mold plates of a mold tooling when the device is positioned between the mold plates to maintain the flexible tape substrate in a centralized position within a mold chamber and inhibit the tape from bending as a molding compound flows into the chamber during encapsulation. This may be perfectly suitable for flexible substrate when the semiconductor device is bulky. As for thin semiconductor packages, however, both the warpage and die/pad flexing have to be taken into consideration.

Summary of the Invention

[0007] Therefore, one of the objectives of the present invention is to provide a very thin semiconductor package that has a good balance of warpage and die/pad flexing.

[0008] The present invention provides a very thin semiconductor package that, in one embodiment, comprises a leadframe with a die-attach pad and a plurality of lead terminals, a die attached to the die-attach pad and electrically connected to the lead terminals via bonding wires, a position member disposed upon the die and/or die-attach pad, and a molding material encapsulating the leadframe, the die, and the position member

together to form the semiconductor package. The position member is used for controlling the die Z-position within the very thin semiconductor package so as to prevent large variation from occurring during the package assembly process.

[0009] The present invention further provides a method for manufacturing a very thin semiconductor package. In one embodiment, the method comprises the steps of disposing a first position member on one side of the die-attach pad of a leadframe, attaching a die onto the opposite side of the die-attach pad, optionally disposing a second position member on top of the die, electrically connecting the die to the lead terminals of the leadframe, and encapsulating the leadframe, the die, and the position member(s) together to form the very thin semiconductor package.

[0010] One advantage of the present invention is that the very thin semiconductor package may be manufactured without redesigning new leadframes.

[0011] Another advantage of the present invention is that die thickness and die attaching process are well controlled; the extra steps are multiple passes of die attaching.

[0012] Yet another advantage of the present invention is that the manufacturing process for die stacking is well established and currently being done for System-In-Package.

[0013] These and additional objectives and advantages of the invention will become apparent from the following detailed description of preferred embodiments thereof in connection with the accompanying drawings.

Brief Description of the Drawings

[0014] Preferred embodiments according to the present invention will now be described with reference to the Figures, in which like reference numerals denote like elements.

[0015] FIG 1 illustrates the die/pad flexing problem encountered in the molding process of a very thin semiconductor package.

[0016] FIG 2A shows a cross-section view of one die-down very thin semiconductor package in accordance with one embodiment of the present invention.

[0017] FIG 2B shows a cross-section view of another die-down very thin semiconductor package with an offset die-attach pad in accordance with one embodiment of the present invention.

[0018] FIG 2C shows another embodiment of the die-up semiconductor package that is similar to the one shown in FIG 2B.

[0019] FIG 2D shows another embodiment of the die-down semiconductor package with a split die-attach pad.

[0020] FIGS 3A-3E shows an illustrative process for manufacturing a very thin semiconductor package with two position members in accordance with one embodiment of the present invention.

[0021] FIG 4 shows a very thin semiconductor package design for warpage test.

Detailed Description of the Invention

[0022] The present invention may be understood more readily by reference to the following detailed description of certain embodiments of the invention.

[0023] Throughout this application, where publications are referenced, the disclosures of these publications are hereby incorporated by reference, in their entireties, into this application in order to more fully describe the state of art to which this invention pertains.

[0024] The present invention provides a very thin semiconductor package that has a good balance of warpage and die/pad flexing, and a method for manufacturing the very thin semiconductor package. Prior to detailed description of the package and method, it is to be appreciated that the basic manufacturing technology and semiconductor designs are well known to those skilled in the art. Therefore, if the missing of any details will not affect the practice of the principles of the present invention, the details will not be provided herein for the sake of brevity and simplicity.

[0025] Briefly, the very thin semiconductor package in accordance with one embodiment of the present invention comprises a leadframe with a die-attach pad and a plurality of lead terminals, a die attached to the die-attach pad and electrically connected to the lead terminals via bonding wires, a position member disposed upon the die and/or die-attach pad, and a molding material encapsulating the leadframe, the die, and the position

member together to form the semiconductor package. The position member is used for controlling the die Z-position within the very thin semiconductor package so as to prevent large variation from occurring during the package assembly process. The “Z-position” used herein refers to the vertical variation.

[0026] Now referring to FIG 2A, the very thin semiconductor package 10 comprises a leadframe with lead terminals 11 and die-attach pad 12, a die 13 disposed onto the die-attach pad 12, bonding wires 14 electrically connecting the die 13 and the lead terminals 11, two position members 15, 16 disposed directly under the die 13 or directly above the die-attach pad 12 for preventing large variation occurrence during package assembly process, and a molding compound 17 for encapsulating the semiconductor package. In certain embodiments, the position member could be an integral part of the leadframe. FIG 2B shows another embodiment of the die-down semiconductor package that comprises only one position member and, in addition, has a down-set die-attach pad in comparison with the lead terminals. FIG 2C shows another embodiment of the die-up semiconductor package that is similar to the one shown in FIG 2B. FIG 2D shows another embodiment of the die-down semiconductor package that has a split die-attach pad so that each part of the die-attach pad has a position member.

[0027] The leadframe could be preformed, e.g., at the tie bar, such that the position member can always maintain a fixed height flush against the surface of the mold by the use of spring effect from the down-set as shown in FIG 2B, 2C, and 2D. The leadframe may be manufactured from any available leadframe material known to those skilled in the art. In the preferred embodiment, the leadframe is composed of Cu, PPF, or Alloy 42.

[0028] The die-attach pad may have any suitable design. In certain embodiments, the die-attach pad has a split configuration.

[0029] The position members may be made of any suitable material. In the preferred embodiment, the position members are composed of Si, Cu, or Epoxy.

[0030] The materials for die attach may be any available die attach material known to those skilled in the art. In the preferred embodiment, the die attach material is paste, tape, or deformable adhesives.

[0031] The wires for wire bonding may be any available wire bonding material known to those skilled in the art. In the preferred embodiment, the wires for wire bonding are composed of gold, copper, or aluminum.

[0032] The molding compound may be any available molding material known to those skilled in the art. It may be hard or soft deformable material.

[0033] Now there is provided a detailed description of assembling the semiconductor package in accordance with one embodiment of the present invention. The assembly process initially provides a leadframe with a die-attach pad and a plurality of lead terminals. While the process is illustrated using a single die-attach pad, it is totally applicable to a split design die-attach pad.

[0034] Referring to FIGS 3A-3E, the assembling process starts with disposing a first position member **16** to one side of the die-attach pad **12** as shown in FIG 3A. If the die-attach pad is a split design, each pad will be disposed with one position member. In one embodiment, the position member may be adhered to the leadframe by adhesives such as glue, paste, tape and deformable material. In another embodiment, the position member may be an integrated part of the leadframe, so that this step may be omitted altogether. Then, one die **13** is attached to the die-attach pad using any conventional die attach techniques as shown in FIG 3B. Then, a second position member **15** is optionally disposed onto the top of the die as the first position member as shown in FIG 3C. Then, the die is electrically connected to the lead terminals **11** of the leadframe by wire bonding **14** as shown in FIG 3D. The wire bonding can be done using any of the available techniques known to those skilled in the art. Finally, the leadframe, die, bonding wires, and position member(s) are encapsulated by a molding compound **17** via injection molding as shown in FIG 3E. The mold **18** can be any suitable molding device. It is to be appreciated that the typical sequence of assembly of the package is not restricted to the sequences as described above. For example, the attaching of the position member can be done before or after the die attach process is completed. In addition, the position members are exposed at the surface of the packages.

[0035] In certain embodiments, the position member may be made of thermal conductive materials. When the adhesive materials used for the position member attachment are thermal conductive, the exposure of the position members on the surface of the very thin semiconductor package will enhance the thermal performance of the package.

[0036] Examples

[0037] The following model examples are provided for the sole purpose of illustration of some embodiments of the present invention. They are by no means intended to limit the practice of the principles of the present invention.

[0038] As shown in FIG 4, there is provided a model semiconductor package that is manufactured in accordance with an embodiment of the present invention. In FIG 4, PM is for position member thickness; PMA for position member attach thickness; DP for Die Pad Thickness; DT for Die Thickness; DA for Die Attach Thickness; UR for Resin thickness in upper cavity; and DR for Resin thickness in lower cavity. The model semiconductor packages were subjected to warpage tests. The split pad package as a control case comprises a copper leadframe with split pad design, while the full pad package comprises a full pad design. The simulation results are shown in Table 1. Negative warpage means that the edge of package warps down and its center warps up. Positive warpage means that the edge of package warps up and its center warps down.

[0039] Table 1. Effects of different position member on warpages

	No position member	With position member 3x3mm (silicon)	With position member 3x3mm (copper)
Control case	4.3um	-33.2um	18.26um
Full pad	-35.32um	-64.25um	-15.72um

[0040] The warpage tests were conducted with different sizes of position member. When the package design with a split pad was tested with different sizes of position members, the warpages increased with the increase of the sizes of position members. The results are shown in Table 2.

[0041] Table 2 shows the effects of the size of position member on the warpages.

No position member	position member 1x1mm	position member 2x2mm	position member 3x3mm	position member 4x4mm
4.3um	-6.42um	-17.52um	-33.2um	-51.81um

[0042] The introduction of a position member into a semiconductor package in accordance with the principles of the present invention has been experimentally determined to significantly increase the yield of the molding process during packaging. When semiconductor packages are without any position members, the dies and bonding materials can be subjected to substantial offset flexing by high speed molding processes. The offset flexing has two effects on the final semiconductor packages: (1) the dies and bonding

materials may lose their good contacts so that the packages will have dissatisfactory electronic characteristics, and (2) the offset dies and bonding materials can cause very substantial warpages when the offset flexing is substantial. Such very substantial warpages typically disqualify the affected packages from further applications. Notably, the two effects of offset flexing are not mutually exclusive, but rather can both be present in a single semiconductor package.

[0043] While a position member as disclosed herein can reduce or prevent the substantial package warpages described, the position member can also introduce small but acceptable warpages into packages. The afore-mentioned examples illustrate increased warpage as a result of the addition of position member(s). In addition, position-member size can correlate with increased warpages.

[0044] Warpage is defined as the deviation of edges and center from an assumed plane. When the position member and the remaining package are composed of different materials, warpage may be increased. Moreover, it appears from the examples that the material composition of the position member can further affect warpage. Routine experimentation will determine appropriate selection of materials for a position-member.

[0045] While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Alternative embodiments of the present invention will become apparent to those having ordinary skill in the art to which the present invention pertains. Such alternate embodiments are considered to be encompassed within the spirit and scope of the present invention. Accordingly, the scope of the present invention is described by the appended claims and is supported by the foregoing description.

CLAIMS

What is claimed is:

1. A very thin semiconductor package, comprising:
 - a leadframe with a plurality of lead terminals and a die-attach pad;
 - a die disposed onto the die-attach pad;
 - a plurality of bonding wires electrically connecting the die and the plurality of lead terminals;
 - at least two position members for preventing large variation occurrence during package assembly process, wherein one of the at least two position members is disposed onto the die and one of the at least two position members is disposed onto the die-attach pad; and
 - a molding compound for encapsulating the leadframe, the die, the bonding wires, the position member so as to form the very thin semiconductor package.
2. The very thin semiconductor package of claim 1, wherein, when the die-attach pad has a split die-attach pad design, each part of the die-attach pad has a position member.
3. The very thin semiconductor package of claim 1, wherein the leadframe is made of at least one material selected from the group consisting of Cu, PPF, and Alloy 42.
4. The very thin semiconductor package of claim 1, wherein the position members are made of at least one material selected from the group consisting of Si, Cu, and Epoxy.
5. The very thin semiconductor package of claim 1, wherein the position member is made of thermal conductive materials; thereby, when a thermal conductive adhesive material is used for the position member attachment, the exposure of the position member on the surface of the very thin semiconductor package will enhance the thermal performance of the package.

6. The very thin semiconductor package of claim 1, wherein the wire bonding is made of at least one material selected from the group consisting of gold, copper, and aluminum.
7. The very thin semiconductor package of claim 1, wherein the position member is an integral part of the leadframe.
8. A method for manufacturing a very thin semiconductor package, said method comprising the steps of:
 - providing a leadframe with a plurality of lead terminals and a die-attach pad;
 - disposing a first position member to one side of the die-attach pad
 - disposing a die to another side of the die-attach pad opposite to the first position member;
 - disposing a second position member onto the top of the die opposite to the die-attach pad;
 - electrically connecting die to the plurality of lead terminals; and
 - encapsulating the leadframe, die, bonding wires, and position member so as to form the very thin semiconductor package.
9. The method of claim 8, wherein the disposing of die and position member uses adhesives selected from the group consisting of glue, paste, tape and deformable material.
10. The method of claim 8, wherein the electrically connecting of the die to the lead terminals is done by wire bonding.
11. The method of claim 8, wherein the wire bonding is made of a material selected from the group consisting of gold, copper, and aluminum.
12. The method of claim 8, wherein, when the die-attach pad has a split die-attach pad design, each part of the die-attach pad has a position member.
13. The method of claim 8, wherein the leadframe is made of a material selected from the group consisting of Cu, PPF, and Alloy 42.

14. The method of claim 8, wherein the position member is made of a material selected from the group consisting of Si, Cu, and Epoxy.

15. The method of claim 8, wherein the position member is made of thermal conductive materials; thereby, when a thermal conductive adhesive material is used for the position member attachment, the exposure of the position member on the surface of the very thin semiconductor package will enhance the thermal performance of the package.

16. The method of claim 8, wherein the position member is an integral part of the leadframe.

17. A method for manufacturing a very thin semiconductor package, said method comprising the steps of:

providing a leadframe with a plurality of lead terminals and a die-attach pad;

disposing a die to one side of the die-attach pad;

disposing a first position member to the other side of the die;

disposing a second position member onto the other side of the die-attach pad opposite to the die;

electrically connecting die to the plurality of lead terminals; and

encapsulating the leadframe, die, bonding wires, and position member so as to form the very thin semiconductor package.

18. The method of claim 17, wherein the disposing of die and position member uses adhesives selected from the group consisting of glue, paste, tape and deformable material.

19. The method of claim 17, wherein the electrically connecting of the die to the lead terminals is done by wire bonding.

20. The method of claim 17, wherein the wire bonding is made of a material selected from the group consisting of gold, copper, and aluminum.

21. The method of claim 17, wherein the die-attach pad has a split die-attach pad design.
22. The method of claim 17, wherein, when the die-attach pad has a split die-attach pad design, each part of the die-attach pad has a position member.
23. The method of claim 17, wherein the leadframe is made of a material selected from the group consisting of Cu, PPF, and Alloy 42.
24. The method of claim 17, wherein the position member is made of a material selected from the group consisting of Si, Cu, and Epoxy.
25. The method of claim 17, wherein the position member is made of thermal conductive materials; thereby, when a thermal conductive adhesive material is used for the position member attachment, the exposure of the position member on the surface of the very thin semiconductor package will enhance the thermal performance of the package.
26. The method of claim 17, wherein the position member is an integral part of the leadframe.