WORK FUNCTION LAYER FOR PMOS STACK

TECHNICAL FIELD

[0001] Embodiments of the present disclosure pertain to the field of semiconductor device manufacturing, and in particular, to transistors. More particularly, embodiments of the disclosure are directed to FinFET and GAA devices and methods of manufacturing FinFET and GAA devices.

BACKGROUND

[0002] Integrated circuits have evolved into complex devices that can include millions of transistors, capacitors, and resistors on a single chip. In the course of integrated circuit evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased.

[0003] Transistors are circuit components or elements that are often formed on semiconductor devices. Many transistors may be formed on a semiconductor device in addition to capacitors, inductors, resistors, diodes, conductive lines, or other elements, depending on the circuit design. Integrated circuits incorporate planar field-effect transistors (FETs) in which current flows through a semiconducting channel between a source and a drain, in response to a voltage applied to a control gate.

[0004] With more advanced device scaling, it is becoming more challenging for PMOS high-k metal gate (HKMG) stacks to achieve the desired bandedge performance because of the significant flatband voltage (V_{fb}) rolloff, potentially due to Fermi level pinning.

[0005] Accordingly, there is a need for semiconductor devices and methods of manufacturing such semiconductor devices that achieve the desired bandedge performance.

SUMMARY

[0006] One or more embodiments of the disclosure are directed to methods of manufacturing a semiconductor device. In one or more embodiments, a method of manufacturing a semiconductor device comprises: depositing an interfacial layer on a

top surface of a channel located between a source and a drain on a substrate; depositing a high-κ dielectric layer on the interfacial layer; depositing a depinning layer on the high-κ dielectric layer; depositing a P-metal layer on the depinning layer; and depositing a barrier layer on the P-metal layer.

[0007] Additional embodiments of the disclosure are directed to methods of manufacturing semiconductor devices comprising: depositing an interfacial layer on a top surface of a channel located between a source and a drain on a substrate; depositing a high-κ dielectric layer on the interfacial layer; depositing a depinning layer on the high-κ dielectric layer, the depinning layer a metal selected from one or more of aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), vanadium (V), niobium (Nb), ruthenium (Ru), antimony (Sb), and tin (Sn) and the depinning layer having a work function about 4.4 eV to about 4.7 eV; depositing a P-metal layer on the depinning layer, the P-metal layer comprising a metal selected from one or more of titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt), iridium (Ir), nickel (Ni), palladium (Pd), cobalt (Co), ruthenium (Ru), and molybdenum (Mo); and depositing a barrier layer on the P-metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments. The embodiments, as described herein, are illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references indicate similar elements.

[0009] FIG. 1 depicts a process flow diagram of a method according to one or more embodiments described herein;

[0010] FIG. 2A illustrates a cross-sectional view of a semiconductor device according to one or more embodiments;

[0011] FIG. 2B illustrates a cross-sectional view of a semiconductor device

according to one or more embodiments;

[0012] FIG. 2C illustrates a cross-sectional view of a semiconductor device according to one or more embodiments;

[0013] FIG. 2D illustrates a cross-sectional view of a semiconductor device according to one or more embodiments;

[0014] FIG. 2E illustrates a cross-sectional view of a semiconductor device according to one or more embodiments; and

[0015] FIG. 3 illustrates a cluster tool according to one or more embodiments of the disclosure.

DETAILED DESCRIPTION

[0016] Before describing several exemplary embodiments of the disclosure, it is to be understood that the disclosure is not limited to the details of construction or process steps set forth in the following description. The disclosure is capable of other embodiments and of being practiced or being carried out in various ways.

[0017] The term “about” as used herein means approximately or nearly and in the context of a numerical value or range set forth means a variation of ±15%, or less, of the numerical value. For example, a value differing by ±14%, ±10%, ±5%, ±2%, or ±1%, would satisfy the definition of about.

[0018] As used in this specification and the appended claims, the term "substrate" or "wafer" refers to a surface, or portion of a surface, upon which a process acts. It will also be understood by those skilled in the art that reference to a substrate can refer to only a portion of the substrate unless the context clearly indicates otherwise. Additionally, reference to depositing on a substrate can mean both a bare substrate and a substrate with one or more films or features deposited or formed thereon.

[0019] A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, amorphous silicon, doped silicon, germanium, gallium arsenide, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include,

without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal and/or bake the substrate surface. In addition to film processing directly on the surface of the substrate itself, in the present disclosure, any of the film processing steps disclosed may also be performed on an under-layer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such under-layer as the context indicates. Thus, for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface.

[0020] The term "on" indicates that there is direct contact between elements. The term "directly on" indicates that there is direct contact between elements with no intervening elements.

[0021] As used in this specification and the appended claims, the terms "precursor", "reactant", "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

[0022] "Atomic layer deposition" or "cyclical deposition" as used herein refers to the sequential exposure of two or more reactive compounds to deposit a layer of material on a substrate surface. The substrate, or portion of the substrate, is exposed separately to the two or more reactive compounds which are introduced into a reaction zone of a processing chamber. In a time-domain ALD process, exposure to each reactive compound is separated by a time delay to allow each compound to adhere and/or react on the substrate surface and then be purged from the processing chamber. These reactive compounds are said to be exposed to the substrate sequentially. In a spatial ALD process, different portions of the substrate surface, or material on the substrate surface, are exposed simultaneously to the two or more reactive compounds so that any given point on the substrate is substantially not exposed to more than one reactive compound simultaneously. As used in this specification and the appended claims, the term "substantially" used in this respect means, as will be understood by those skilled in the art, that there is the possibility that a small portion of the substrate may be exposed to multiple reactive gases simultaneously due to diffusion, and that the simultaneous exposure is unintended.

[0023] In one aspect of a time-domain ALD process, a first reactive gas (i.e., a first

precursor or compound A) is pulsed into the reaction zone followed by a first time-delay. Next, a second precursor or compound B is pulsed into the reaction zone followed by a second delay. During each time delay, a purge gas, such as argon, is introduced into the processing chamber to purge the reaction zone or otherwise remove any residual reactive compound or reaction by-products from the reaction zone. Alternatively, the purge gas may flow continuously throughout the deposition process so that only the purge gas flows during the time delay between pulses of reactive compounds. The reactive compounds are alternatively pulsed until a desired film or film thickness is formed on the substrate surface. In either scenario, the ALD process of pulsing compound A, purge gas, compound B and purge gas is a cycle. A cycle can start with either compound A or compound B and continue the respective order of the cycle until achieving a film with the predetermined thickness.

[0024] In an embodiment of a spatial ALD process, a first reactive gas and second reactive gas (e.g., nitrogen gas) are delivered simultaneously to the reaction zone but are separated by an inert gas curtain and/or a vacuum curtain. The substrate is moved relative to the gas delivery apparatus so that any given point on the substrate is exposed to the first reactive gas and the second reactive gas.

[0025] Transistors are circuit components or elements that are often formed on semiconductor devices. Depending upon the circuit design, in addition to capacitors, inductors, resistors, diodes, conductive lines, or other elements, transistors are formed on a semiconductor device. Generally, a transistor includes a gate formed between source and drain regions. In one or more embodiments, the source and drain regions include a doped region of a substrate and exhibit a doping profile suitable for a particular application. The gate is positioned over the channel region and includes a gate dielectric interposed between a gate electrode and the channel region in the substrate.

[0026] As used herein, the term "field effect transistor" or "FET" refers to a transistor that uses an electric field to control the electrical behavior of the device. Field effect transistors are voltage-controlled devices where their current carrying ability is changed by applying an electric field. Field effect transistors generally display very high input impedance at low temperatures. The conductivity between the drain and source terminals is controlled by an electric field in the device, which is generated

by a voltage difference between the body and the gate of the device. The FET's three terminals are source (S), through which the carriers enter the channel; drain (D), through which the carriers leave the channel; and gate (G), the terminal that modulates the channel conductivity. Conventionally, current entering the channel at the source (S) is designated IS and current entering the channel at the drain (D) is designated ID. Drain-to-source voltage is designated VDS. By applying voltage to gate (G), the current entering the channel at the drain (i.e., ID) can be controlled.

[0027] The metal–oxide–semiconductor field-effect transistor (MOSFET) is a type of field-effect transistor (FET) and is used in integrated circuits and high-speed switching applications. MOSFET has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage is used for amplifying or switching electronic signals. A MOSFET is based on the modulation of charge concentration by a metal–oxide–semiconductor (MOS) capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer. Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they are both of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a "+" sign after the type of doping.

[0028] If the MOSFET is an n-channel or nMOS FET, then the source and drain are n+ regions and the body is a p-type substrate region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are p+ regions and the body is a n-type substrate region. The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

[0029] A nMOS FET, is made up of an n-type source and drain and a p-type substrate. When a voltage is applied to the gate, holes in the body (p-type substrate) are driven away from the gate. This allows forming an n-type channel between the source and the drain and a current is carried by electrons from source to the drain through an induced n-type channel. Logic gates and other digital devices implemented using NMOSs are said to have NMOS logic. There are three modes of operation in a

NMOS called the cut-off, triode, and saturation. Circuits with NMOS logic gates dissipate static power when the circuit is idling, since DC current flows through the logic gate when the output is low.

[0030] A pMOS FET is made up of p-type source and drain and an n-type substrate. When a positive voltage is applied between the source and the gate (negative voltage between gate and source), a p-type channel is formed between the source and the drain with opposite polarities. A current is carried by holes from source to the drain through an induced p-type channel. A high voltage on the gate will cause a PMOS not to conduct, while a low voltage on the gate will cause it to conduct. Logic gates and other digital devices implemented using PMOS are said to have PMOS logic. PMOS technology is low cost and has a good noise immunity.

[0031] In an NMOS, carriers are electrons, while in a PMOS, carriers are holes. When a high voltage is applied to the gate, NMOS will conduct, while PMOS will not. Furthermore, when a low voltage is applied in the gate, NMOS will not conduct and PMOS will conduct. NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as holes, which are the carriers in PMOS. But PMOS devices are more immune to noise than NMOS devices. Furthermore, NMOS ICs would be smaller than PMOS ICs (that give the same functionality), since the NMOS can provide one-half of the impedance provided by a PMOS (which has the same geometry and operating conditions).

[0032] As used herein, the term "fin field-effect transistor (FinFET)" refers to a MOSFET transistor built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. FinFET devices have been given the generic name FinFETs because the source/drain region forms "fins" on the substrate. FinFET devices have fast switching times and high current density.

[0033] As used herein, the term "gate all-around (GAA)," is used to refer to an electronic device, e.g., a transistor, in which the gate material surrounds the channel region on all sides. The channel region of a GAA transistor may include nanowires or nano-slabs or nano-sheets, bar-shaped channels, or other suitable channel configurations known to one of skill in the art. In one or more embodiments, the channel region of a GAA device has multiple horizontal nanowires or horizontal bars

vertically spaced, making the GAA transistor a stacked horizontal gate-all-around (hGAA) transistor.

[0034] As used herein, the term "nanowire" refers to a nanostructure, with a diameter on the order of a nanometer (10^{-9} meters). Nanowires can also be defined as the ratio of the length to width being greater than 1000. Alternatively, nanowires can be defined as structures having a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Nanowires are used in transistors and some laser applications, and, in one or more embodiments, are made of semiconducting materials, metallic materials, insulating materials, superconducting materials, or molecular materials. In one or more embodiments, nanowires are used in transistors for logic CPU, GPU, MPU, and volatile (e.g., DRAM) and non-volatile (e.g., NAND) devices. As used herein, the term "nanosheet" refers to a two-dimensional nanostructure with a thickness in a scale ranging from about 0.1 nm to about 1000 nm, or from 0.5 nm to 500 nm, or from 0.5 nm to 100 nm, or from 1 nm to 500 nm, or from 1 nm to 100 nm, or from 1 nm to 50 nm.

[0035] Embodiments of the present disclosure advantageously provide semiconductor devices which, instead of having a p-metal directly on a high-k dielectric layer, include a barrier or depinning layer deposited to advantageously minimize flatband voltage (V_{fb}) rolloff. In one or more embodiments, the barrier or depinning layer can be an oxide, nitride, oxynitride, silicide, or selenide of metals. In one or more embodiments, the barrier or depinning layer can provide a mid-gap work function, e.g., about 4.4 to about 4.7 eV. The metal can comprise any suitable metal, including, but not limited to, aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), vanadium (V), niobium (Nb), ruthenium (Ru), antimony (Sb), and tin (Sn). In one or more embodiments, the addition of the barrier or depinning layer may advantageously increase the flatband voltage (V_{fb}) by more than 100 mV when compared to a PMOS stack that does not have a depinning layer.

[0036] The embodiments of the disclosure are described by way of the Figures, which illustrate devices (e.g., transistors) and processes for forming transistors in accordance with one or more embodiments of the disclosure. The processes shown are merely illustrative possible uses for the disclosed processes, and the skilled artisan will recognize that the disclosed processes are not limited to the illustrated

applications.

[0037] FIG. 1 illustrates a process flow diagram of a method 100 of manufacturing a semiconductor device in accordance with one or more embodiments of the present disclosure. With reference to FIG. 1, the method 100 begins at operation 102 by depositing an interfacial layer on a top surface of a channel located between a source and a drain on a substrate. At operation 104, a high-k dielectric layer is deposited on the interfacial layer. At operation 106, a depinning layer is deposited on the high-k dielectric layer. At operation 108, a P-metal layer is deposited on the depinning layer. At operation 110, the substrate is treated to neutralize charges in the interfacial layer or high-k dielectric layer and passivate oxygen vacancies.

[0038] FIGS. 2A-2E are cross-sectional views of a semiconductor device (e.g., a transistor such as a FinFET or GAA) 200 according to one or more embodiments. The semiconductor devices 200 shown in FIGS. 2A–2E may be manufactured by the method 100 illustrated in FIG. 1. In some embodiments, the semiconductor devices 200 are manufactured by method 100 illustrated in FIG. 1.

[0039] In one or more embodiments, the semiconductor device 200 comprises a semiconductor substrate 202 having a top surface 203. The semiconductor substrate 202 can be any suitable substrate material. In one or more embodiments, the semiconductor substrate 202 comprises a semiconductor material, e.g., silicon (Si), carbon (C), germanium (Ge), silicon germanium (SiGe), gallium arsenide (GaAs), indium phosphate (InP), indium gallium arsenide (InGaAs), indium aluminum arsenide (InAlAs), germanium (Ge), silicon germanium (SiGe), other semiconductor materials, or any combination thereof. In one or more embodiments, the semiconductor substrate 202 comprises one or more of silicon (Si), germanium (Ge), gallium (Ga), arsenic (As), indium (In), phosphorus (P), or selenium (Se). Although a few examples of materials from which the substrate 202 may be formed are described herein, any material that may serve as a foundation upon which passive and active electronic devices (e.g., transistors, memories, capacitors, inductors, resistors, switches, integrated circuits, amplifiers, optoelectronic devices, or any other electronic devices) may be built falls within the spirit and scope of the present disclosure.

[0040] In one or more embodiments, the semiconductor substrate 202 is a p-type or n-type substrate. As used herein, the term "n-type" refers to semiconductors that are

created by doping an intrinsic semiconductor with an electron donor element during manufacture. The term n-type comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. As used herein, the term "p-type" refers to the positive charge of a well (or hole). As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers.

[0041] In one or more embodiments, a source region 206a is on the top surface 203 of the semiconductor substrate 202. In one or more embodiments, the source region 206a has a source and a source contact (not illustrated). A drain region 206b is on the top surface 203 of the semiconductor substrate 202 opposite the source region 206a. In one or more embodiments, the drain region 206b has a drain and a drain contact (not illustrated).

[0042] In one or more embodiments, the source region 206a and/or the drain region 206b can be any suitable material known to the skilled artisan. In one or more embodiments, the source region 206a and/or the drain region 206b may have more than one layer. For example, the source region 206a and/or the drain region 206b may independently comprise three layers. In one or more embodiments, the source region 206a and the drain region 206b may independently comprise one or more of copper (Cu), cobalt (Co), tungsten (W), titanium (Ti), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), gold (Au), iridium (Ir), platinum (Pt), phosphorus (P), germanium (Ge), silicon (Si), aluminum (Al), or zirconium (Zr). In some embodiments, the source region 206a and the drain region 206b may independently comprise a bottom layer of silicon with doped epi (e.g., SiGe, SiP, and the like), a second layer of silicide, which may contain nickel (Ni), titanium (Ti), aluminum (Al), and the like, and a third, or top, layer which may be a metal such as, but not limited to, cobalt, tungsten, ruthenium, and the like. In some embodiments, the source region 206a and the drain region 206b may be raised source/drain regions formed by EPI growth.

[0043] In one or more embodiments, the source contact and/or the drain contact may independently be selected from one or more of nitrogen (N), copper (Cu), cobalt (Co), tungsten (W), titanium (Ti), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), gold (Au), iridium (Ir), tantalum (Ta), or platinum (Pt). In one or more

embodiments, formation of the source contact and/or the drain contact is conducted by any suitable process known to the skilled artisan, including, but not limited to ALD, CVD, PVD, MBE, MOCVD, spin-on, or other insulating layer deposition techniques known to the skilled artisan.

[0044] In one or more embodiments, a channel 204 is located between the source 204a and the drain 204b. In one or more embodiments, the channel 204 comprises silicon (Si).

[0045] In one or more embodiments, with reference to FIG. 1 and FIG. 2A, at operation 102, an interfacial layer 208 is deposited on a top surface 205 of the channel 204. In one or more embodiments, the interfacial layer 208 can be any suitable material known to the skilled artisan. For example, in one or more embodiments, the interfacial layer 208 comprises a dielectric material. In one or more embodiments, the dielectric material is selected from one or more of silicon (Si), silicon dioxide (SiO_2), silicon nitride (SiN), silicon oxynitride (SiON), silicon oxycarbide (SiOC), silicon carbon oxynitride (SiCONH), doped silicon, doped silicon oxide, doped silicon nitride, doped silicon oxynitride, spin-on dielectrics, or diffusion species growths. In one or more embodiments, the interfacial layer 208 comprises silicon dioxide (SiO_2). The interfacial layer 208 may be deposited using one or more deposition techniques known to one of ordinary skill in the art of semiconductor device manufacturing. In one or more embodiments, the interfacial layer 208 is deposited using one of deposition techniques, such as, but not limited to, ALD, CVD, PVD, MBE, MOCVD, spin-on, or other insulating layer deposition techniques known to the skilled artisan. In one or more embodiments, the interfacial layer 208 may be formed by etching and forming an oxide on the top surface 205 of the channel 204. In one or more embodiments, the interfacial layer 208 has a thickness in a range of 1 Å to 10 Å, or in a range of from 6 Å to 8 Å.

[0046] In one or more embodiments, a wet chemistry technique is performed to form the interfacial layer 208. The wet chemistry technique may be any technique known to the skilled artisan. In some embodiments, the wet chemistry technique includes a pre-clean process. In some embodiments, the pre-clean process includes using a solution comprising one or more of ozone, ammonium hydroxide or hydrogen peroxide. In some embodiments, the pre-clean process includes using a solution

without ozone, ammonium hydroxide or hydrogen peroxide. In some embodiments, after using the solution, the pre-clean process includes using dilute hydrofluoric acid (dilute HF) to etch away native oxide on the semiconductor substrate 202 to form a hydrophobic surface (i.e., the interfacial layer 208).

[0047] Referring to FIG. 1 and FIG. 2B, at operation 104, a high-κ dielectric layer 210 is formed on a top surface 207 of the interfacial layer 208. The high-κ dielectric layer 210 can be any suitable high-κ dielectric material known to the skilled artisan. In one or more embodiments, the high-κ dielectric layer 210 comprises one or more of hafnium oxide (HfOx), zirconium oxide (ZrOx), or hafnium zirconium oxide (HfZrOx). In one or more embodiments, the high-κ dielectric layer 210 is deposited using one of deposition techniques, such as, but not limited to, ALD, CVD, PVD, MBE, MOCVD, spin-on, or other insulating layer deposition techniques known to the skilled artisan. In one or more embodiments, the high-κ dielectric layer 210 has a thickness in a range of 5 Å to 25 Å, including in a range of from 5 Å to 20 Å, and a range of from 10 Å to 15 Å, including all subranges and values therebetween.

[0048] With reference to FIG. 1 and FIG. 2C, at operation 106, a depinning layer 212 is formed or deposited on a top surface 209 of the high-κ dielectric layer 210. In one or more embodiments, the depinning layer 212 advantageously minimizes flatband voltage (V_{fb}) rolloff at low equivalent oxide thickness (EOT). In one or more embodiments, the depinning layer 212 may provide a mid-gap work function, e.g., about 4.4 eV to about 4.7 eV.

[0049] In one or more embodiments, the depinning layer 212 may comprise any suitable material known to the skilled artisan. In some embodiments, the material for the depinning layer 212 is selected based on its affinity for oxygen (O_2). In one or more embodiments, the depinning layer 212 comprises a material that has a low affinity for oxygen in order to prevent or minimize oxygen gettering from the interfacial layer 208 or high-κ dielectric layer 210 and in order to potentially recover during anneal. In some embodiments, the depinning layer 212 enables oxygen (O_2), deuterium (D_2), and fluorine anneal to recover vacancies in the interfacial layer 208 or high-κ dielectric layer 210. In one or more embodiments, the depinning layer 212 has an effective work function (eWF) that is less than the P-metal layer 214.

[0050] The metal of the depinning layer 212 can comprise any suitable metal,

including, but not limited to, aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), vanadium (V), niobium (Nb), ruthenium (Ru), antimony (Sb), and tin (Sn). In one or more embodiments, the depinning layer 212 is selected from one or more of tantalum silicide (TaSix), tantalum silicon nitride (TaSiN), tantalum nitride (TaN), tantalum oxynitride (TaON), tantalum carbonitride (TaCN), titanium silicide (TiSix), titanium silicon nitride (TiSiN), titanium oxynitride (TiON), tungsten silicide (WSix), tungsten silicon nitride (WSiN), tungsten carbonitride (WCN), aluminum silicon nitride (AlSiN), aluminum nitride (AlN), selenium (Se), selenium nitride (SeN), graphene, titanium selenide (TiSe), titanium selenium nitride (TiSeN), and transition metal dichalcogenides. In one or more embodiments, the transition metal dichalcogenides are selected from one or more of molybdenum sulfide (MoS_2), molybdenum telluride ($MoTe_2$), molybdenum selenide (MoSe), tungsten sulfide (WS_2), tungsten telluride (WTe_2), and tungsten selenide (WSe).

[0051] In one or more embodiments, the depinning layer 212 may have any suitable thickness. In some embodiments, the depinning layer 212 has a thickness in a range of from >0 Å to 10 Å, including in a range of from 1 Å to 8 Å, or a range of from 1 Å to 5 Å.

[0052] In one or more embodiments, the depinning layer 212 may be deposited on the high-κ dielectric layer 210 by any suitable deposition technique known to the skilled artisan. In one or more embodiments, the depinning layer 212 is deposited using one of deposition techniques, such as, but not limited to, ALD, CVD, PVD, MBE, MOCVD, spin-on, radical assisted processes, or other deposition techniques known to the skilled artisan.

[0053] Referring to FIG. 1 and FIG. 2D, at operation 108, a p-metal layer 214 is deposited on a top surface 211 of the depinning layer 212. In one or more embodiments, the P-metal layer 214 is deposited using one of deposition techniques, such as, but not limited to, ALD, CVD, PVD, MBE, MOCVD, spin-on, or other insulating layer deposition techniques known to the skilled artisan. In one or more specific embodiments, the P-metal layer 214 is deposited by atomic layer deposition (ALD). In one or more embodiments, the P-metal layer 214 is deposited by atomic layer deposition (ALD) at a temperature in the range of about 200 °C to about 600 °C. In one or more embodiments, the P-metal layer 214 is deposited by atomic layer

deposition (ALD) at a temperature less than or equal to about 450 °C.

[0054] In one or more embodiments, the P-metal layer 214 may have any suitable thickness. In some embodiments, the P-metal layer 214 has a thickness in a range of >0 Å to 15 Å, or in a range of 1 Å to 10 Å. In one or more specific embodiments, the P-metal layer 214 has a thickness in a range of 10 Å to 20 Å.

[0055] In one or more embodiments, the P-metal layer 214 can comprise any suitable metal. In one or more embodiments, the P-metal layer 214 comprises a high work function metal or metal nitride. In some embodiments, doping more electronegative elements into a metal nitride, e.g., molybdenum nitride (MoN), titanium nitride (TiN), and the like, provides a P-metal layer 214 with the desired work function tunability without changing the thickness of the P-metal layer 214.

[0056] In one or more embodiments, the P-metal layer 214 comprises a metal selected from one or more of titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt), iridium (Ir), nickel (Ni), palladium (Pd), cobalt (Co), ruthenium (Ru), and molybdenum (Mo). In some embodiments, the P-metal layer 214 comprises one or more of titanium nitride (TiN), oxygen doped titanium nitride (O-doped TiN), selenium doped titanium nitride (Se doped-TiN), tellurium doped titanium nitride (Te-doped TiN), molybdenum nitride (MoN), carbon doped molybdenum nitride (C-doped MoN), selenium doped molybdenum nitride (Se-doped MoN), tellurium doped molybdenum nitride (Te-doped MoN), tungsten nitride (WN), carbon doped tungsten nitride (C-doped WN), selenium doped tungsten nitride (Se-doped WN), tellurium doped tungsten nitride (Te-doped WN), iridium nitride (IrN), selenium doped iridium nitride (Se-doped IrN), tellurium doped iridium nitride (Te-doped IrN), iridium oxide (IrO_2), iridium silicide ($IrSi_2$), ruthenium oxide (RuOx), ruthenium nitride (RuN), carbon doped tantalum nitride (C-doped TaN), selenium doped tantalum nitride (Se-doped TaN), tellurium doped tantalum nitride (Te-doped TaN), selenium (Se)-doped transition metals and their nitrides, and tellurium (Te)-doped transition metals and their nitrides, and the like.

[0057] Referring to FIG. 1 and FIG. 2E, at operation 110, in one or more embodiments, the method 100 includes one or more treatments to neutralize charges in the interfacial layer 208 or high-κ dielectric layer 210 and passivate oxygen vacancies. In one or more embodiments, the treatment may be used to control ambient atmosphere from interacting with the P-metal layer 214 and causing an

interaction on equivalent oxide thickness (EOT).

[0058] In one or more embodiments, the treatment of operation 110 includes the formation of a barrier layer 216 on a top surface 213 of the P-metal layer 214.

[0059] In one or more embodiments, the barrier layer 216 is deposited using one of deposition techniques, such as, but not limited to, ALD, CVD, PVD, MBE, MOCVD, spin-on, or other insulating layer deposition techniques known to the skilled artisan. In one or more specific embodiments, the barrier layer 216 is deposited by atomic layer deposition (ALD).

[0060] In one or more embodiments, the barrier layer 216 may have any suitable thickness. In some embodiments, the barrier layer 216 has a thickness in a range of 5 Å to 10 Å.

[0061] In one or more embodiments, the barrier layer 216 can comprise any suitable material. In one or more embodiments, the barrier layer 216 comprises one or more of titanium nitride (TiN), titanium nitride with amorphous silicon (TiN + a-Si), titanium silicon nitride (TiSiN), and amorphous silicon (a-Si).

[0062] In one or more embodiments, deposition of the barrier layer 216 on the P-metal layer 214 forms a PMOS stack 218 having a thickness in a range of from 20 Å to 35 Å, depending upon the device geometry.

[0063] Additional embodiments of the disclosure are directed to processing tools (i.e., a cluster tool) 900 for the formation of the logic/memory devices and methods described, as shown in FIG. 3. The cluster tool 900 includes at least one central transfer station 921, 931 with a plurality of sides. A robot 925, 935 is positioned within the central transfer station 921, 931 and is configured to move a robot blade and a wafer to each of the plurality of sides.

[0064] The cluster tool 900 comprises a plurality of processing chambers 902, 904, 906, 908, 910, 912, 914, 916, and 918, also referred to as process stations, connected to the central transfer station 921, 931. The various processing chambers provide separate processing regions isolated from adjacent process stations. The processing chamber can be any suitable chamber including, but not limited to, a preclean chamber, a buffer chamber, transfer space(s), a wafer orienter/degas chamber, a cryo cooling chamber, a deposition chamber, annealing chamber, etching chamber, a thermal processing (RTP) chamber, a plasma oxidation chamber, a

plasma nitridation chamber, and an atomic layer deposition (ALD) chamber. The particular arrangement of process chambers and components can be varied depending on the cluster tool and should not be taken as limiting the scope of the disclosure.

[0065] In one or more embodiments, a gate comprising one or more of a gate metal (not illustrated) or a gate contact (not illustrated) may optionally be formed or deposited on the exposed surface of the barrier layer 216. The gate metal may be any material known to one of skill in the art. In one or more embodiments, the gate metal comprises one or more of nitrogen (N), copper (Cu), cobalt (Co), tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), gold (Au), iridium (Ir), aluminum (Al), or platinum (Pt). In one or more specific embodiments, the gate metal comprises a metal selected from one or more of nitrogen (N), cobalt (Co), tungsten (W), titanium (Ti), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), iridium (Ir), aluminum (Al), or platinum (Pt). In other specific embodiments, the gate metal comprises a metal selected from one or more of nitrogen (N), cobalt (Co), tungsten (W), titanium (Ti), molybdenum (Mo), or ruthenium (Ru). In one or more embodiments, the gate contact may be any suitable material known to the skilled artisan. In one or more embodiments, the gate contact is selected from one or more of nitrogen (N), copper (Cu), cobalt (Co), tungsten (W), titanium (Ti), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), gold (Au), iridium (Ir), tantalum (Ta), aluminum (Al), or platinum (Pt).

[0066] In one or more embodiments, the cluster tool 900 includes an interfacial layer deposition chamber to deposit an interfacial layer, e.g., silicon dioxide (SiO_2). The interfacial layer deposition chamber of some embodiments comprises an atomic layer deposition chamber, a plasma enhanced atomic layer deposition chamber, or a spatial atomic layer deposition chamber. In one or more embodiments, the cluster tool 900 includes a pre-cleaning chamber connected to the central transfer station.

[0067] In the embodiment shown in FIG. 3, a factory interface 950 is connected to the front of the cluster tool 900. The factory interface 950 includes a loading chamber 954 and an unloading chamber 956 on a front 951 of the factory interface 950. While the loading chamber 954 is shown on the left and the unloading chamber 956 is shown on the right, those skilled in the art will understand that this is merely

representative of one possible configuration.

[0068] The size and shape of the loading chamber 954 and unloading chamber 956 can vary depending on, for example, the substrates being processed in the cluster tool 900. In the embodiment shown, the loading chamber 954 and unloading chamber 956 are sized to hold a wafer cassette with a plurality of wafers positioned within the cassette.

[0069] A robot 952 is within the factory interface 950 and can move between the loading chamber 954 and the unloading chamber 956. The robot 952 is capable of transferring a wafer from a cassette in the loading chamber 954 through the factory interface 950 to load lock chamber 960. The robot 952 is also capable of transferring a wafer from the load lock chamber 962 through the factory interface 950 to a cassette in the unloading chamber 956. As will be understood by those skilled in the art, the factory interface 950 can have more than one robot 952. For example, the factory interface 950 may have a first robot that transfers wafers between the loading chamber 954 and load lock chamber 960, and a second robot that transfers wafers between the load lock 962 and the unloading chamber 956.

[0070] The cluster tool 900 shown in FIG. 3 has a first section 920 and a second section 930. The first section 920 is connected to the factory interface 950 through load lock chambers 960, 962. The first section 920 includes a first transfer chamber 921 with at least one robot 925 positioned therein. The robot 925 is also referred to as a robotic wafer transport mechanism. The first transfer chamber 921 is centrally located with respect to the load lock chambers 960, 962, process chambers 902, 904, 916, 918, and buffer chambers 922, 924. The robot 925 of some embodiments is a multi-arm robot capable of independently moving more than one wafer at a time. In one or more embodiments, the first transfer chamber 921 comprises more than one robotic wafer transfer mechanism. The robot 925 in first transfer chamber 921 is configured to move wafers between the chambers around the first transfer chamber 921. Individual wafers are carried upon a wafer transport blade that is located at a distal end of the first robotic mechanism.

[0071] After processing a wafer in the first section 920, the wafer can be passed to the second section 930 through a pass-through chamber. For example, chambers 922, 924 can be uni-directional or bi-directional pass-through chambers. The pass-

through chambers 922, 924 can be used, for example, to cryo cool the wafer before processing in the second section 930 or to allow wafer cooling or post-processing before moving back to the first section 920.

[0072] A system controller 990 is in communication with the first robot 925, second robot 935, first plurality of processing chambers 902, 904, 916, 918 and second plurality of processing chambers 906, 908, 910, 912, 914. The system controller 990 can be any suitable component that can control the processing chambers and robots. For example, the system controller 990 can be a computer including a central processing unit, memory, suitable circuits, and storage.

[0073] Processes may generally be stored in the memory of the system controller 990 as a software routine that, when executed by the processor, causes the process chamber to perform processes of the present disclosure. The software routine may also be stored and/or executed by a second processor (not shown) that is remotely located from the hardware being controlled by the processor. Some or all of the methods of the present disclosure may also be performed in hardware. As such, the process may be implemented in software and executed using a computer system, in hardware as, e.g., an application specific integrated circuit or other type of hardware implementation, or as a combination of software and hardware. The software routine, when executed by the processor, transforms the general-purpose computer into a specific-purpose computer (controller) that controls the chamber operation such that the processes are performed.

[0074] Embodiments of the disclosure are directed to a non-transitory computer readable medium. In one or more embodiments, the non-transitory computer readable medium includes instructions that, when executed by a controller of a processing chamber, causes the processing chamber to perform the operations of any of the method 100 described herein. In one or more embodiments, the controller causes the processing chamber to perform the operations of method 100. In one or more embodiments, the controller causes the processing chamber to perform the operations of depositing an interfacial layer on a top surface of a channel located between a source and a drain on a substrate (operation 102), depositing a high-κ dielectric layer (operation 104) on the interfacial layer (operation 104), depositing a depinning layer (operation 106) on the high-κ dielectric layer, depositing a P-metal layer (operation

108) on the depinning layer, and depositing a barrier layer (operation 110) on the depinning layer.

[0075] In one or more embodiments, the processing tool 900 comprises a central transfer station 921, 931 comprising at least one robot 925, 935 configured to move a wafer; an atomic layer deposition (ALD) station connected to the central transfer station; an optional pre-clean station connected to the central transfer station; and at least one controller connected to the one or more of the central transfer station, the ALD station or the optional pre-clean station. In one or more embodiments, the at least one controller has at least one configuration selected from: a configuration to move the wafer between stations using the robot; a configuration to perform a deposition process; a configuration to deposit a depinning layer by atomic layer deposition; and a configuration to pre-clean the wafer.

[0076] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below," or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" may encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0077] The use of the terms "a" and "an" and "the" and similar referents in the context of describing the materials and methods discussed herein (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. Recitation of ranges of values herein are merely intended to serve as a shorthand method of referring individually to each separate value falling within the range, unless otherwise indicated herein, and each separate value is incorporated into the specification as if it were individually recited herein. All methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by

context. The use of any and all examples, or exemplary language (e.g., "such as") provided herein, is intended merely to better illuminate the materials and methods and does not pose a limitation on the scope unless otherwise claimed. No language in the specification should be construed as indicating any non-claimed element as essential to the practice of the disclosed materials and methods.

[0078] Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the disclosure. In one or more embodiments, the particular features, structures, materials, or characteristics are combined in any suitable manner.

[0079] Although the disclosure herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present disclosure. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present disclosure without departing from the spirit and scope of the disclosure. Thus, it is intended that the present disclosure includes modifications and variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising:

depositing an interfacial layer on a top surface of a channel located between a source and a drain on a substrate;

depositing a high-κ dielectric layer on the interfacial layer;

depositing a depinning layer on the high-κ dielectric layer;

depositing a P-metal layer on the depinning layer; and

depositing a barrier layer on the P-metal layer.

2. The method of claim 1, wherein the interfacial layer comprises a dielectric material.

3. The method of claim 2, wherein the dielectric material is selected from one or more of silicon (Si), silicon dioxide (SiO_2), doped silicon, doped silicon oxide, or spin-on dielectrics.

4. The method of claim 1, wherein the channel comprises silicon.

5. The method of claim 1, wherein the high-κ dielectric layer comprises one or more of hafnium oxide (HfOx), zirconium oxide (ZrOx), or hafnium zirconium (HfZr).

6. The method of claim 1, wherein the depinning layer comprises a metal selected from one or more of aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), vanadium (V), niobium (Nb), ruthenium (Ru), antimony (Sb), and tin (Sn).

7. The method of claim 6, wherein the depinning layer comprises one or more of tantalum silicide (TaSix), tantalum silicon nitride (TaSiN), tantalum nitride (TaN), tantalum oxynitride (TaON), tantalum carbonitride (TaCN), titanium silicide (TiSix), titanium silicon nitride (TiSiN), titanium oxynitride (TiON), tungsten silicide (WSix), tungsten silicon nitride (WSiN), tungsten carbonitride (WCN), aluminum silicon nitride (AlSiN), aluminum nitride (AlN), selenium (Se), selenium nitride (SeN), graphene,

titanium selenide (TiSe), titanium selenium nitride (TiSeN), and transition metal dichalcogenides.

8. The method of claim 7, wherein the transition metal dichalcogenides are selected from one or more of molybdenum sulfide (MoS_2), molybdenum telluride ($MoTe_2$), molybdenum selenide (MoSe), tungsten sulfide (WS_2), tungsten telluride (WTe_2), and tungsten selenide (WSe).

9. The method of claim 1, wherein the P-metal layer comprises a metal selected from one or more of titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt), iridium (Ir), nickel (Ni), palladium (Pd), cobalt (Co), ruthenium (Ru), and molybdenum (Mo).

10. The method of claim 9, wherein the P-metal layer comprises one or more of platinum (Pt), palladium (Pd), titanium nitride (TiN), oxygen doped titanium nitride (O-doped TiN), selenium doped titanium nitride (Se doped-TiN), tellurium doped titanium nitride (Te-doped TiN), molybdenum nitride (MoN), carbon doped molybdenum nitride (C-doped MoN), selenium doped molybdenum nitride (Se-doped MoN), tellurium doped molybdenum nitride (Te-doped MoN), tungsten nitride (WN), carbon doped tungsten nitride (C-doped WN), selenium doped tungsten nitride (Se-doped WN), tellurium doped tungsten nitride (Te-doped WN), iridium nitride (IrN), selenium doped iridium nitride (Se-doped IrN), tellurium doped iridium nitride (Te-doped IrN), iridium oxide (IrO_2), iridium silicide ($IrSi_2$), ruthenium oxide (RuOx), ruthenium nitride (RuN), carbon doped tantalum nitride (C-doped TaN), selenium doped tantalum nitride (Se-doped TaN), tellurium doped tantalum nitride (Te-doped TaN), and the like.

11. The method of claim 1, wherein the barrier layer comprises one or more of titanium nitride (TiN), titanium nitride with amorphous silicon (TiN + a-Si), titanium silicon nitride (TiSiN), and amorphous silicon (a-Si).

12. The method of claim 1, wherein the depinning layer, the P-metal layer, and the barrier layer have a combined thickness in a range of from 20 Å to 35 Å, depending upon the device geometry.

13. A method of manufacturing a semiconductor device, the method comprising:

depositing an interfacial layer on a top surface of a channel located between a source and a drain on a substrate;

depositing a high-κ dielectric layer on the interfacial layer;

depositing a depinning layer on the high-κ dielectric layer, the depinning layer a metal selected from one or more of aluminum (Al), tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), vanadium (V), niobium (Nb), ruthenium (Ru), antimony (Sb), and tin (Sn) and the depinning layer having a work function about 4.4 eV to about 4.7 eV;

depositing a P-metal layer on the depinning layer, the P-metal layer comprising a metal selected from one or more of titanium (Ti), tungsten (W), tantalum (Ta), platinum (Pt), iridium (Ir), nickel (Ni), palladium (Pd), cobalt (Co), ruthenium (Ru), and molybdenum (Mo); and

depositing a barrier layer on the P-metal layer.

14. The method of claim 13, wherein the depinning layer comprises one or more of tantalum silicide (TaSix), tantalum silicon nitride (TaSiN), tantalum nitride (TaN), tantalum oxynitride (TaON), tantalum carbonitride (TaCN), titanium silicide (TiSix), titanium silicon nitride (TiSiN), titanium oxynitride (TiON), tungsten silicide (WSix), tungsten silicon nitride (WSiN), tungsten carbonitride (WCN), aluminum silicon nitride (AlSiN), aluminum nitride (AlN), selenium (Se), selenium nitride (SeN), graphene, titanium selenide (TiSe), titanium selenium nitride (TiSeN), and transition metal dichalcogenides.

15. The method of claim 14, wherein the transition metal dichalcogenides are selected from one or more of molybdenum sulfide (MoS_2), molybdenum telluride ($MoTe_2$), molybdenum selenide (MoSe), tungsten sulfide (WS_2), tungsten telluride (WTe_2), and tungsten selenide (WSe).

16. The method of claim 13, wherein the P-metal layer comprises one or more of palladium (Pd), platinum (Pt), titanium nitride (TiN), oxygen doped titanium nitride (O-

doped TiN), selenium doped titanium nitride (Se doped-TiN), tellurium doped titanium nitride (Te-doped TiN), molybdenum nitride (MoN), carbon doped molybdenum nitride (C-doped MoN), selenium doped molybdenum nitride (Se-doped MoN), tellurium doped molybdenum nitride (Te-doped MoN), tungsten nitride (WN), carbon doped tungsten nitride (C-doped WN), selenium doped tungsten nitride (Se-doped WN), tellurium doped tungsten nitride (Te-doped WN), iridium nitride (IrN), selenium doped iridium nitride (Se-doped IrN), tellurium doped iridium nitride (Te-doped IrN), iridium oxide (IrO_2), iridium silicide ($IrSi_2$), ruthenium oxide (RuOx), ruthenium nitride (RuN), carbon doped tantalum nitride (C-doped TaN), selenium doped tantalum nitride (Se-doped TaN), tellurium doped tantalum nitride (Te-doped TaN), and the like.

17. The method of claim 13, wherein the barrier layer comprises one or more of titanium nitride (TiN), titanium nitride with amorphous silicon (TiN + a-Si), titanium silicon nitride (TiSiN), and amorphous silicon (a-Si).

18. The method of claim 13, wherein the depinning layer, the P-metal layer, and the barrier layer have a combined thickness of less than 25 Å.

19. The method of claim 13, further comprising depositing a gate metal on the barrier layer.

20. The method of claim 19, wherein the gate metal comprises one or more of nitrogen (N), copper (Cu), cobalt (Co), tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo), nickel (Ni), ruthenium (Ru), silver (Ag), gold (Au), iridium (Ir), aluminum (Al), and platinum (Pt).