SEMICONDUCTOR DEVICE COMPRISING A THIN OXIDE LINER AND METHOD OF MANUFACTURING THE SAME

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor devices, and more particularly, to the formation of doped regions in a semiconductor device.

BACKGROUND OF THE INVENTION

Over the last few decades, the semiconductor industry has undergone a revolution by the use of semiconductor technology to fabricate small, highly-integrated electronic devices, and the most common semiconductor technology presently used is silicon-based. A conventional process for preparing such a semiconductor device involves the deposition of a polysilicon gate layer over silicon substrate. The polysilicon gate layer is then etched to a desired width. The etching is performed anisotropically to provide substantially vertical sidewalls on the gate electrode.

Following the formation of the gate electrode, a source/drain extension implant is typically performed. The polysilicon gate electrode masks the substrate directly underneath the electrode, so that source/drain extensions are formed adjacent to the gate electrode.

After the source/drain extension implants, sidewall spacers are formed on the gate electrode. A deep source/drain implant process is then performed to create the source/drain regions. The sidewall spacers formed on the gate electrode act as masks to prevent the deep source/drain implants from being implanted into the substrate directly underneath the sidewall spacers. By this process, the deep source/drain regions are separated from the gate electrode by the width of the spacers. After the implantation processes are completed, an annealing step activates the implanted dopants.

The sidewall spacers are typically formed on the sidewalls on the gate electrode by etching of a dielectric layer such as silicon nitride that has been deposited over the substrate and the gate electrode. It is known to employ a liner oxide deposited prior to the primary dielectric layer to use as an etch stop layer during the etching of the silicon nitride sidewall spacers. The anisotropic etching of the dielectric layer etches the silicon nitride and stops on the liner oxide, preventing undesirable gouging of the silicon substrate. The liner oxide is typically deposited with a thickness of between 100 Å to 300Å, and most typically, 150 Å. A semiconductor device fabricated with this methodology is depicted in Figure 1. The semiconductor device includes a substrate 10, gate electrode 12, liner oxide 14, silicon nitride spacer 16, source/drain extensions 18 and deep source/drain regions 20.

A concern recognized by the inventors of such a configuration and methodology relates to the out-diffusion of dopants, especially from the source/drain extensions 18, into overlayers of the semiconductor device. The out-diffusion of the dopants results in higher resistance source/drains and

more graded junctions. Both of these problems degrade the transistor performance. The oxide layer 14, used as an etch stop layer during the etching of the silicon nitride sidewall spacers, acts as a sink for the dopants during the subsequent thermal processing. This allows the dopants to out-diffuse from the source/drain extensions 18 into the oxide liner 14. Hence, there is a concern regarding the provision of an etch stop layer to prevent gouging during the spacer etch, but that will not serve as a dopant sink for out-diffusion of dopants during thermal processing.

SUMMARY OF THE INVENTION

There is a need for an arrangement and method for making a semiconductor device the prevents out-diffusion of dopants to overlayers, but still provides adequate etch stopping capability to allow a sidewall spacer etch to be performed without gouging of the silicon substrate.

This and other needs are met by embodiments of the present invention which provide a method of forming a semiconductor device, comprising the steps of forming a gate electrode on a substrate, and forming an oxide liner less than 100 Å in thickness on the substrate and the gate electrode. A nitride layer is deposited on the oxide liner, and the nitride layer is etched to form nitride spacers, this etching stopping on the oxide liner.

The use of an oxide liner that is less than 100 Å in thickness suppresses out-diffusion of the dopants since that layer forms less of a sink for dopants and more dopants are retained in the substrate. In order to allow the oxide liner to still serve the function of etch stopping during the etching of the nitride layer, a very selective dry etch may be used, using CF_4 chemistries during the spacer formation, in certain preferred embodiments of the invention. The suppression of the out-diffusion of the dopants, especially in the source/drain extension regions, results in lower resistance source/drains and less graded junctions, thereby improving transistor performance.

The earlier stated needs are also met by embodiments of the present invention which provide a semiconductor device, comprising a substrate, a gate electrode on the substrate, and an oxide liner on the substrate. The oxide liner has a thickness of less than 100 Å. Nitride sidewall spacers are provided on the oxide liner.

The foregoing and other features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic, cross-sectional view of a semiconductor device constructed in accordance with prior art methodologies, illustrating the out-diffusion of dopants into overlayers.

Figure 2 depicts a semiconductor device manufactured in accordance with embodiments of the present invention, during one stage of manufacture.

Figure 3 depicts the structure of Figure 2, following the formation of an oxide liner in accordance with embodiments of the present invention.

Figure 4 shows the structure of Figure 3, after source/drain extension implants are performed, in accordance with embodiments of the present invention.

Figure 5 depicts the structure of Figure 4, after a dielectric layer has been deposited, in accordance with embodiments of the present invention.

Figure 6 shows the structure of Figure 5, following the etching of the dielectric layer to form sidewall spacers on the gate electrode, in accordance with embodiments of the present invention.

Figure 7 depicts the structure of Figure 6, after a deep source/drain implant has been performed to create source/drain regions of the semiconductor device, in accordance with embodiments of the present invention.

Figures 8a-8c depict the formation of a disposable spacer and an implant process employing the disposable spacer in accordance with embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention addresses and solves problems related to the out-diffusion of dopants into overlayers during thermal processing, resulting in higher resistance source/drain regions and more graded junctions, decreasing transistor performance. The present invention solves these problems, in part, by forming a semiconductor device with an oxide liner that is less than 100 Å in thickness on a substrate and a gate electrode. A nitride layer formed on the oxide liner is etched to form nitride spacers, this etching stopping on the oxide liner. During subsequent thermal processing, out-diffusion of the dopants that have been previously implanted are suppressed by the thinner oxide liner, which does not provide as a great a dopant sink as in the prior art. Hence, more dopant is retained in the substrate of the semiconductor device. This results in lower resistance source/drains, less graded junctions, and improved transistor performance.

Figure 2 shows the structure of a semiconductor device during one step of manufacturing. In this schematic depiction, a gate electrode 32, made up of polysilicon, for example, is formed on a substrate 30. The formation of the polysilicon gate electrode 32, or metal gate electrode, for example, is accomplished in a conventional manner, such as by deposition of a polysilicon gate layer over a silicon substrate, followed by photolithography and etching steps. A gate oxide (not shown) may also be provided between the substrate 30 and the polysilicon gate electrode 32, to create a gate dielectric.

As shown in Figure 3, following the formation of the gate electrode 32, an oxide liner 34 is deposited. A typical method of forming an oxide liner is through PECVD (plasma enhanced chemical vapor deposition) methods which are known to those of ordinary skill in the art. The oxide liner is deposited to a thickness of less than 100 Å, and between 20 and 70 Å in especially preferred

embodiments. In even further especially preferred embodiments, the thickness of the oxide liner is less than about 45 Å thick. The oxide liner 34 covers the gate electrode 32 and the surface of the substrate 30.

In Figure 4, a source/drain extension implant is performed in a conventional manner to create source/drain extensions 36 adjacent to the gate electrode 32. The gate electrode 32 masks the substrate 30 to prevent implantation of dopants directly underneath the gate electrode 32. Although Figures 3 and 4 depict one embodiment of the sequence of process steps in the present invention, in other embodiments, the steps of Figures 3 and 4 are reversed, so that the extension implant is performed prior to the deposition of the oxide liner 34.

In Figure 5, a dielectric layer, such as silicon nitride, for example, is deposited as a layer 38 over the oxide liner 34. The dielectric layer 38, may be deposited in a conventional manner, such as by CVD. Other materials may be used in the dielectric layer 38, provided such materials may be etched very selectively in comparison to oxide.

In Figure 6, the silicon nitride in the dielectric layer 38 has been etched to form sidewall spacers 40. It is critical for the oxide liner 34 to act as an etch stop to prevent gouging of the silicon substrate 30 during the nitride etch. Since the oxide liner 34 has been made thinner than in conventional prior art methods, care must be taken to avoid overetching. Accordingly, a highly selective dry etch is employed to form the sidewall spacers 40. The etch chemistry must exhibit high nitride-to-oxide selectivity so that the thin liner will serve as an adequate etch stop layer. An exemplary chemistry includes CF_4. Other etchant chemistries and recipes for etching, including plasma etching or reactive ion etching, include the following: $CF_4/HBr/HeO_2$ and $Cl_2/HBr/HeO_2$.

Figure 7 shows the structure of Figure 6 following the formation of source/drain regions 42 by a deep implant process and subsequent thermal processing. During the deep source/drain implantation, the sidewalls spacers 40 act as masks to prevent implantation of dopants in the substrate 30 directly underneath the sidewall spacers 40. Conventional dosages, implantation energies, and thermal annealing parameters may be employed.

During the thermal annealing, the thin oxide liner 34 suppresses the out-diffusion of the dopants in the source/drain extensions 36 and the source/drain regions 42, since the thinness of the oxide liner 34 substantially prevents the liner from acting as a sink for dopants. Hence, more dopants are retained in the substrate 30. The overall affect of this is to lower the resistance of the source/drain regions 42 and the source/drain extensions 36, and produce less graded junctions. This acts to improve the transistor performance.

In another aspect, a highly etch selective film for a disposable spacer process is provided. In this process, germanium oxide is employed as a disposable spacer material. Germanium oxide is preferred as it has the property of dissolving in water. The germanium oxide may be deposited by a sputter method, or by Ge CVD with subsequent oxidation. It is then anisotropically dry etched to

form a spacer. Figure 8a depicts an arrangement after germanium oxide spacers 50 have been deposited over a liner 52, made of oxide, nitride, or other material.

Disposable spacers may be used in different manners. An exemplary use is to perform deep source/drain implants 54 after the formation of the spacers, as depicted in Figure 8b. An anneal step is then performed that may be hotter than conventional, since the source/drain extension formed after spacer removal will not be subjected to the higher temperatures. The spacers 50 are then disposed of and an LDD implant 56 and lower temperature anneal is performed, as indicated in Figure 8c.

The germanium oxide is advantageous in that it can be removed very safely in water, and very selectively from other films traditionally used in semiconductor processing.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate (30);

a gate electrode (32) on the substrate (30);

an oxide liner (34) on the substrate (32), the oxide liner (34) having a thickness less than 100 Å; and

a nitride sidewall spacer (40) on the oxide liner (34).

2. The device of claim 1, further comprising source/drain extension implants (36) and source/drain regions (42) in the substrate (30).

3. The device of claim 2, wherein the oxide liner (34) is less than 45 Å thick.

4. A method of forming a semiconductor device, comprising the steps of:

forming a gate electrode (32) on a substrate (30);

forming an oxide liner (34) less than 100 Å in thickness on a substrate (30) and the gate electrode (32);

depositing a nitride layer (38) on the oxide liner (34); and

etching the nitride layer (38) to form nitride spacers (40), the etching stopping on the oxide liner (34).

5. The method of claim 4, wherein the step of etching the nitride layer (38) includes dry etching the nitride layer (38) with an etching chemistry with very high nitride-to-oxide selectivity.

6. A method of suppressing out-diffusion of dopants from implanted regions into overlayers of a semiconductor device, comprising the steps of:

implanting dopants into regions (36, 42) in a substrate (30); and

forming an oxide liner (34) less than 100 Å thick over the substrate (30).

7. The method of claim 6, further comprising forming a gate electrode (32) prior to the implanting of the dopants, and forming sidewall spacers (40) on the gate electrode (32) and oxide liner (34).

8. The method of claim 7, wherein the step of forming sidewall spacers (40) includes depositing a nitride layer (38) over the oxide liner (34) and the gate electrode (32), and dry etching the nitride layer (38) anisotropically with an etch receipt that has a high nitride-to-oxide selectivity.

9. The method of claim 8, wherein the etch recipe comprises at least one of $CF_4/HBr/HeO_2$ or $Cl_2/HBr/HeO_2$.

10. The method of claim 8, wherein the etch recipe comprises a CF_4 chemistry.