

1 CCD CHARGE SPLITTER

2 Field of the Invention

3 The field of the invention relates to charge coupled
4 devices and in particular to charge splitters implementing a 2
5 to 1 binary split.

6 Background of the Invention

7 Charge coupled devices (CCDs) (e.g., photodetectors,
8 analog to digital converters, signal processors, etc.) are known.
9 Such devices are used for accomplishing charge domain operations
10 such as charge packet transfer, summation, and splitting. CCDs
11 are useful in certain signal processing operations such as
12 decoding of radio frequency signals. For example, charge domain
13 filters have been constructed which provide finite impulse
14 response (FIR) filtering or infinite impulse response filtering
15 (IIR) filtering, often from within a single CCD device at very
16 low rates of power consumption.

17 Charge domain analog to digital (A/D) converters are
18 further examples of CCD devices that process signals in the
19 charge domain. Charge domain A/D converters, in fact, are often
20 used in conjunction with charge domain FIR or IIR filtering
21 devices because signals received by a radio frequency receiver
22 in the frequency domain are often more efficiently processed in
23 the charge domain before conversion to the digital domain within
24 the charge domain A/D converter.

25 One of the listed charge domain operations, charge
26 splitting, is of critical importance in charge domain analog to
27 digital (A/D) or digital analog (D/A) converters in that it is
28 used to implement fractional multiplication by binary weighting
29 (i.e., $\frac{1}{2}$) and therefore is one of the fundamental operations in
30 A/D and D/A converters. Charge splitting, as a consequence,
31 determines conversion accuracy, and therefore the converter

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1 characteristics, such as linearity, spurious response and
2 effective bits. Charge splitting serves a similar functionality
3 in charge domain finite impulse response (FIR) and infinite
4 impulse response (IIR) filters.

5 It has been suggested that charge splitting may be
6 accomplished by creating a field oxide barrier in a charge
7 transfer channel and clocking a charge packet into adjacent but
8 isolated reservoirs separated by the barrier. Such a suggestion
9 is based upon the assumption that charge distribution of the
10 charge packet in the charge channel passing the barrier is
11 uniform and reproducible. The suggestion is also based upon the
12 assumption that the barrier can be accurately located within the
13 charge channel and that the divided charges may then be later
14 removed from the isolated reservoirs without recombining the
15 previously divided charge.

16 Charge splitting error produced under the previously
17 suggested methods have ranged from as high as a few percent to
18 as little as a few tenths of a percent. Efforts aimed at
19 improving accuracy have included increasing the width of the
20 charge channel (to reduce the impact of an inaccurately placed
21 charge splitter) and placing dummy splitters in the charge
22 channel to compensate for nonlinearities caused by edge effects
23 and to equalize lateral forces applied to charge carriers.
24 Because of the importance of charge splitting in CCDs, a need
25 exists for a method of improving the accuracy of charge splitting
26 that is not dependent upon process parameters used in creating
27 the CCDs.

28 Summary of the Invention

29 It is an object of the invention to provide a charge
30 splitter that divides a charge packet into two equal charge
31 packets with improved accuracy over the prior art.

32 It is a further object of the invention to provide a
33 charge splitter that can be used in an iterative mode to achieve
34 varying levels of improved accuracy.

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1 It is a further object of the invention to provide a
2 charge splitter that can continuously process charge mode
3 signals.

4 These and other objects are provided by an apparatus
5 and method of equalizing a first and second charge. The
6 apparatus includes a charge splitter for splitting the first
7 charge packet into a third charge component on the first side of
8 the charge splitter and into a fourth charge component on the
9 second side of the charge splitter. The second charge packet is
10 split within the charge splitter into a fifth charge component
11 on the first side of the charge splitter and a sixth charge
12 component on the second side of the charge splitter. The
13 apparatus includes a combiner for adding the third component and
14 sixth component and the fourth and fifth components.

15 Description of the Drawings

16 FIG. 1 depicts a prior art charge splitter and charge
17 transfer gates;

18 FIG. 2 depicts a prior art charge transfer gate;

19 FIG. 3 is a time line diagram of charge transfer using
20 a four-phase clock;

21 FIG. 4 depicts a charge splitting system in accordance
22 with an embodiment of the invention;

23 FIG. 5 depicts a specific charge transfer system for
24 the charge splitting system of FIG. 4;

25 FIG. 6 depicts a particular type of charge transfer and
26 combining gate of FIG. 5;

27 FIG. 7 depicts a sequence of charge transfer states of
28 the apparatus of FIG. 5; and

29 FIG. 8 is an alternate charge transfer system for the
30 charge splitting system of FIG. 4.

31 Brief Description of a Preferred Embodiment

32 Under an embodiment of the invention, accurate charge
33 splitting is accomplished through an iterative charge splitting
34 process involving at least one charge splitter and a series of
35 charge transfer gates. To aid the reader in his understanding

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1 of the embodiment, an explanation will first be offered of charge
2 transfer and splitting. Following the explanation of charge
3 transfer and splitting, a novel process of splitting a charge
4 into two nominally equal components offering greatly improved
5 accuracy will be described in detail.

6 FIG. 1 shows a CCD charge splitter 10 and transfer
7 gates 20 in accordance with an embodiment of the invention.
8 Under the embodiment, a charge splitter 10 is comprised of a
9 charge splitting barrier gate 12, a splitter receiving well 14
10 and a field oxide charge-splitting barrier mechanism 16. (The
11 charge splitter 10 could also be fabricated through the use of
12 an overlapped polysilicon gate.) The charge transfer gates 20
13 may have a similar structure from one gate to the next and may
14 rely on a connection to a multi-phase (e.g., a 4-phase) clock for
15 proper operation.

16 FIG. 2 is a cross-section of a particular type of
17 transfer channel (i.e., an interline charge transfer channel) of
18 transfer gates 20 that may be used under the embodiment in
19 conjunction with the charge splitter 10. Under the embodiment,
20 the charge transfer channel (i.e., gates 20) and the charge
21 splitter 10 may be is fabricated using conventional CCD
22 technology. The CCD backside substrate 30 may be comprised of
23 a single carrier-type semiconductor material, such as P-type
24 crystalline silicon having a resistivity in the range of 0.01 to
25 0.02 ohm-centimeter (Ω -cm). A P-type epitaxial layer 32 may be
26 grown on the heavily-doped backside substrate 30. The epitaxial
27 layer 32 may have a resistivity in the range of from 30-40 Ω -cm.
28 Both the backside substrate 30 and the epitaxial layer 32 will
29 be generally referred to as the substrate.

30 A buried channel implant 34, formed by diffusing a
31 light doping of an opposite carrier-type material (shown as N-)
32 into the (P-type) silicon substrate, extends below the surface
33 of the semiconductor. A threshold adjust implant 36 is formed
34 by diffusing a light doping of the same type (P-type) material
35 (shown as P-) into the substrate after the buried channel implant
36 34 has been formed. A silicon-dioxide dielectric layer 38 is
37 then grown on the semiconductor surface before the CCD

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1 polysilicon gates 22, 24, 26, 28, 30 are applied. Finally,
2 metalization (not shown) for the clock lines is applied and
3 connected to the polysilicon gates via contacts as is well known
4 in the art.

5 The charge splitter 10 may be fabricated in a similar
6 manner except for the addition of the charge splitting barrier
7 16 and metalization. The barrier 16 is fabricated by depositing
8 a field oxide barrier over the epitaxial layer 32 in the area
9 defining the barrier 16 before the implant 34 occurs. Placing
10 the field oxide barrier over the epitaxial layer 32 results in
11 a longitudinal separation (i.e., the field oxide barrier 16) in
12 the charge transfer channel.

13 The polysilicon gates of the charge splitter 10 is also
14 longitudinally divided to provide an A and B clock connections.
15 The A and B clock connections allow charge packets on each side
16 A, B of the barrier 16 to be independently controlled.

17 Charge transfer within the gates 20 of the charge
18 transfer channel occurs under control of the multi-phase clock.
19 Where unidirectional charge transfer is required by the process,
20 a two-phase clock ϕ_1 , ϕ_2 as shown in FIG. 2 may be used. Where
21 bidirectional charge transfer is necessary a four-phase clock
22 would typically be used.

23 For the charge transfer channel 20 of FIG. 2 a two-
24 phase clock would typically be used. When a first phase ϕ_1 is
25 high +V, a charge packet Q (entering the channel 20 from the
26 left) is attracted to and held in a first potential well 31 under
27 the first gate 30. On the next clock pulse, the first clock
28 signal ϕ_1 goes low 0V and the second clock phase ϕ_2 goes high +V.
29 The charge packet Q, in response, flows to the next potential
30 well 33 under a next gate 22 and so on from left to right in FIG.
31 2, or from top to bottom in FIG. 1.

32 FIG. 3 is a time-line diagram of a four-phase charge
33 transfer channel. Using a four-phase clock, the adjacent clock
34 connections of FIG. 2 would be interconnected as shown in FIGS.
35 3b-3e with a four-phase clock and clocked with the signals shown
36 in FIG. 3a. The threshold implant 36 is also not present with
37 four-phase clocking.

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1 At time t_1 , clock signals ϕ_1 and ϕ_2 are high, such that
2 a potential well 40 is formed for storage of charge 42 under the
3 first two gates. At time t_2 , clock signal ϕ_1 has gone low and
4 clock signal ϕ_3 has gone high, such that the change in the
5 potential well 40 has shifted the charge packet 42 to the right
6 as shown. At time t_3 and t_4 , the charge packet is shifted
7 further to the right in a similar manner. It should be noted
8 that while the illustrated example shows the charge packet 42
9 being shifted from the left to right, the direction of movement
10 of the charge packet 42 could be changed at any time by a
11 reversal of the phasing of the clock signals ϕ_1 - ϕ_4 .

12 Each side A, B of the charge splitter 10 of FIG. 1 has
13 an independently controllable clock input signal ϕ_A , ϕ_B . Where
14 ϕ_A , ϕ_B are clocked together (with the same magnitude and phase)
15 the splitter 10 performs substantially the same as any other
16 charge transfer gate 20. Where either clock signal ϕ_A , ϕ_B is
17 held at a high level any charge entering the charge splitter 10
18 will be held on that side A, B of the charge splitter 10.

19 Where a four-phase clock is used, a charge transfer
20 gate 20 will be assumed to be made up of gates 22, 24, 26, 28
21 with the first phase ϕ_1 connected to the first gate 22, the
22 second phase ϕ_2 connected to the second gate 24, and so on. If
23 a two phase clock were used, gates 22 and 24 would make up a
24 first charge transfer gate 20 and gates 26 and 28 would make up
25 a second gate 20.

26 Due to mutual charge repulsion, the charge will be
27 uniformly distributed throughout the input gate 28. The charge
28 Q is held within the transfer gate 28 by the high state of the
29 gate's clock signal.

30 At the appropriate instant, the gate signals ϕ_A , ϕ_B of
31 the charge splitter 10 are both activated (while the gate signal
32 of the input gate 28 is deactivated) to draw the charge Q from
33 the input gate 28 into the charge splitter 10. Because of the
34 characteristics of the splitter 10, part of the charge determined
35 by the splitting ratio (e.g., $Q_A=1/3$) will reside in the A-well
36 and the remainder (e.g., $Q_B=2/3$) will reside in the B-well.

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1 It has been determined that the accuracy of charge
2 splitting can be improved significantly through the use of
3 multiple charge splits. Under an embodiment of the invention,
4 the improved charge splitting process can be iterative (i.e.,
5 through use of a single charge splitter have a splitting ratio
6 A:B) or the process may be pipelined through a number of
7 splitters (i.e., through a first charge splitter having an A:B
8 splitting ratio, a second splitter have a C:D ratio, a third
9 splitter having a ratio E:F, etc.).

10 Where pipeline charge splitting is used, the result of
11 the first split produces charge components A and B. The result
12 of the second charge split (first splitting A and then B and
13 combining) is $AD+BC$ and $AC+BD$. The result of the third charge
14 split is $E(AC+BD)+F(AD+BC)$ and $F(AC+BD)+E(AD+BC)$.

15 Where iterative charge splitting is used (i.e., using
16 a single charge splitter have a splitting ratio of A:B) the
17 pipelined result can be simplified to a third charge split result
18 of $A(AA+BB)+B(AB+BA)$ and $B(AA+BB)+A(AB+BA)$, since $A=C=E$ and
19 $B=D=F$.

20 Turning now to FIG. 4 a simplified charge splitter
21 system 50 is shown in accordance with an embodiment of the
22 invention. The charge splitter system 50 includes a charge
23 splitter 10, an input transfer gate 52 and an output transfer
24 gate 54. The charge splitter 10 is assumed to have some unequal
25 splitting ratio A:B (e.g., 1:2) that is characteristic of the
26 splitter's fabrication. This charge splitter 10 is intended to
27 divide an input charge packet into two equal size output packets,
28 but in practice the splitting ratio of an individual splitter 10
29 will depart from the desired 1:1 ratio by a small amount that is
30 characteristic of the splitter's fabrication. The splitter 50
31 is assumed to receive an input charge Q and to output two charge
32 packets Q_A and Q_B . The splitter 10 of FIG. 4 is assumed to be
33 the same as the splitter 10 of FIG. 1 except that the splitter
34 10 of FIG. 4 may be assumed to have a splitter barrier gate 12
35 on each side of the splitter receiving well 14.

36 For the sake of simplicity, the charge Q will be
37 assumed to have an idealized value of 1 and that the sum of the

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1 charge accumulating on each side of the splitter, when added
2 together, equals Q . A and B will be assumed to have a fractional
3 value consistent with the splitting ratio. Also, since $AQ+BQ=Q$,
4 $AQ=Q_A=A$, and $BQ=Q_B=B$, the letters A and B will be used to refer
5 to the charge packets after the first splitting operation as well
6 as to the splitting fractions, as appropriate.

7 Under the embodiment, the charge packets are passed
8 through the splitter 10 a number of times to reduce the net
9 error. For purposes of discussion, the error in the splitting
10 ratio will be exaggerated (e.g., $A=1/3$, $B=2/3$) instead of ideal
11 (i.e., $A=B=1/2$). Table I shows results of charge splitting under
12 the embodiment. On the left side is shown the iteration number.
13 The right side shows the error of each successive iteration under
14 the embodiment.

15 Under the embodiment, the charge packet Q is
16 transferred into the charge splitter system 50 from the left into
17 the charge transfer gate 52. The gate signals ϕ_A , ϕ_B are both
18 activated to draw the charge Q from the input gate 52 into the
19 charge splitter 10.

20 On the next clock cycle, the charge in the A-well 56
21 (i.e., Q_A) is clocked into the next charge transfer gate 54 while
22 the other charge (i.e., Q_B) remaining in the B-well 58. Q_A is
23 clocked out of the A-well by causing the clock signal ϕ_y to go
24 high while the clock signal ϕ_A of the A-well is caused to go low.
25 Q_A may then be retained in another transfer gate (not shown in
26 FIG. 4) for subsequent iterative splitting operations.

27 The Q_B charge held in the B-well 58 is retained in the
28 B-well by maintaining the clock signal ϕ_B high on that side of
29 the splitter 10. During a subsequent clock cycle, the charge Q_B
30 in the B-well is shifted out on the next iterative cycle.

31 As shown in Table I and at the end of the first
32 splitting operation, Q_A has a value equal to A (which for the
33 example given, equals $1/3$). Q_B has a value equal to B (i.e.,
34 $2/3$). The error (since the goal is a 50-50 split) is 17%.

35 During a second iterative cycle the two charge packets
36 Q_A , Q_B are again divided. The results are then added to reduce
37 the overall error.

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The first charge packet Q_A (hereinafter referred to as "A") is again split in a second splitting operation, the result of which can be characterized by multiplying the first charge packet A by the two splitting ratios A, B to produce two smaller charge packets AA and AB. Similarly the second charge packet Q_B (hereinafter referred to as "B") is split in a third splitting operation (multiplied by the two splitting ratios) to produce two smaller charge packets AB and BB.

The AA charge packet of the second splitting operation is added to the BB charge packet of the third splitting operation to produce a new Q_A value AA+BB (i.e., $1/3 \times 1/3 + 2/3 \times 2/3 = 5/9$) assuming A=1/3 and B=2/3. Similarly the AB charge packet of the second split is added to the BA charge packet of the third split to produce a new Q_B value AB+BA (i.e., $1/3 \times 2/3 + 2/3 \times 1/3 = 4/9$). The error of this split (i.e., $5/9 - 4/9$ or $1/9$) is now 5.5% as shown in Table I.

Where the first charge packet Q_A (i.e., AA+BB) is again passed through the charge splitter 50, the result of the fourth split is A(AA+BB) and B(AA+BB). Similarly the second charge packet Q_B (i.e., AB+BA) is put through the charge splitter 50 for a fifth split to produce results of A(AB+BA) and B(AB+BA).

As before the opposing elements of the fourth and fifth splits (i.e., A(AA+BB) and B(AB+BA)) are added together to form a new first charge packet Q_A . Likewise, the opposing elements of the fourth and fifth splits (i.e., B(AA+BB) and A(AB+BA)) are added together to form a new second charge packet Q_B . The error of this split is now 1.85% as shown in Table I.

Table I

<u>Iteration No.</u>	<u>QA</u>	<u>QB</u>	<u>Error</u>
1	A	B	17%
2	AA+BB	AB+BA	5.5%
3	A(AA+BB)+B(AB+BA)	B(AA+BB)+A(AB+BA)	1.85%

For the example offered above, the splitting ratio was assumed to be 1:2. A more practical example, however, is the case where the splitting error were to be less than 1%. For the

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1 example shown above for an first splitting error or 1%, a second
2 splitting error would be 0.02%. A third splitting error would
3 be 0.0004%.

4 In the case where the splitting ratio is 0.5%, a second
5 splitting error would be 0.005%. A third splitting error would
6 be 0.00005%.

7 Implicit in the above-example is that the iterative
8 process could be extended to any number of steps. The number of
9 steps required for any given application must be determined by
10 the accuracy required.

11 FIG. 5 depicts a practical example of an iterative
12 charge splitting device 70 in accordance with an embodiment of
13 the invention. The charge splitter device 70 is a CCD device
14 containing a splitter 10 and a number of transfer gates 20. The
15 splitting device 70 also includes a charge storage well 60 and
16 an input/output (I/O) gate 62. The storage well 60 is
17 constructed by locating a receiving well between two barrier
18 gates as is well known in the art.

19 The I/O gate 62 is a gate similar to those shown in
20 FIG. 1 but capable of receiving (and combining) charges from
21 transfer gates 20 to the left and right of the I/O gate 62. The
22 I/O gate 62 is also constructed to transfer charge into the
23 charge splitter 10 or to receive an input charge from an external
24 source (not shown) or to output a charge, as appropriate. The
25 I/O gate 62 may be constructed as shown in FIG. 6 as a charge
26 well 64 surrounded by a series of barrier gates 66 all as well
27 known in the art.

28 FIG. 7 depicts the charge splitting device 70 during
29 two of the three previously described iterative charge splitting
30 operations. The seven depicted steps show the initial charge
31 split as well as the subsequent splitting of the initially split
32 charges and combining of opposing elements to provide an interim
33 result for the example provided above.

34 As shown in FIG. 7, for the first step (labeled "1"),
35 a charge is input from an external device (not shown). In the
36 second step the first charge packet "a" is transferred back to
37 the splitter 10 along a circular path going clockwise to the left

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1 while the second charge packet "b" is held in the charge well 60
2 for a sufficient number of clock cycles to allow the first charge
3 packet "a" to reach in the I/O gate 62 in advance of the second
4 charge packet "b".

5 In the third step of FIG. 7, the first charge packet
6 "a" has returned to the charge splitter 10 and is divided into
7 charge components "aa" and "ab". In the third step of FIG. 7,
8 the charge component "ab" is not transferred into the charge well
9 60 but is instead routed to the bottom of the charge transfer
10 path shown in the bottom right of FIGs. 5 and 7.

11 Step 4 of FIG. 7 shows the second charge packet "b"
12 being split within the charge splitter 10 (shown as components
13 "ba" and "bb" in Step 5). Step 4 of FIG. 7 also shows the charge
14 packet "aa" being transferred back to the I/O gate 62 along the
15 circular charge transfer path on the left side.

16 After splitting the second charge packet "b" the split
17 packet "bb" is transferred through the charge well 60 without
18 delay (step 5) so as to ensure that the split packet "bb" arrives
19 (step 6) at the I/O gate 62 at the same instant as the split
20 component "aa" of the first charge packet "a".

21 As the two opposing packets "aa" and "bb" reach the I/O
22 gate 62 they are combined within the I/O gate 62. The combined
23 packets "aa" and "bb" may then be output or the process can be
24 repeated.

25 It is to be understood that the iterative charge
26 splitting process shown in FIG. 7 (using the iterative charge
27 splitting device of FIG. 6) could be terminated after the two
28 iterative charge splitting operations shown (and the resultant
29 packets provided as outputs) or the iterative process may be
30 continued as in the first example. Where the process is to be
31 continued, the iterative process of the embodiment may be
32 continued to achieve degrees of charge splitting accuracy not
33 available with prior charge splitting devices.

34 Under another embodiment of the invention, iterative
35 charge splitting is accomplished in-line using a number of charge
36 splitting devices 10. Under the embodiment, charge splitters 10,
37 charge transfer gates 20, charge combiners 62, and charge storage

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1 wells 60 are combined to provide a charge splitting CCD device
2 80 (FIG. 8) of high accuracy and speed.

3 Under the embodiment, a charge Q enters from the left
4 (FIG. 8) and is split into charge packets "a" and "b" (the a
5 packet and b packet) within a first charge splitter 10. The a
6 packet is transferred to second charge splitter 10 (having a c:d
7 charge splitting ratio) while the b packet is transferred to and
8 held in a charge storage well 60.

9 In the second charge splitter 10 the a packet is split
10 into packets "ac" and "ad" (herein after the ac packet and ad
11 packet). The ac packet enters a second charge well 60. The ad
12 packet is shifted into a third charge well 60.

13 After splitting the a packet, the b packet is shifted
14 out of the charge well 60 and split in the second (c:d) charge
15 splitter to form a bc packet and a bd packet. The bd charge
16 packet is transferred to where the ac charge packet was
17 previously stored in an adjacent charge well 60 and combined with
18 the ac packet in the charge combiner 62. The sum (i.e., $ac+bd$)
19 is transferred to and split within the third charge splitter 10
20 (having a ratio of e:f). The results (i.e., $e(ac+bd)$ and
21 $f(ac+bd)$) are stored in charge wells 60.

22 The bc packet split in the second charge splitter 10
23 is transferred to the charge combiner 62 adjacent the ad packet
24 and combined with the ad packet. The sum (i.e., $ad+bc$) arrives
25 at the third splitter 10 after (because it had a longer path to
26 travel) the previous sum ($ac+b$). The $ad+bc$ packet is split
27 within the third splitter to produce the charge packets $e(ad+bc)$
28 and $f(ad+bc)$. The $f(ad+bc)$ packet is shifted along the charge
29 transfer channel until it is opposite the $e(ac+b)$ packet stored
30 in a charge well 60. The $f(ad+bc)$ and $e(ac+bd)$ are combined in
31 the charge combiner 62 and transferred to an output gate 20.
32 Similarly the $e(ad+bc)$ packet is transferred to the gate opposite
33 the $f(ac+bd)$ packet and combined with the $f(ac+bd)$ packet.

34 In another embodiment of the invention, charge
35 splitting is used to create precisely proportional charger
36 packets by splitting and combining unequal portions. For
37 example, a charge packet having a value of 1 could be iteratively

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1 split to provide precise packets of $1/2$ and $1/2$. One of the
2 packets could, again, be iteratively split to produce packets of
3 $1/4$ and $1/4$. One of the products of the second split, $1/4$ could
4 be added to the remaining product of the first split, $1/2$, to
5 produce a total packet value of $3/4$. The result is a precisely
6 proportioned 3:1 charge division. In a similar manner the
7 process could be continued to produce any desired proportion.

8 A specific embodiment of novel methods and apparatus
9 of dividing charge packets within charge coupled devices
10 according to the present invention have been described for the
11 purpose of illustrating the manner in which the invention is made
12 and used. It should be understood that the implementation of
13 other variations and modifications of the invention and its
14 various aspects will be apparent to one skilled in the art, and
15 that the invention is not limited by the specific embodiments
16 described. Therefore, it is contemplated to cover the present
17 invention any and all modifications, variations, or equivalents
18 that fall within the true spirit and scope of the basic
19 underlying principles disclosed and claimed herein.

What is claimed is:

1 1. Apparatus for equalizing a first and a second
2 charge packet comprising :

3 a) a charge splitter for splitting the first
4 charge packet into a third charge packet on a first side of the
5 charge splitter and a fourth charge packet on a second side of
6 the charge splitter and for splitting the second charge packet
7 into a fifth charge packet on the first side of the charge
8 splitter and a sixth charge packet on the second side of the
9 charge splitter; and

10 b) a charge combiner for adding the third and
11 sixth charge packets and the fourth and fifth charge packets.

1 2. The method of claim 1 further comprising means for
2 iteratively repeating the equalization process.

1 3. The apparatus as in claim 1 further comprising a
2 second charge splitter for splitting the second charge packet
3 into fifth and sixth charge packets.

1 4. A method of equalizing a first and a second charge
2 packet within a charge splitter comprising the steps of:

3 a) splitting the first charge packet into a
4 third charge packet on a first side of the charge splitter and
5 a fourth charge packet on a second side of the charge splitter;

6 b) splitting the second charge packet into a
7 fifth charge packet on the first side of the charge splitter and
8 a sixth charge packet on the second side of the charge splitter;
9 and

10 c) adding the third and sixth charge packets and
11 the fourth and fifth charge packets.

1 5. The method of claim 4 further comprising the step
2 of repeating the process iteratively.

1 6. A method of splitting a charge within a charge
2 coupled device comprising the steps of:

3 a) splitting the charge into a first charge
4 component on a first side of a charge splitter and a second
5 charge component on a second side of the charge splitter;

6 b) splitting the first charge component into a
7 third charge component on the first side of the charge splitter



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8 and into a fourth charge component on the second side of the
9 charge splitter;

10 c) splitting the second charge component into
11 a fifth charge component on the first side of the charge splitter
12 and a sixth charge component on the second side of the charge
13 splitter;

14 d) adding the third component and sixth
15 component to produce a first split charge and the fourth and
16 fifth components to produce a second split charge; and

17 e) outputting the first and second split
18 charges.

1 7. The method as in claim 6 further comprising the
2 steps of repeating steps b through d an at least second time
3 using the first split charge as the first component and the
4 second split charge as the second component.

1 8. The method as in claim 6 further comprising the
2 step of using an at least second charge splitter to split the
3 first and second charge components.

1 9. A charge coupled device for splitting a charge
2 comprising:

3 a) a first charge splitter for splitting the
4 charge into first and second charge components;

5 b) a second charge splitter having first and
6 second sides for splitting the first charge component into a
7 third charge component on the first side of the second charge
8 splitter and into a fourth charge component on the second side
9 of the charge splitter;

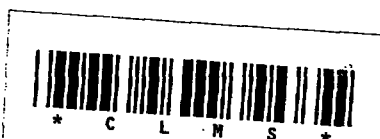
10 c) a third charge splitter having first and
11 second sides for splitting the second charge component into a
12 fifth charge component on the first side of the third charge
13 splitter and a sixth charge component on the second side of the
14 third charge splitter;

15 d) a charge adder for adding the third component
16 and sixth component to produce a first split charge and the
17 fourth and fifth components to produce a second split charge; and

18 e) a transfer channel for outputting the first
19 and second split charges.

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1 10. The charge coupled device as in claim 9 further
2 comprising a fourth charge splitter having first and second sides
3 for splitting the first split charge into a seventh charge
4 component from the first side of the fourth charge splitter and
5 into a eighth charge component from the second side of the fourth
6 charge splitter.

1 11. The charge coupled device as in claim 10 further
2 comprising a fifth charge splitter having first and second sides
3 for splitting the second split charge into a ninth charge
4 component from the first side of the fourth charge splitter and
5 into a tenth charge component from the second side of the fourth
6 charge splitter.

1 12. The charge coupled device as in claim 11 further
2 comprising a second charge adder for adding the seventh and tenth
3 charge component to produce a third split charge and the eighth
4 and ninth components to produce a fourth split charge.

1 13. The charge coupled device as in claim 11 further
2 comprising a second charge adder for adding the seventh component
3 and ninth component to produce the first split charge and the
4 eighth and tenth components to produce the second split charge.

1 14. The charge coupled device as in claim 9 wherein
2 the charge splitter further comprises a field oxide barrier
3 dividing a charge transfer channel.

1 15. A method of charge splitting in a charge coupled
2 device comprising the steps of:

3 a) splitting the charge within a charge splitter
4 having a first and second side into first and second charge
5 components;

6 b) splitting the first charge component into a
7 third charge component on the first side of the charge splitter
8 and a fourth charge component on the second side of the charge
9 splitter;

10 c) splitting the second charge component into
11 a fifth charge component on the first side of the charge splitter
12 and a sixth charge component on the second side of the charge
13 splitter;

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14 d) adding the third component and sixth
15 component to produce a first split charge and the fourth and
16 fifth components to produce a second split charge; and

17 e) outputting the first and second split charges
18 as a charge splitter output.

1 16. The method as in claim 15 further comprising the
2 step of transferring the first and second charge components out
3 of the charge splitter.

1 17. The method as in claim 16 further comprising the
2 step of transferring the first charge component back to the
3 charge splitter.

1 18. The method as in claim 16 further comprising the
2 step of transferring the second charge component back to the
3 charge splitter.

1 19. The method as in claim 15 further comprising the
2 steps of repeating steps b through d and at least second time
3 using the first split charge as a first charge component and the
4 second split charge as the second charge component.

1 20. A method of charge splitting in a charge coupled
2 device comprising the steps of:

3 splitting the charge within a charge splitter
4 having a first and second side into first and second charge
5 components;

6 transferring the first and second charge
7 components out of the charge splitter;

8 transferring the first charge component back to
9 the charge splitter and splitting the first charge component into
10 a third charge component on the first side of the charge splitter
11 and a fourth charge component on the second side of the charge
12 splitter;

13 transferring the second charge component back to
14 the charge splitter and splitting the second charge component
15 into a fifth charge component on the first side of the charge
16 splitter and a sixth charge component on the second side of the
17 charge splitter;



18 adding the third component and sixth component to
19 produce a first split charge and the fourth and fifth components
20 to produce a second split charge; and

21 outputting the first and second split charges as
22 a charge splitter output.

1 21. A charge coupled device for splitting a charge
2 packet comprising:

3 a charge splitter having first and second sides
4 for splitting the charge into first and second charge components;

5 a first charge transfer channel for transferring
6 the first and second charge components out of the charge
7 splitter;

8 a second charge transfer channel for transferring
9 the first charge component back to the charge splitter and
10 splitting the first charge component into a third charge
11 component on the first side of the charge splitter and a fourth
12 charge component on the second side of the charge splitter;

13 a third charge transfer channel for transferring
14 the second charge component back to the charge splitter and
15 splitting the second charge component into a fifth charge
16 component on the first side of the charge splitter and a sixth
17 charge component on the second side of the charge splitter;

18 an adder for adding the third component and sixth
19 component to produce a first split charge and the fourth and
20 fifth components to produce a second split charge; and

21 an output buffer for outputting the first and
22 second split charges as a charge splitter output.

1 22. The charge coupled device as in claim 20 wherein
2 the charge splitter further comprises a field oxide barrier
3 dividing a charge transfer channel.