

ABSTRACT

CLOCK RECOVERY METHOD BY PHASE SELECTION

The present invention demonstrates a method and circuit where a plurality of phase clocks from a “frequency lock only” PLL are used to sample an input clock CLKIN. This results in a series of signals from which the phase clock most in synchronization with CLKIN can be determined and presented to the output CLKOUT. If used for data sampling, a phase clock that lags the phase clock most in synchronization may be selected to appear at CLKOUT. This guarantees that sampled data are static during sampling. This system is less complex and consumes minimal power over systems using variable delay circuits.

(Figure 2 is suitable for publication)