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(54) **Title:** HIGH-PERFORMANCE CODE PARALLELIZATION COMPILER WITH LOOP-LEVEL PARALLELIZATION

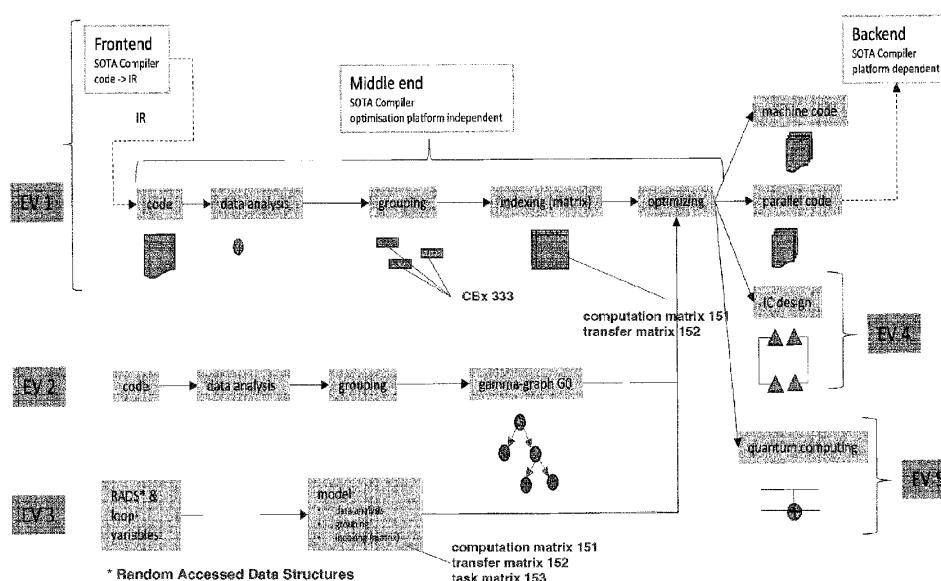


Fig. 106

(57) Abstract: Proposed is a system for generic static multiple issue CPU design with static pipelining of auto-parallelized code, and method thereof. The multi-core and/or multiprocessor integrated circuit (2) has a plurality of processing units (21) and/or processing pipelines (53) simultaneously processing instructions on data by executing a parallelized processing machine code (32). The execution of the parallelized processing code (32) by the parallel processing multi-core and/or multi-processor integrated circuit (2) comprises the occurrence of latency times (26), where the latency times being given by idle time of a processing unit (21) between transmitting data back after having processed a specific block of instructions of the processing code (32) on the data by the processing unit (21) and receiving data necessary for execution of a consecutive block of instructions of the processing code (32) by said processing units (21). The parallel pipelines (53) comprise means for (i) forwarding by providing data forwarding from a MEM stage as EX/MEM register to

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EX stage as ID/EX-stage register; (ii) exchanging by providing result exchange between pipelines by making Ex-MEM-stage register results accessible to the EX stage of a parallel pipeline (53), and (iii) branch pipeline flushing by providing a control hazard by flushing only those pipelines (53) depending on one pipeline (53) by computing condition based on branch addresses.