Claims

1. A light emitting diode structure comprising:

a p-type region;

an n-type region;

a light emitting region for recombination of carriers injectable by the p-type region and the n-type region, wherein the p-type region and the n-type region are on the same side of the light emitting region; and

a via passing through the light emitting region, wherein the via defines the perimeter of a light emitting surface of at least one pixel and comprises a material configured to enable injection of carriers into the p-type region or the n-type region, wherein one of the p-type region and n-type region is configured such that carriers generated in the one of the p-type region and the n-type region diffuses through the other one of the n-type region and the p-type region prior to recombination in the light emitting region.

2. The light emitting diode structure of claim 1, wherein the light emitting region comprises at least one epitaxial quantum well layer ~~and/or wherein the p-type region and the n-type region are on the same side of the light emitting region~~.

3. The light emitting diode structure of any one of the preceding claims, wherein the via~~material~~ comprises a further~~at least part of the~~ n-type region or p-type region ~~and/or wherein the material comprises a conductive material, preferably wherein the conductive material is a metal~~.

4. The light emitting diode structure of any one of the preceding claims, comprising a further light emitting region, ~~preferably wherein the light emitting region and the further light emitting region are separated by an undoped region thereby to provide a stack of light emitting regions, more preferably~~ wherein the via passes through both the light emitting region and the further light emitting region, ~~yet more preferably~~ wherein the light emitting region and the further light emitting region are configured to emit light of different wavelengths and ~~, still more preferably~~ wherein the light

emitting region and the further light emitting region are arranged such that the surface areas of the light emitting region and further light emitting region partially overlap.

5. The light emitting diode structure of claim 4, comprising at least three light emitting regions, wherein one of the light emitting regions emits blue light, one of the light emitting regions emits green light and one of the light emitting regions emits red light.

6. The light emitting diode structure of any one of the preceding claims, wherein the via is a grid via defining an array comprising a plurality of pixels, ~~preferably~~ wherein the grid via is arranged to provide a common electrode~~, more preferably wherein at least one pixel of the plurality of pixels comprises a further electrode, preferably wherein the further electrode is centrally located within the perimeter of the light emitting surface of at least one pixel, yet more preferably wherein at least two pixels are configured to emit light of different wavelengths~~.

7. The light emitting diode structure of any one of the preceding claims, wherein at least one of the light emitting region and~~/or~~ the further light emitting region is formed on an undoped epitaxial layer~~ and/or wherein the light emitting region and/or further light emitting region is formed between undoped epitaxial layers, preferably~~ wherein the undoped epitaxial layer is formed on a barrier layer configured to block vertical carrier diffusion~~, more preferably wherein the undoped epitaxial layer is gallium nitride, yet more preferably wherein the barrier layer is AlGaN~~.

8. The light emitting diode structure of any one of the preceding claims, wherein at least one of the n-type region and the p-type region is a planar region~~formed in a via~~ that is connected to a further~~planar~~ n-type region or a further~~planar~~ p-type region respectively, the further n-type region or the further p-type region being formed in the via.

9. The light emitting diode structure of any one of the preceding claims, wherein the light emitting surface has an area based on the diffusion length of carriers within the light

emitting region~~at least one of the n-type region and the p-type region is formed by selected area growth~~.

10. The light emitting diode structure of any one of the preceding claims, ~~wherein the via is an etched via and/or wherein the light emitting surface has an area based on the diffusion length of carriers within the light emitting region, preferably~~ wherein the light emitting surface area is less than or equal to 100μm^2~~, and more preferably less than or equal to 16μm^2~~.

11. The light emitting diode structure of any one of the preceding claims, wherein the at least one pixel is defined peripherally entirely by a single electrode.

12. A ~~high resolution~~ micro LED array comprising the light emitting diode structure of any one of claims 1 to 11.

13. The ~~high resolution~~ micro LED array of claim 12, wherein the array is a multi-colour array, ~~preferably~~ wherein the array has a pixel pitch less than 10 microns~~, more preferably less than 4 microns~~.

14. A method of forming a light emitting diode structure comprising:

forming a p-type region;

forming an n-type region;

forming an light emitting region for recombination of carriers injectable by the p-type region and the n-type region, wherein the p-type region and the n-type region are on the same side of the light emitting region; and

forming a via passing through the light emitting region, wherein the via defines the perimeter of a light emitting surface of at least one pixel and comprises a material configured to enable injection of carriers into the p-type region or the n-type region, wherein one of the p-type region and n-type region is configured such that carriers generated in the one of the p-type region and the n-type region diffuses through the other one of the n-type region and the p-type region prior to recombination in the light emitting region.

15. The method of claim 14 wherein forming the light emitting region comprises forming at least one epitaxial quantum well layer.

~~16. The method of claim 14, comprising forming the p-type region and the n-type region are on the same side of the light emitting region.~~

~~17.~~16. The method of ~~any of~~ claims 14 or 15~~to 16~~, wherein the via~~material~~ comprises a further~~t least part of the~~ p-type region or ~~the~~ n-type region ~~and/or wherein the material comprises a conductive material, preferably wherein the conductive material is a metal~~.

~~18.~~17. The method of any one of claims 14 to 1~~67~~, comprising providing a further light emitting region, ~~preferably wherein the light emitting region and the further light emitting region are separated by an undoped region thereby to provide a stack of light emitting regions, more preferably~~ wherein the via passes through both the light emitting region and the further light emitting region, ~~yet more preferably~~ wherein the light emitting region and the further light emitting region are configured to emit light of different wavelengths and~~, still more preferably~~ wherein the light emitting region and the further light emitting region are arranged such that the surface areas of the light emitting region and further light emitting region partially overlap.

~~19.~~18. The method of ~~any of~~ claim 1~~78~~, comprising at least three light emitting regions, wherein one of the light emitting regions emits blue light, one of the light emitting regions emits green light and one of the light emitting regions emits red light~~, preferably wherein the planar surface area of the further light emitting region is less than the planar surface area of the light emitting region~~.

~~20.~~19. The method of any one of claims 14 to 1~~89~~, wherein the via is a grid via defining a plurality of pixels, ~~preferably~~ wherein the grid is arranged to provide a common electrode~~, preferably further comprising forming a further electrode for at least one of the pixels, more preferably wherein the further electrode is formed centrally within~~

~~the perimeter of the light emitting surface of the at least one pixel, yet more preferably wherein at least two pixels are configured to emit light of different wavelengths~~.

~~21.~~20. The method of any one of claims 14 to 19~~20~~, comprising forming the n-type region and the p-type region as a planar region~~in a via~~ that is connected to a further~~planar~~ n-type region or ~~a planar~~ p-type region respectively, the further n-type region or the further p-type region being formed in the via.

~~22.~~21. The method of any one of claims 14 to 20~~1~~, comprising forming at least one of the n-type region and the p-type region by selected area growth.

~~23.~~22. The method of any one of claims 14 to 21~~2~~, comprising etching through the light emitting region to form the via defining the perimeter of the light emitting surface.

~~24.~~23. The method of any one of claims 18 to 21~~2~~, when dependent on claim 17~~18~~, comprising at least partially etching through at least one light emitting region in order locally to remove an unwanted longest wavelength~~, preferably~~ prior to forming each of the n-type region and the p-type region associated with the light emitting region and the further light emitting region respectively.

~~25.~~24. A method of forming an ~~high resolution~~ LED array comprising any of claims 14 to 23~~4~~.