CLAIMS

1. A process for transferring a thin layer to a carrier substrate, comprising the following steps:
- preparing a carrier substrate using a preparation process comprising the provision of a base substrate that has, on a main face, a charge-trapping layer and the formation of a dielectric layer having a thickness greater than 200 nm on the charge-trapping layer, the formation of the dielectric layer simultaneously implementing the deposition and the ion sputtering of the dielectric layer;
- joining, by means of molecular bonding and without preparing the free face of the dielectric layer by polishing, a donor substrate to the dielectric layer of the carrier substrate, the donor substrate featuring a weakened plane defining the thin layer;
- splitting the donor substrate at the weakened plane so as to release the thin layer and transfer it to the carrier substrate.

2. The process according to claim 1, wherein the preparation process comprises the formation of a bow compensation layer on a back face of the base substrate, opposite the main face.

3. The process according to claim 2, wherein the bow compensation layer has a thickness of between 500 nm and 1000 nm.

4. The process according to one of the preceding claims, wherein the base substrate is a monocrystalline silicon substrate exhibiting a resistivity higher than 600 ohm.cm.

5. The process according to one of the preceding claims, wherein the charge-trapping layer comprises polycrystalline silicon.

6. The process according to one of the preceding claims, wherein the charge-trapping layer comprises carbon.

7. The process according to one of the preceding claims, wherein the charge-trapping layer has a thickness of between 1 micron and 20 microns.

8. The process according to one of the preceding claims, wherein the dielectric layer consists of silicon oxide.

9. The process according to one of the preceding claims, wherein the dielectric layer comprises a barrier layer made of silicon nitride or of silicon oxynitride.

10. The process according to one of the preceding claims, wherein the dielectric layer has a thickness of between 200 nm and 10 microns, and preferably between 600 nm and 10 microns.

11. The process according to one of the preceding claims, wherein the deposition/sputtering ratio is between 1 and 10, preferably between 2 and 5.

12. The process according to one of the preceding claims, wherein the dielectric layer is formed at a temperature of between 300°C and 450°C, preferably between 350°C and 400°C.

13. The process according to one of the preceding claims, wherein the dielectric layer is formed in an atmosphere exhibiting a pressure lower than atmospheric pressure.

14. The process according to one of the preceding claims, further comprising an operation of annealing the dielectric layer in a neutral atmosphere and at a temperature exceeding the temperature of formation of the dielectric layer, preferably lower than 950°C.

15. The process according to one of the preceding claims, wherein the free face of the dielectric layer exhibits a roughness lower than 0.5 nm in terms of RMS value over a field of measurement of 10 microns by 10 microns.

16. The process according to one of the preceding claims, wherein the donor substrate is devoid of any dielectric surface layer.